CprE 381, Computer Organization and Assembly Level Programming

Team Contract – Project Part 1

Team Members: **Jayson Acosta, Parnika Dasgupta, Nakota Clark**

Project Teams Group #: **Section D_01**

Discuss the following aspects of teamwork with your team – make sure to get input from each member. Write down your team's consensus for each of the bolded headings. Italicized text contains instructions and examples and should be deleted once you've read it. Please see the example contract for rough length expectations.

Course Goals: *List and acknowledge the goals of your individual team members. Examples may include:*

- *learn everything about computer architecture*
- *know enough to understand security risks posed by hardware primitives*
- *get an A/B/C/Pass in the course*
- *minimize the number of lost points*
- *prepare myself for a career in hardware design*
- *prepare myself to be able to do research involving FPGAs*
- *be able to explain the workings of a stored-program computer from gates to C*

Team Expectations:

- **Conduct:** *What are the expectations for personal conduct of group members?*
- **Communication:** *What is the best mode of communication for the group? How often should communication occur? How fast should a response be expected?*

We will be communicating with each other through a group chat, updating each other whenever we have completed something or need help.

- **Group conventions:** *Naming conventions? Compilation and simulation methodology? Testbench strategies? Do file usage? Version control strategies? Commenting standards?*

Naming Conventions: Test benches will be named tb_<component>.vhd. We will also use snake_case for naming
Compilation and Simulation: When one person completes a component, the other two members will test and approve its addition
Testbench Strategies: Testbenches should test multiple configurations for normal cases and should have some tests for fringe cases as well
Do Files: Do file usage is not mandatory. If its usage would make things easier it is encouraged.

Version Control: We will use Gitlab for our programming and Google drive to store other files.

- **Meetings:** *Given the significant portion of the course that the lab covers, it is expected that your team will spend more time working on the labs than in your scheduled lab sections. How will your group expect to handle this? Please include at least two additional times outside of lab that your team can meet (preferably in-person).*

  We decided that we are going to meet every Wednesday and discuss the Project and then distribute work among ourselves. Every Wednesday, we will come and discuss our progress and how we can help each other. Based on the workload, we may decide to meet more during the week as well. Other than that, we have an active group-chat, where we keep discussing things.

Group members will work on their own and combine what is complete during lab sections and meetings twice a week, one day on the weekend and one day on the weekdays sometime between 4pm to 8pm decided a few days beforehand.

- **Peer Evaluation Criteria:** *Please create a brief criteria for how effort and contribution are defined. Note that teams with **vastly** divergent scores may require a meeting with course instructors and result in different grades for different group members. Teams with reasonably equitable scores will receive the same grade.*

Effort and contribution will be based on the team member completing their assigned components in a timely manner. The work should be shared roughly equally, so that everyone contributes a similar amount.

Communication is very important. If someone needs help, or an extension, it is very important to let the other team members know that in advance.

Role Responsibilities: *Complete the following planning table. Each lab part should be the responsibility of one team member. Also make sure that no one team member is the lead on both the design and test aspects of a single lab part. These guidelines aid in all students having a complete view of the lab. Note that the non-lead is encouraged to participate and support the lead wherever possible, increasing both the quality of the lab part and each team member's knowledge.*

Lab Part	Estimated Time	Design		Test	
		Lead	Timeline	Lead	Timeline
High-level design	1 hr	PD	Week 1	JA NC	Week 2
Test programs	4 hr	PD	Rolling	JA	Rolling
Control logic	2 hr	JA	Week 1	NC	Week 2
Fetch logic	3 hr	JA	Week 2	NC	Week 3
Barrel shifter	2 hr	NC	Week 2	PD	Week 3
ALU integration + Misc updates	2 hr	JA	Week 2	NC	Week 3

High-level integration	4 hr	NC	Week 3	PD	Week 4
Synthesis (human effort)	1.5 hr	JA PD	Week 3	NC	Week 4

*Estimated Time is given as a **very rough** guide for even distribution of tasks assuming you've already read through the lab document and have the prerequisite knowledge. Depending on your group's skill and prerequisite knowledge, some tasks may take disproportionately long or short. For your future planning, track this – for future prelabs you will be asked to note why past tasks took longer than expected and how you might avoid such issues in the future.*

Integrity of Work: *Do not delete the following.* We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature Jayson Acosta **Date** 10/2/2024

Student Signature Parnika Dasgupta **Date** 10/2/2024

Student Signature Nakota Clark **Date** 10/2/2024