DESIGN OF CMOS BASED ARTIFICIAL NEURAL NETWORKS

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***Abstract*—Analog artificial neural networks (ANNs) present a promising approach to achieving efficient computation for AI applications by leveraging CMOS circuits. In this paper, we introduce a CMOS-based implementation of an ANN, focusing on the design of a multiplier for neuron-level multiplication and exploring various CMOS-based activation circuits. Our approach to activation functions examines sigmoid to identify configurations compatible with CMOS technology, ensuring minimal power consumption and enhanced integration. This work contributes to the development of low-power, high-performance ANNs that can potentially scale for larger analog-based neural networks.**

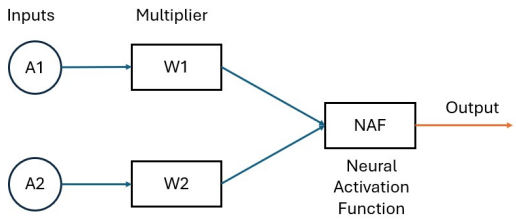
Keywords: *ANN, CMOS, Activation function, AI&ML*

I. INTRODUCTION

The rapid growth of artificial intelligence (AI) and machine learning (ML) has led to a significant demand for efficient and scalable neural network hardware. Analog CMOS circuits offer an energy-efficient allowing for low-power neural network designs. In this paper, we explore a CMOS-based analog implementation of an ANN, focusing on the design of critical components at the neuron level, including the multiplier and activation function circuits. The neuron's multiplication process is implemented using a Gilbert cell multiplier, a widely recognized topology in analog design due to its precision, stability, and ease of integration within CMOS technology. By leveraging the Gilbert cell's ability to perform current-mode multiplication, we achieve the weighted summation necessary for neural network computation in a compact and power-efficient form. In addition to the multiplication, the activation function is a fundamental operation within each neuron that introduces non-linearity to the network. This design enables the realization of analog ANNs that retain computational effectiveness while significantly reducing power requirements compared to digital counterparts. This work contributes to the growing field of analog neural networks by demonstrating a CMOS-based implementation that can operate efficiently in constrained environments, setting a foundation for further advancements in energy-efficient AI hardware.

II.PRINCIPLE OF GENERATION

The core principle behind this CMOS-based neural network is the analog emulation of neuron functions, which include weighted summation (multiplication) and activation. The analog approach leverages continuous current or voltage levels rather than discrete values, allowing efficient computation with lower power requirements. This section covers the two main components of our CMOS neuron design: the Gilbert cell multiplier for the weighted summation and the activation function circuit for introducing non-linearity.



III. ISSUES AND IMPROVEMENTS

Analog circuits, unlike digital ones, are highly sensitive to noise, which can introduce errors in signal accuracy. For CMOS-based neural networks, noise can cause unintended variations in the weighted summation or distort the activation function, ultimately impacting network performance. Careful layout design, shielding, and proper grounding to reduce noise interference. Additionally, using differential signaling and precise transistor matching can help minimize the impact of noise.

IV. CONCLUSION

This work presents a CMOS-based analog artificial neural network (ANN) design, incorporating multiplier for efficient weighted summation and a CMOS-compatible circuits for activation functions. Our approach demonstrates the viability of using analog circuits to replicate neural network computations, achieving reduced power consumption and area requirements compared to traditional digital implementations. Future work could focus on optimizing the circuit for larger, more complex neural networks and exploring alternative activation functions to enhance computational capabilities. Overall, this research underscores the potential of analog ANNs in the quest for efficient and scalable AI hardware, paving the way for further advancements in low-power, high-performance neural network implementations.

V. REFERENCE

[1] https://www.geeksforgeeks.org/introduction-to-ann-set-4-network-architectures

[2] CMOS Implementation of ANNs Based on Analog Optimization of N-Dimensional Objective Functions. Sensors **2021**,