CSE231 Operating System (Section B), Quiz 2 Monsoon 2024

Name	
Roll Number	

Instructions:
• This is a closed book and closed notes quiz. Please be aware of the strict plagiarism policy. • For questions requiring justification, please be as concise as possible. 2-3 sentences would be the ideal size of a justification. No extra pages will be provided.

1. What is the primary function of the Memory Management Unit (MMU)?
- a. Handle disk I/O to physical addresses
- b. **Translate virtual addresses**
- c. Manage CPU register operations
- d. Control file system

2. The _____ is used as an index into the page table.
- a. Frame bit
- b. **Page number**
- c. Page offset
- d. Frame offset

3. With paging, there is no ____ fragmentation.
- a. Internal
- b. **External**
- c. Either type of
- d. None of the mentioned

4. Consider the following statements:
S1: A small page size causes large page tables.
S2: Internal fragmentation is increased with small pages.
S3: I/O transfers are more efficient with large pages.
- a. S1, and S2 are true
- b. **S1 is true, and S2 is false**
- c. S2 and S3 are true
- d. S1 is true, and S3 is false

5. Consider the page sequence 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 1, 7, 0, 1 and a cache size of 4. Calculate the number of page faults using the optimal page replacement algorithm.
- a. 7
- b. 9
- c**. 8**
- d. 6

6. The essential contents in each entry of a page table is/are
- a. Page access information
- b. Page frame number
- c. Virtual page number
- d. **Both b & c**

7. The physical address generated by the CPU is referred to as
- a. Physical address
- b. **Logical address**
- c. Neither physical nor logical
- d. None of the mentioned

8. Swap space is allocated ____
- a. **As a chunk of disk**
- b. Separate from a file system
- c. In the main memory
- d. All of the mentioned

9. Virtual memory is
- a. Large secondary memory
- b. Large main memory
- c.**Illusion of large main memory**
- d. None of the above

10. Paging helps to eliminate which of the following?

a. Internal fragmentation
b. **External fragmentation**
c. Memory tasks
d. Deadlocks

11. Consider the page sequence 5, 7,0,3,5,0,1,8,5 and a cache size 3. Which page will be evicted first from the cache in Optimal Page Replacement policy ?

a. 0
b**. 7**
c. 5
d. 8

12. Dirty bit for a page in a page table

a. **Helps avoid unnecessary writes to the disk**
b. Helps maintain LRU information
c. Allows only read on a page
d. None of the above

13. Increasing the RAM of a computer typically improves performance because

a. Virtual memory increases
b. **Fewer page faults occur**
c. Larger RAMs are faster
d. Fewer segmentation faults occur

14. When the page fault rate is low

a. The turnaround time increases
b. The effective access time increases
c. **The effective access time decreases**
d. Turnaround time and effective access time increases

15. In the context of operating systems, which of the following statements is/are correct with respect to paging?

a. **Paging helps solve the issue of external fragmentation**
b. Page size has no impact on internal fragmentation
c. **Paging incurs memory overheads**
d. Multi-level paging is necessary to support pages of different sizes

16. A multilevel page table is preferred in comparison to a single-level page table for translating virtual address to physical address because

a. It reduces the memory access time to read or write a memory location.
b. **It helps to reduce the size of the page table needed to implement the virtual address space of a process.**
c. It is required by the translation lookaside buffer.
d. It helps to reduce the number of page faults in page replacement algorithms.

17. Which of the following statements is/are true regarding the functions of the OS and MMU in a modern computer system?

a. **The OS sets the address of the page table in a CPU register accessible to MMU every time a new process is created in the system**
b. **The OS sets the address of the page table in a CPU register accessible to the MMU every time a new process is context-switched by the CPU scheduler**
c. MMU traps to OS every time an address is not found in the TLB cache.
d. **MMU traps to OS every time it cannot translate an address using the page table available to it.**

18. Which of the following statements best describes dynamic relocation using the base and bound registers?

a. It is a method where a virtual address is converted to a physical address at compile

time.

b. **It is a method where a virtual address is converted to a physical address at execution time using base and bound registers.**

c. It involves converting physical addresses to virtual addresses using a page table.

d. It uses a stack-based approach for address translation.

19. Which of the following statements is/are true regarding the functions of the OS and MMU in a modern computer system?

a. MMU helps the OS in context switching the processes.

b. **The OS sets the address of the page table in a CPU register accessible to the MMU every time a new process is context-switched in by the CPU scheduler**

c. **MMU traps to OS every time it cannot translate an address using the page table available to it.**

d. None of the above

20. What is the primary function of the Memory Management Unit(MMU)?

a. To manage CPU scheduling

b. **To translate virtual addresses to physical addresses**

c. To execute instructions in parallel

d. To manage I/O operations

21. In dynamic relocation using base and bound registers, what do the base and bound registers specify?

a. Base specifies the virtual address space and bound specifies the physical address space.

b. **Base specifies the starting address of the process in physical memory, and bound specifies the size of the process.**

c. Base specifies the physical address space, and bound specifies the virtual address space.

d. Base and bound are both used to specify the size of the virtual memory.

22. Which of the following statements about multi-level paging is true?

a. It uses a single-level page table to map virtual addresses

b. **It reduces the amount of memory required for page tables**

c. It eliminates the need for paging entirely

d. It increases the amount of memory required for page tables.

23. How does the TLB improve system performance?

a. By eliminating the need for a page table.

b. By storing frequently used in physical memory.

c. **By caching recent virtual-to-physical address translations.**

d. By reducing the size of the page table

24. Which of the following is a characteristic of segmentation in memory management?

a. Fixed-size blocks of memory

b. **Logical division of memory into segments of varying sizes**

c. Uses page tables to translate addresses

d. It is not a memory management technique

25. In a system using dynamic relocation with base and bound registers, what happens if a process attempts to access an address outside its bounds?

a. The process is allowed to access the address, and the data is fetched from memory

b. The system crashes immediately

c. **The MMU generates an interrupt, leading to a segmentation fault.**

d. The address is automatically adjusted to the nearest valid address.

26. When do the following occur: (i) Page Fault, (ii) Thrashing

A Page Fault occurs when a process accesses an address in a page which is not currently resident in memory. Thrashing occurs when the incidence of page faults becomes so high that the system spends all its time swapping pages rather than doing useful work.

27. A machine has 64-bit virtual addresses and 48-bit physical addresses. Page size is 16K. How many entries are needed in a conventional page table?

(2^50)

28. Explain the concept of dynamic relocation using the base and bound registers. How does it work?

The base register holds the starting physical address of a process's memory segment, while the bound register indicates the upper limit of the segment. When a virtual address is generated, the MMU adds the base address to the virtual address to compute the physical address. If the resulting address exceeds the bound register, an exception occurs, preventing access outside the allocated segment, thereby ensuring memory protection.

29. What is a Translation Lookaside Buffer (TLB), and how does it improve address translation performance?

A Translation Lookaside Buffer (TLB) is a specialized cache that stores a limited number of recently used virtual-to-physical address translations. When the MMU needs to translate a virtual address, it first checks the TLB. If the translation is found (a TLB hit), it is used directly, leading to faster access. If not (a TLB miss), the MMU must consult the page table, which is slower. The TLB improves performance by reducing the average time to access memory, as TLB hits significantly speed up address translation compared to accessing the page table in main memory.

30. The page size in a system (running a Linux-like operating system on x86 hardware) is increased while keeping everything else (including the total size of main memory) the same. For each of the following metrics below, indicate whether the metric is *generally* expected to increase, decrease, or not change as a result of this increase in page size. (i) Size of the page table of a process. (ii) TLB hit rate. (iii) Internal fragmentation of main memory.

(a) PT size decreases (fewer entries)
(b) TLB hit rate increases (more coverage)
(c) Internal fragmentation increases (more space wasted in a page)