RESULT ANALYZATION

Simulation Process

To run simulation of Mod-12 Synchronous Up/Down Loadable Counter , we used Makefile utilities and it is in simulation folder.by giving "**Make help**" command you can see all available option, similar to below:

```
================================================================================================
 USAGE         -- make target
 clean         => clean the earlier log and intermediate files.
 sv_cmp    => Create library and compile the code.
 TC1       => To compile and run the testcase1 in batch mode.
 TC2       => To compile and run the testcase2 in batch mode.(This testcase is not written,if you want you can extend it(Testcase 1(TC1) covered 10
0%
 report_12 => To merge coverage reports for testcases TC1 and  convert to html format.
 covhtml              => To view the coverage report in firefox.
 covtxt   => To view the coverage report in text editor [only for VCS]
cov_verdi      => To view the coverage report in verdi [only for VCS]
================================================================================================
```

- Now based on your target you can run commands, but the exact order to run commands is..
    1. Make sv_cmp
    2. Make TC1.
    3. Make report_1.
    4. Make covhtml or Make cov_verdi

1. Make sv_cmp

This complies the code for any syntax errors, if no errors it complies 5 Modules.

2.Make TC1

TC1 means Test case 1, default it applied with 100 transactions, you can change in top module if you want as number of transactions.

It displays the **Write Driver**, **write monitor**, **Reference Model** and **Read Monitor data**

At end how many transactions is generated and how many transactions is received from read monitor and reference model will be updated in scoreboard and no. of matched data also.

```
============================================================
============================================================
DATA FROM REFERENCE MODEL
        Data_out=1
        Data_in=3
        Load=1
        Mode=0
        Reset=0
============================================================
Data Matched
====================================================================
100 Read Data Generated, 100 Received Data, 100 Read data Verified

====================================================================
$finish called from file "../test/counter_top..sv", line 28.
$finish at simulation time                1045
           V C S   S i m u l a t i o n   R e p o r t
Time: 1045
CPU Time:      0.340 seconds;       Data structure size:   0.0Mb
Wed Apr 10 16:05:16 2024
urg -dir cov1.vdb -format both -report urgReport
Note: Bumping stack limit from 8192 to unlimited Kbytes.
URG Version T-2022.06-SP1                    Copyright (c) 1991 -  Synopsys, Inc.
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Note-[URG-RDG] Report directory generated
  Report written to directory urgReport
```

3.Make report_1

After simulation the coverage report need to be saved in directory and to convert it to html.

When TC1 cmd is runed at that time also it shows same message at end but it is not converted to html

```
Note-[URG-RDG] Report directory generated
  Report written to directory urgReport
```

4.Make covhtml or Make cov_verdi

If you want to view the coverage report in html go for **Make covhtml.** for simple and easy to understand the coverage report.

If you have Synopsys Verdi tool, the better to open with **Make cov_verdi** as it gives more detailed version than html, you will know which line is not covered and also it is displayed in the same tool.

```
                              Verdi (R)

                Version T-2022.06-SP1 for linux64 - Aug 28, 2022

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```
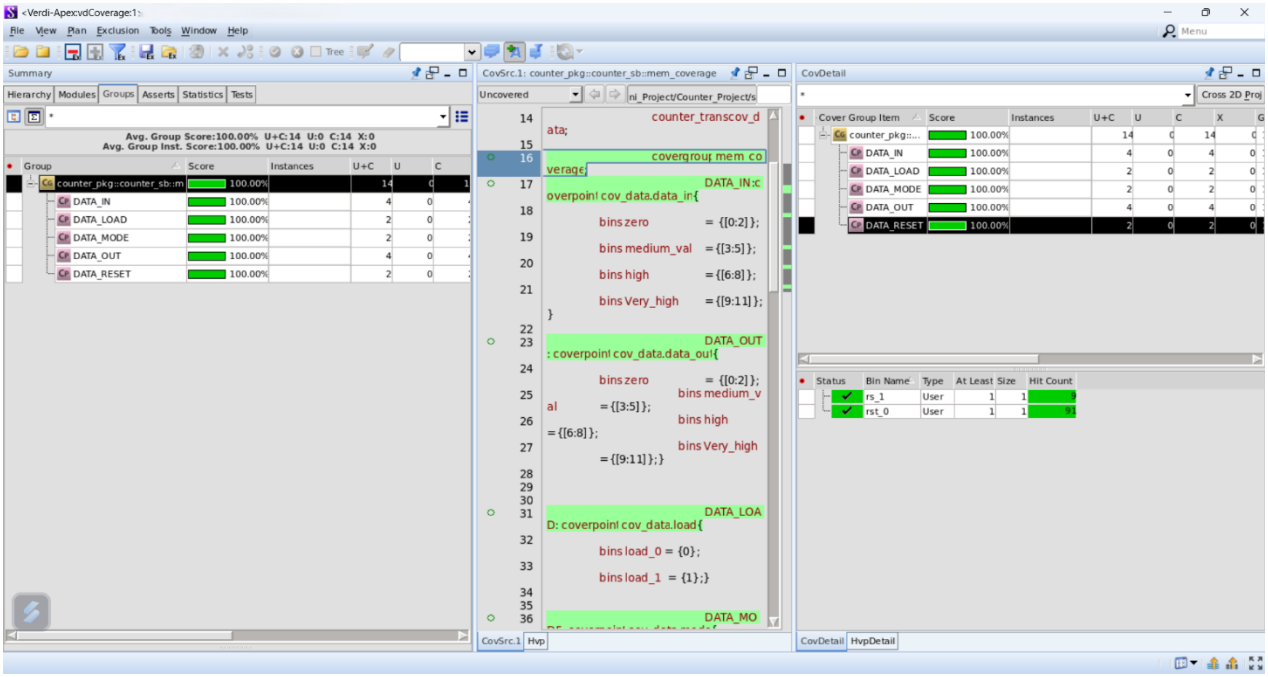
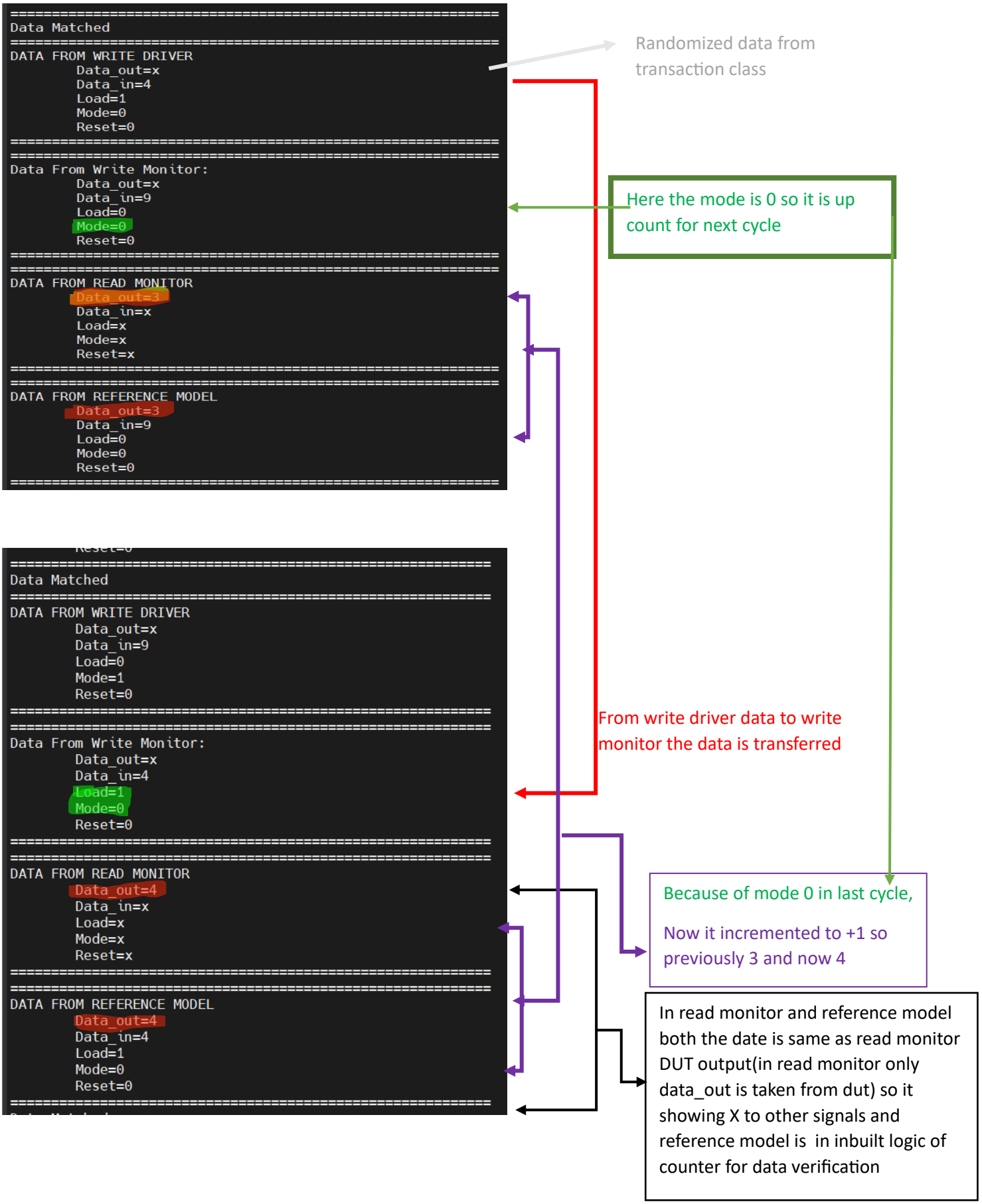



HOW TO ANALYSE THE COUNTING VALUE

When simulation is completed you can observe the values will print from write monitor and write driver and read monitor and reference model. ..similar to this

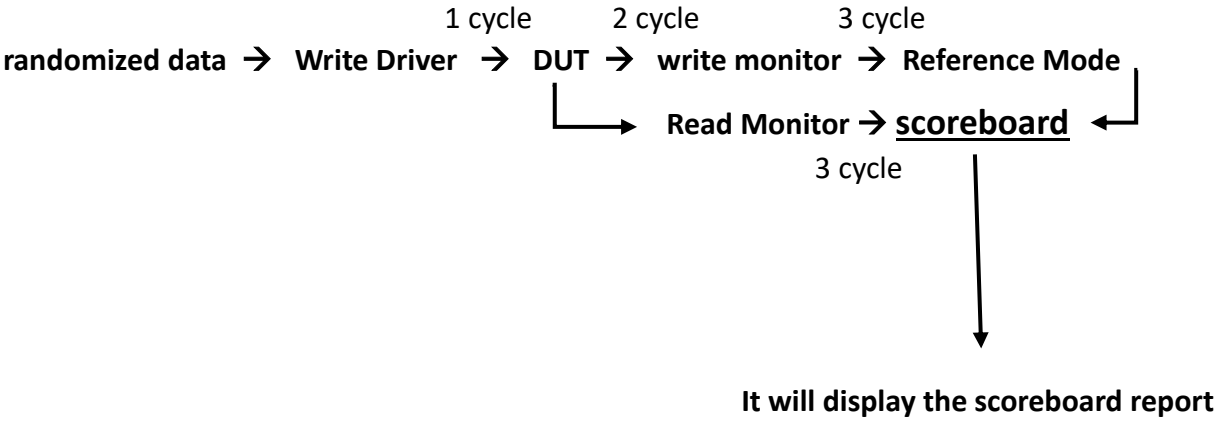


Note:

First randomized data will display

In first cycle of randomized data input for write driver the reset will high due to default setting when first simulation is started, in environment.

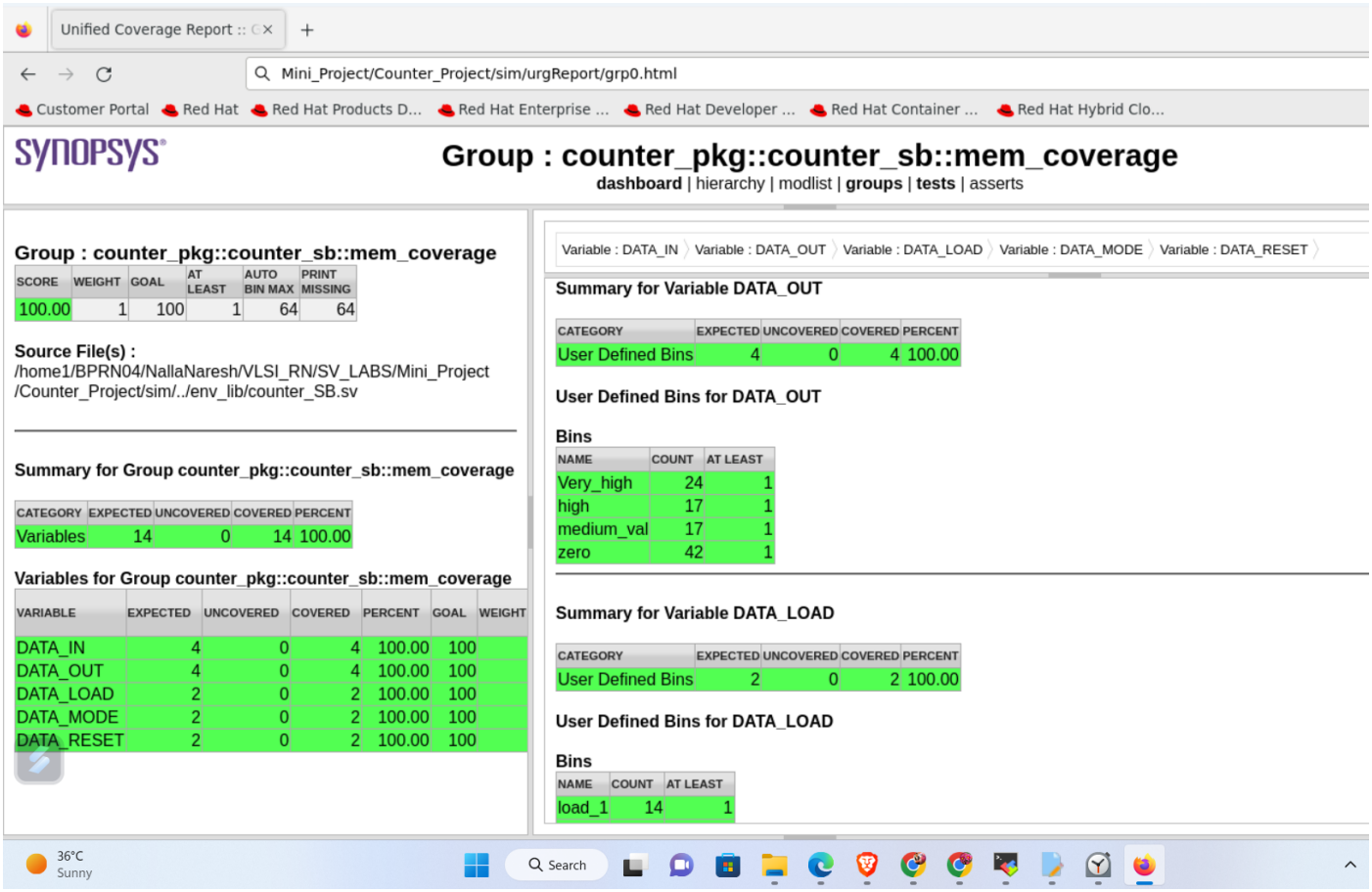
The count value will display to next cycle. always the write driver input will go to write monitor only in next cycle and then to ref model and read monitor but reference model and read monitor both works as parallelly



----Synopsys Verdi Tool----

If you licenced tool then you go with Verdi tool, else use html.

I covered 100% of functionality.



Download folders RTL , env, env_lib,test and simulation into a one folder .

Then go to simulation folder and from there you can use make file.

This make file can only run in batch mode.(in terminal)

==========END==========