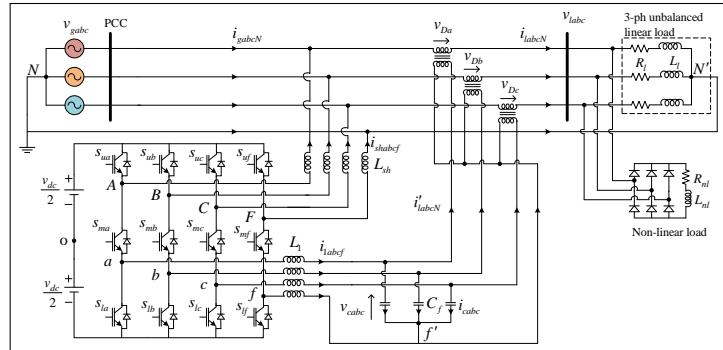




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INDIAN INSTITUTE OF
TECHNOLOGY
MADRAS
CHENNAI-600 036

AN IMPROVED SLIDING MODE CONTROL SCHEME FOR POWER QUALITY CONDITIONERS IN DISTRIBUTION SYSTEM



A thesis

Submitted by

LOKESH N

For the award of the degree

Of

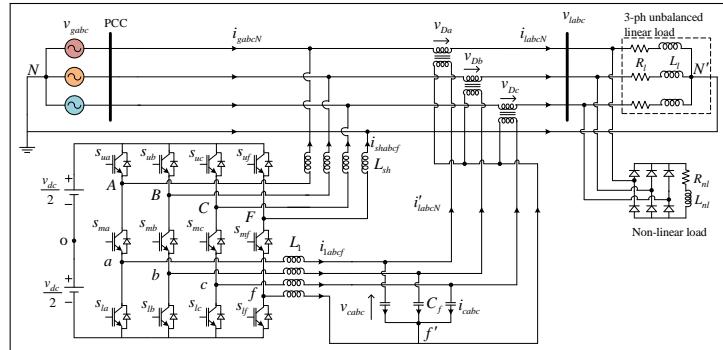
DOCTOR OF PHILOSOPHY

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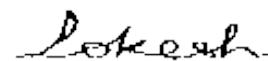
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THESIS CERTIFICATE

This is to undertake that the Thesis titled, ***AN IMPROVED SLIDING MODE CONTROL SCHEME FOR POWER QUALITY CONDITIONERS IN DISTRIBUTION SYSTEM*** submitted by me to the Indian Institute of Technology Madras, for the award of *Ph.D.* is a bonafide record of the research work done by me under the supervision of *Prof. Mahesh Kumar*. The contents of this Thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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LIST OF PUBLICATIONS

The publications arising out of the work mentioned in this thesis are given as follows.

PUBLICATIONS IN REFEREED JOURNALS

1. N. Lokesh and Mahesh K. Mishra, "Design of a Decoupled Sliding Mode Control for Four-Leg Distribution Static Compensator," *IEEE Transactions on Power Delivery*, vol. 37, no. 6, pp. 5014-5024, Dec. 2022.
2. N. Lokesh, Mahesh K. Mishra and A. Ghosh, "Sliding Mode Control of a Four-Leg Dynamic Voltage Restorer in a Natural Reference Frame," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 4, no. 3, pp. 919-927, July 2023.

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1. N. Lokesh, Mahesh K. Mishra and N.M.Ismail, "Variable Structure Control for Three phase-Three Wire Nine Switch Converter with LCL Filter," *2019 IEEE 13th International Conference on Power Electronics and Drive Systems (PEDS)*, Toulouse, France, 2019, pp. 1-5.
2. N. Lokesh and Mahesh K. Mishra, "A Robust Control Scheme for an Integrated Nine-Switch Power Quality Conditioner," *2019 National Power Electronics Conference (NPEC)*, Tiruchirappalli, India, 2019, pp. 1-6.
3. N. Lokesh and Mahesh K. Mishra, "A Comparative Performance Study of Advanced PLLs for Grid Synchronization," *2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE'2020)*, Cochin, India, 2020, pp. 1-6.

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Lokesh Nalla

ABSTRACT

KEYWORDS: Distribution static compensator, dual-output converter, dynamic voltage restorer, phase-locked loop (PLL), sliding mode control, unified power quality conditioner.

Distributed generation (DG) is a constantly evolving trend that connects renewable energy sources (RES) like solar and wind to the utility grid, in addition to the conventional energy sources like coal, oil, and gas. The widespread use of RESs and the power-switching electronics devices at the industrial and residential levels create power quality (PQ) issues. The custom power devices (CPD) were developed at the distribution system as a result of the severe regulations imposed on DG systems and the consumer demand for better PQ. This thesis is focused on improvements to the sliding mode control schemes of CPDs under various conditions and configurations, and an overview is given below.

Distribution static compensator (DSTATCOM), in general, improves current-related PQ issues, while dynamic voltage restorer (DVR), in general, improves voltage-related PQ concerns. The back-to-back (BTB) configuration of the unified power quality conditioner (UPQC) combines DSTATCOM and DVR. As a result, UPQC is a versatile CPD that can strengthen the system against both current and voltage-related PQ difficulties. However, the DVR converter is almost idle most of the time, since the occurrence of voltage related issues is less often. Thus, the converter utilization is poor with BTB configuration. To improve the converter utilization factor without compromising the functionalities of UPQC, the reduced switch count converter: dual-output converter (DOC) is considered in this thesis for UPQC system. The control algorithms of DOC based systems should include the control of converter neutral-point voltage in addition to current and voltage control. Further, accurate extraction of fundamental frequency positive sequence (FFPS) components and phase angle of grid voltages are required for an improved performance of UPQC system.

Therefore, the extraction of FFPS components based on the operators: second order

generalized integrator (SOGI), cascaded delayed signal cancellation (CDSC) and multiple delayed signal cancellation (MDSC) are reviewed. The extraction accuracy of three operators are evaluated, for various grid conditions, based on the quality of frequency output from synchronous reference frame (SRF) phase-locked loop (PLL). The performance comparison of these three operators based PLLs is presented using simulation results. The CDSC operator is found with superior performance characteristics and hence it is considered for the control of UPQC in this thesis.

The control algorithm can be implemented in any one of the reference frames: dq , $\alpha\beta$ and natural reference frame (abc). Due to availability of generation of reference voltages/currents in abc frame, implementing a suitable controller in the same reference frame would reduce the computational burden and the signal transformation errors. However, the three-phase three-leg or four-leg voltage source converters suffer from the coupling issue in abc frame. The dynamics of each state variable depends on the control inputs of all four legs of the converter. This coupling leads to difficulty in assigning appropriate values to the control inputs using a conventional sliding surface in sliding mode control (SMC) scheme. To address this, a new sliding surface is proposed for both four-leg converter based DSTATCOM and DVR systems. Simulation and experimental studies conducted on both systems are presented. The presented studies verify the performance of the proposed control scheme for both DSTATCOM and DVR systems. Further, the proposed scheme is extended for four-leg dual-output converter based UPQC and its performance verification is presented using simulation results.

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ABBREVIATIONS

3P4W	Three-Phase Four-Wire
3P3W	Three-Phase Three-Wire
AC	Alternating Current
ACD	Anti-Conjugate Decomposition
APF	Active Power Filter
BTB	Back-To-Back
CCM	Current Control Mode
CDSC	Cascaded Delayed Signal Cancellation
CMV	Common Mode Voltage
CPD	Custom Power Device
DC	Direct Current
DER	Distributed Energy Resource
DG	Distributed Generation
DOC	Dual-Output Converter
DSC	Delayed Signal Cancellation
DSO	Distribution System Operator
DSP	Digital Signal Processors
DSTATCOM	Distribution Static Compensator
DVR	Dynamic Voltage Restorer
EPLL	Enhanced Phase-Locked Loop
FFPS	Fundamental Frequency Positive Sequence
FL-VSC	Four-Leg Voltage Source Converter
FPSC	Fundamental Positive Sequence Components
HCC	Hysteresis Current Control
HPF	High Pass Filter
ISC	Instantaneous Symmetrical Components
ISCT	Instantaneous Symmetrical Components Theory
LED	Light Emitting Diode
LMS	Least-Mean-Square

LPF	Low Pass Filter
MDSC	Multiple Delayed Signal Cancellation
NPV	Neutral-Point Voltage
NSC	Nine-Switch Converter
PCC	Point of Common Coupling
PI	Proportional Integral
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
PQ	Power Quality
PR	Proportional Resonant
QSG	Quadrature Signal Generator
RES	Renewable Energy Sources
RMS	Root Mean Square
SMC	Sliding Mode Control
SMPWM	Sliding Mode Pulse Width Modulation
SOGI	Second Order Generalized Integrator
SPWM	Sinusoidal Pulse Width Modulation
SRF PLL	Synchronous Reference Frame Phase-Locked Loop
SSFCL	Solid State Fault Current Limiter
SSTS	Solid State Transfer Switch
TDVR	Transformer-less Dynamic Voltage Restorer
THD	Total Harmonic Distortion
TSC	Twelve-Switch Converter
UPQC	Unified Power Quality Conditioner
UPQC-L	Left Shunt Unified Power Quality Conditioner
UPQC-R	Right Shunt Unified Power Quality Conditioner
VCM	Voltage Control Mode
VSC	Voltage Source Converter
VSI	Voltage Source Inverter
VSS	Variable Structure System

NOTATIONS

C_{dc}	DC-link capacitance, μF
C_f	Filter capacitance of DVR, μF
i_g	Instantaneous grid current, A
i_l	Instantaneous load current, A
i'_l	Instantaneous current flowing through primary of DVR injection transformer, A
i_{sh}	Instantaneous DSTATCOM/shunt compensator current, A
L_1	Filter inductance of DVR, mH
L_g	Grid inductance, mH
L_l	Linear load inductance, mH
L_{nl}	Non-linear load inductance, mH
L_{sh}	Filter inductance of DSTATCOM/shunt compensator, mH
L_t	Equivalent inductance of DVR transformer, mH
R_g	Grid resistance, Ω
R_l	Linear load resistance, Ω
R_{nl}	Non-linear load resistance, Ω
R_{sh}	Filter resistance of DSTATCOM/shunt compensator, Ω
v_c	Instantaneous DVR filter voltage, V
v_{dc}	Instantaneous DC-link voltage, V
v_D	Instantaneous DVR voltage, V
$v_{f'o}$	Instantaneous NPV of DVR converter, V
v_g	Instantaneous grid voltage, V
v_{No}	Instantaneous NPV of DSTATCOM converter, V
v_p	Instantaneous PCC voltage, V
σ	Sliding variable
λ	Sliding coefficient
$sgn(\cdot)$	Signum function

CHAPTER 1

INTRODUCTION

An electric power source that is directly connected to the distribution network or located at the meter's client site is known as distributed generation (DG) [1]. Main objectives of the DG are to provide a reliable and quality power to the end consumers. In the past two decades, the adoption of renewable energy sources (RESs) has been increasing to mitigate carbon emissions and build resilience to volatile energy prices from geopolitical wars. Also, the usage of power electronics based utility devices such as LED lighting systems, adjustable speed drives, etc., has been increased in the distribution system. The large penetration of RESs and power switching electronic devices (non-linear loads) into distribution system leads to power quality (PQ) degradation. The non-linear loads draw harmonic currents through the distribution network, resulting in voltage distortion and additional losses in the network. Further, these loads raise the demand for reactive power, which eventually causes the voltage variations such as sag and swell at the point of common coupling (PCC). All of these issues are the reasons for low power factor, inefficient distribution network, work interruption of sensitive equipment, and overheating of transformers and feeder lines [2]. As a result, consumers and regulatory bodies that oversee and establish PQ standards became more aware of PQ issues. One of the widely accepted standards is IEEE-519 [3].

The installation of passive harmonic filters is the standard PQ improvement method used for many decades [4]. The passive filters can improve the power factor of inductive loads and offer harmonic mitigation for DG systems. However, they may not be as effective as they could be due to a number of factors, including pre-tuned compensation frequencies, the formation of harmonic parallel and/or series resonances between the

power system and the passive filter, and their component bulkiness [5]. To overcome the problems with passive filters and to improve PQ in distribution system, active power filters (APFs) are developed [6–9]. The APFs are referred as custom power devices (CPDs) when they are employed in distribution network.

1.1 CUSTOM POWER DEVICES

Typically, the custom power devices (CPDs) are used to provide quality power to the end consumers in the distribution system. The CPDs can also be known as power quality conditioners (PQCs) as they provide quality power to the customers. The family of CPDs includes distribution static compensator (DSTATCOM), dynamic voltage restorer (DVR), unified power quality conditioner (UPQC), solid state transfer switch (SSTS), and solid state fault current limiter (SSFCL). In this section, a brief description of the DSTATCOM, DVR, and UPQC has been presented.

1.1.1 Distribution Static Compensator

The distribution static compensator (DSTATCOM), shunt connected custom power device, solves current-based quality problems in the distribution network. The DSTATCOM injects portion of load currents based on the requirement of consumer and/or distribution system operator (DSO) [8, 10–12]. For instance, to achieve unity power factor, harmonic filtering and load balancing at PCC, the DSTATCOM injects the load current components of harmonic, fundamental reactive, negative and zero sequence currents. The DSTATCOM is generally consists of a voltage source inverter (VSI), filter inductor and the DC storage capacitor as shown in Fig. 1.1.

1.1.2 Dynamic Voltage Restorer

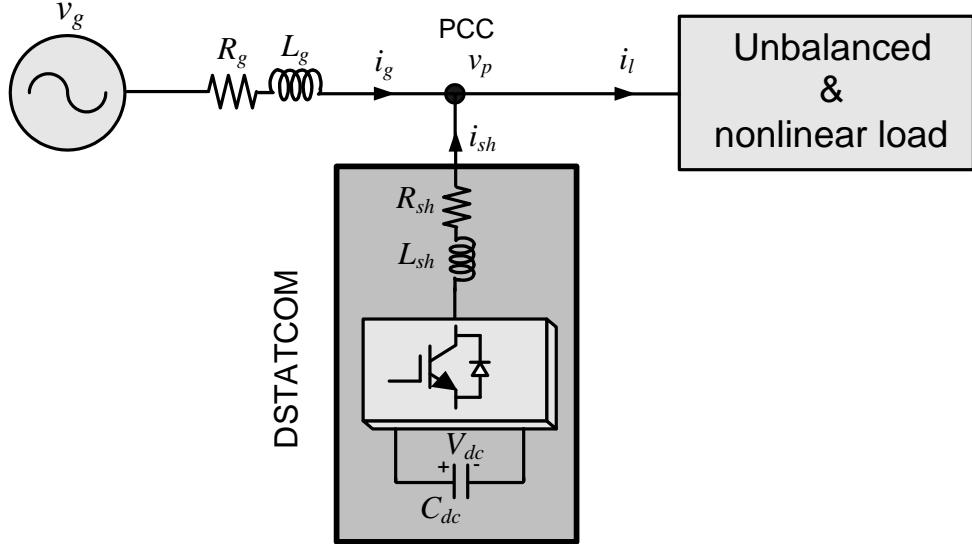


Figure 1.1: Single-line diagram of DSTATCOM

The dynamic voltage regulator (DVR), series connected custom power device, solves voltage-based quality problems in the distribution network. The DVR injects voltage in series with the grid voltage such that the load voltage is maintained as a balanced sinusoidal waveform with a desired amplitude [13]. The primary goal of the DVR is to protect sensitive loads from voltage sag/swell, harmonics and interruptions in the supply side voltage [14, 15]. Fig. 1.2 shows a single-line diagram of DVR system coupled to a distribution system. The DVR consists of VSI, LC filter, injection transformers and the DC storage capacitor.

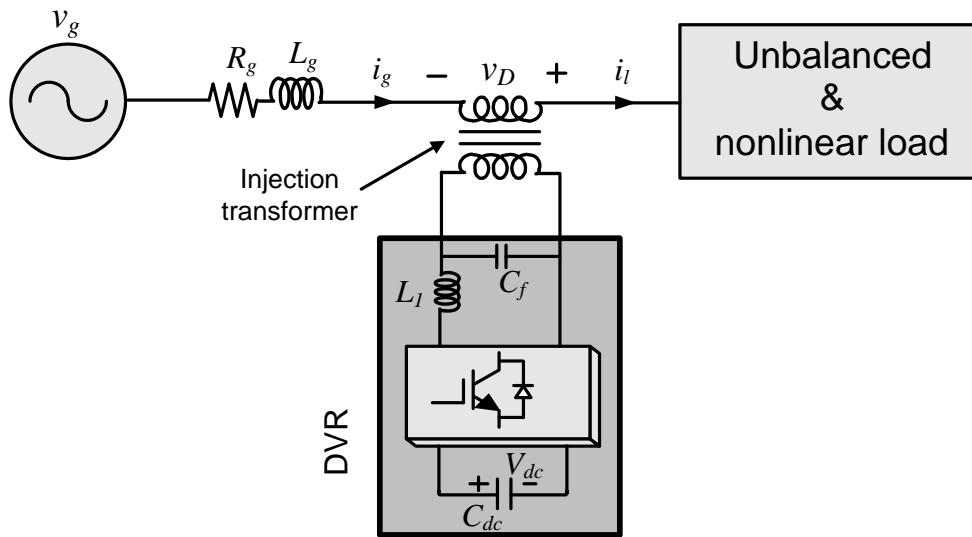


Figure 1.2: Single-line diagram of DVR

1.1.3 Unified Power Quality Conditioner

Unified power quality conditioner (UPQC) is relatively the latest device in the family of the custom power devices [16–20]. The UPQC consists of both DSTATCOM and DVR with a common DC-link as shown in Fig. 1.3. Therefore, the UPQC can simultaneously fulfill the objectives of both DSTATCOM and DVR, i.e., solving both the current and voltage-based quality problems in the distribution network.

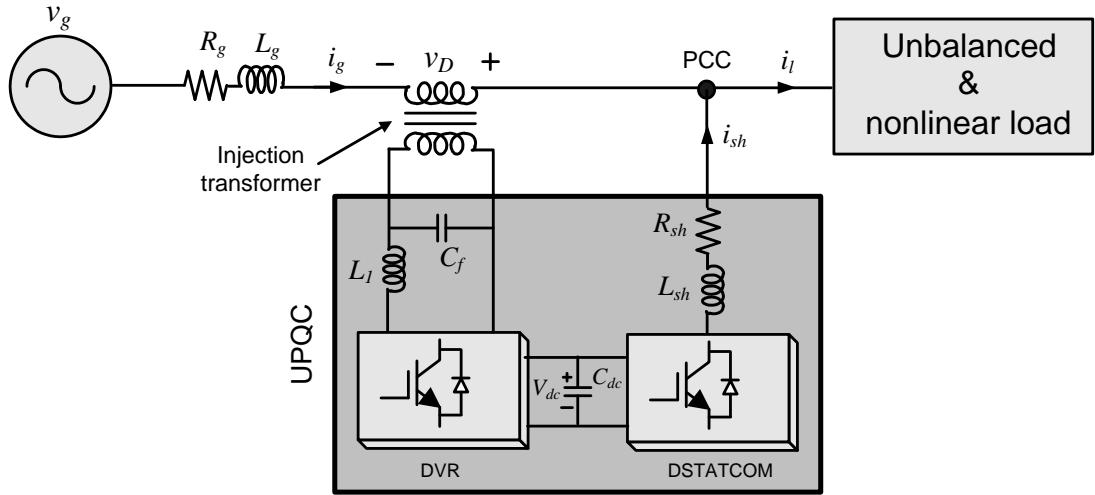


Figure 1.3: Single-line diagram of UPQC

Hybrid power filters, which include passive filters and active filters, are also discussed in the literature [21–23]. These hybrid filters incorporate the advantages of both active and passive filters. Additionally, the passive filters help in decreasing the active filter's rating.

The present work focuses on the use of DSTATCOM and DVR individually in the power distribution network. The problems identified in these areas serve as a motivation for the use of UPQC system as it is a combination of DSTATCOM and DVR. The motivations of this work are described in the following section.

1.2 MOTIVATION

The unified power quality conditioner (UPQC) with back-to-back (BTB) configuration is a flexible custom power device that can improve system performance against both current and voltage related PQ issues. The realization of UPQC, in general any power electronics inverter based system, involves three essential aspects. The first one is the selection of the suitable VSI topology. The second one is the selection of suitable algorithms for generation of reference quantities. The third one is the selection of the suitable controller to realize VSI currents and/or voltages track their respective reference quantities.

The main requirements before selecting the VSI topology can be listed as:

- The DC-link voltage rating is selected such that it has no impact on the ability of power conversion unit to deliver the satisfactory performance.
- The power conversion unit must be compact, efficient and high power density. These features can be achieved by using the power conversion unit with least number of power semiconductor switches and/or with wide-band semiconductor switches.
- The VSI topology must be able to provide path for the flow of zero sequence currents and inject zero sequence voltages into the distribution network.

The series converter of the BTB configured UPQC is almost idle most of the time, since the occurrence of voltage related issues is less often. Thus, the converter utilization is poor with BTB configuration. To improve the converter utilization factor without affecting UPQC's ability to generate required voltages and currents, the reduced switch count converter topologies can be considered.

Various algorithms for generation of reference currents are reported in the literature for DSTATCOM, such as instantaneous reactive power theory [24, 25], generalized

instantaneous reactive power theory [26, 27], Synchronous reference frame theory [28], theory of instantaneous symmetrical components [29] etc. Similarly, various algorithms for generation of reference voltages are reported in the literature for DVR, such as pre-sag, in-phase, energy-optimized compensations, dual instantaneous active-reactive power theory [30–33] etc. The generation of these reference quantities requires approaches for accurate extraction of fundamental frequency positive sequence (FFPS) components and phase angle of grid voltages. Therefore, the extraction of FFPS components based on the operators: second order generalized integrator (SOGI), cascaded delayed signal cancellation (CDSC) and multiple delayed signal cancellation (MDSC) are to be explored and selected the operator with superior characteristics for the UPQC operation.

There are various switching control strategies or controllers to realize the currents and/or voltages of the power conversion unit. Some of these controllers reported in literature are proportional-intergral (PI) and/or proportional-resonant (PR) controller(s) [28, 34–38], hysteresis controller [39–41], model predictive controller [42, 43], sliding mode controller [44–50] etc. The main requirements before selecting the controller can be listed as:

- Control instantaneous currents and/or voltages without amplitude and phase errors.
- Provide high dynamic performance of the power conversion unit.
- Provide limited and constant switching frequency operation to protect the power semiconductor switches and increase the efficiency of the power conversion unit.
- Robust to variations in load and network parameters.
- Simple to implement and low cost.
- The total harmonic distortion (THD) levels should be within the limits specified in the standards.

Considering the above requirements, specifically the insensitive to the model parameter variations, the sliding mode controller is considered for the UPQC system. The sliding mode control scheme can be implemented in any one of the reference frames: dq , $\alpha\beta$ and natural reference frame (abc). Due to availability of generation of reference voltages/currents in abc frame, implementing a controller in the same reference frame would reduce the computational burden and the signal transformation errors. However, the three-phase three-leg or four-leg voltage source converters suffer from the coupling issue in abc frame. The dynamics of each state variable depends on the control inputs of all the legs of the converter. This coupling leads to difficulty in assigning appropriate values to the control inputs using a conventional sliding surface in sliding mode control (SMC) scheme. Therefore, it is necessary to propose a new sliding surface which can provide a per-phase analysis of the system irrespective of the inherent coupling nature in the abc frame.

1.3 OBJECTIVES

The most widely used converter configuration for the UPQC is back-to-back (BTB) converter [20, 51–57]. The BTB configuration contains two VSIs with 16 semiconductor switches in three-phase four-wire (3P4W) distribution system. As described in the previous section, to increase the converter utilization factor, recently proposed dual-output converter (DOC) can be considered for UPQC system [58]. The DOC used in three-phase three-wire (3P3W) distribution system can be called as nine-switch converter (NSC) as it contains only 9 semiconductor switches [59]. The DOC used in 3P4W DG system can be called as twelve-switch converter (TSC) as it contains 12 switches. For both 3P3W and 3P4W DG systems, the required switches in DOC is 25% less than the switches in BTB configuration. The UPQC was designed using NSC for 3P3W DG system in [59, 60] and using TSC for 3P4W DG system in [61]. Nevertheless, the compensation capabilities of UPQC with DOC have been analyzed

only with linear controllers in dq frame. Alternative control techniques can be applied to improve the performance of DOC based UPQC system.

This thesis is focused to develop a new sliding mode control scheme for each four-leg VSI based DSTATCOM and DVR in the natural abc frame. Finally, the developed control scheme is applied to the DOC based UPQC. Based on the literature survey and the motivations, the objectives of the thesis are formulated as given below:

1. To explore and investigate the advanced approaches to extract an accurate FFPS components and phase angle of grid voltages. This is essential for the improved compensation ability of all custom power devices in the DG system.
2. To demonstrate the problems associated with the conventional sliding mode control scheme while developing for four-leg VSI based systems in the natural reference frame.
3. To propose an improved sliding mode control scheme which would provide the control design flexibility in the natural reference frame, incorporate the control of converter neutral-point voltage in addition to control of converter currents and/or voltages and incorporate desired robustness to the parametric variations and uncertainties in the system.
4. Validation of proposed control scheme on four-leg VSI based DSTATCOM and DVR, and DOC based UPQC through simulation and experimental studies.

1.4 ORGANIZATION OF THE THESIS

The reasons for the degradation of power quality, its effects and the PQ standard in the DG system are presented in **Chapter 1**. To address the PQ issues in the DG system, various solutions such as passive filters, active filters or custom power devices and hybrid filters are described. Various custom power devices are briefly discussed as

they are flexible solution for PQ improvement in DG system. Finally, motivations and objectives of the thesis are presented.

Chapter 2 provides an introduction to the conventional or back-to-back UPQC connected to the 3P3W distributed generation (DG) system. It offers a brief overview of the recently proposed nine-switch converter and highlights its advantages and drawbacks compared to the back-to-back topology. The chapter also presents the previously designed nine-switch UPQC, including its control methods and associated challenges. Furthermore, the chapter delves into the discussion of control techniques that are being considered as replacements for the current linear control methods used in the nine-switch UPQC. These alternative control techniques are explored in order to overcome the limitations of the existing linear control methods.

Chapter 3 presents different operators, such as the second-order generalized integrator (SOGI), cascaded delayed signal cancellation (CDSC), and multiple delayed signal cancellation (MDSC). These operators are utilized to extract the fundamental positive sequence components from signals that are distorted and unbalanced. Independently, these operators are cascaded to the synchronous reference frame phase-locked loop (SRF-PLL) to precisely determine the phase angle of the grid voltages. Through simulation studies, the performance of PLLs employing these three operators is thoroughly analyzed.

Chapter 4 introduces a novel sliding mode control (SMC) approach for the four-leg distribution static compensator (DSTATCOM). The proposed control scheme utilizes a new sliding surface, allowing for simultaneous control of both compensator currents and the converter neutral-point voltage (NPV). The inclusion of NPV control is crucial for power quality conditioners based on dual-output converters. To assess the effectiveness of the proposed control scheme, extensive simulation and experimental studies are conducted on the four-leg DSTATCOM system.

In **Chapter 5**, a new sliding mode control (SMC) approach is introduced for the four-leg dynamic voltage restorer (DVR). The proposed control scheme incorporates a novel sliding surface, enabling concurrent control of compensator voltages and the converter neutral-point voltage (NPV). This inclusion of NPV control is particularly significant for power quality conditioners utilizing dual-output converters. To evaluate the effectiveness of the proposed control scheme, comprehensive simulation and experimental studies are carried out on the four-leg DVR system.

Chapter 6 addresses the extension of the control schemes proposed in Chapter 4 for DSTATCOM and Chapter 5 for DVR to dual-output converter (DOC) based unified power quality conditioner (UPQC) applications. The proposed control scheme allows for the simultaneous control of both converter NPVs and compensator voltages and currents. By incorporating NPV control into the controller, the proposed scheme can be implemented directly in the natural frame. A comprehensive model of the proposed control scheme is developed for the DOC-based left shunt UPQC (UPQC-L) system. A novel reference generation approach has also been proposed for the neutral-point voltages in the UPQC-L application. To validate the effectiveness of the proposed scheme, extensive simulation studies are conducted on the DOC-based UPQC-L system.

In **Chapter 7**, important conclusions derived from the research work are presented. These conclusions encapsulate the key findings and outcomes of the study. Additionally, suggestions for future directions and potential areas for further research are outlined, providing a roadmap for future work in the field. Furthermore, the **Appendix A** provides a simplified explanation of the control schemes proposed for both DSTATCOM and DVR systems, while **Appendix B** outlines the motivation behind utilizing a four-leg converter for DVR application due to the limitations of three-wire DVR in distribution systems.

CHAPTER 2

THE TOPOLOGICAL CHARACTERISTICS OF DUAL-OUTPUT VOLTAGE SOURCE CONVERTER

2.1 INTRODUCTION

Various power quality problems and the mitigating devices have been introduced in the previous chapter. This chapter outlines the UPQC with conventional converter and dual-output converter. In addition, the performance characteristics of dual-output converter and its control are presented.

2.2 CONVENTIONAL UPQC

Unified power quality conditioner (UPQC) can be classified in many ways based on converter topology, supply system/DG system, system configuration and voltage sag compensation. A more detailed description of different classification methods is summarized in [51]. In this section, the conventional or back-to-back UPQC connected to 3P4W DG system is described and the single-line representation of two possibly configured UPQC are shown in Figs. 2.1 and 2.2.

The UPQC is a combination of shunt (DSTATCOM) and series (DVR) compensators that share a common self-supporting DC-link [16, 62]. The DC-link voltage is regulated to a reference value by controlling the active power flow through the shunt compensator. The DSTATCOM or shunt converter is commonly utilized in current control mode (CCM), while the DVR or series converter is commonly operated in voltage control mode (VCM). However, it is also feasible to perform the vice versa operation [63]. The

shunt compensator is realized by connecting a voltage source inverter (VSI) in parallel with the load and using an interfacing passive filter. In CCM, the shunt VSI is controlled as a means to address current power quality (PQ) issues in the DG system, making it equivalent to a controlled current source. The shunt VSI can also be operated in VCM to regulate the load voltage [64, 65]. There are three common types of interfacing passive filters, namely L filter, LC filter, and LCL filter, which are utilized to mitigate high-frequency current switching harmonics. Throughout this thesis, the L filter is adopted as the preferred configuration.

The series compensator is implemented by connecting a voltage source inverter (VSI) in series with the feeder. This connection is achieved through three single-phase injection transformers and a low-pass filter. The series VSI is controlled in VCM to solve the voltage related PQ issues in the DG system. The series compensator can therefore be thought of as a controlled voltage source. Alternatively, the series VSI can also operate in current control mode (CCM) to regulate the grid/source current [66–68]. The injection transformers serve the purpose of isolating the converter’s DC bus from the distribution network. Moreover, the low-pass filter effectively mitigates the switching frequency harmonics generated by the series VSI.

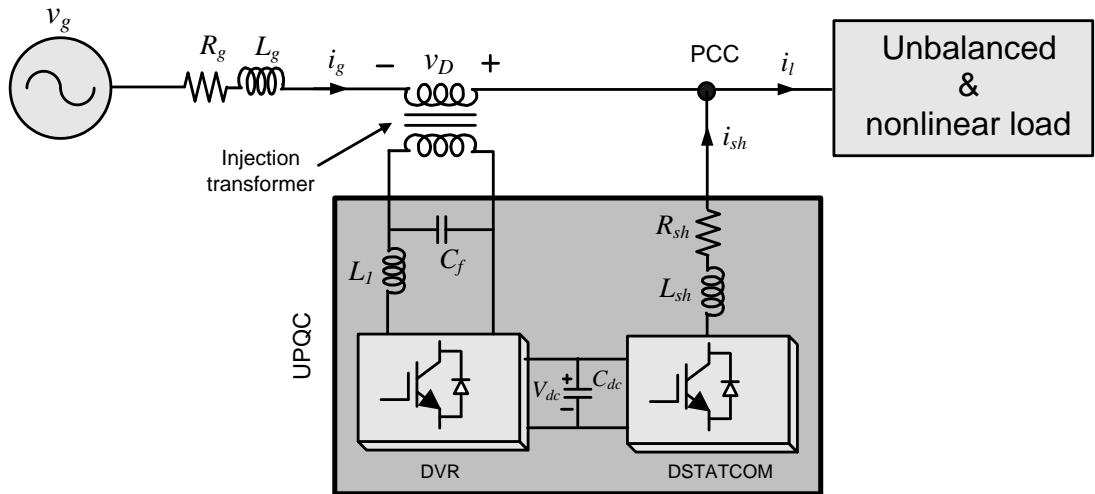


Figure 2.1: Single-line diagram of UPQC-R configuration

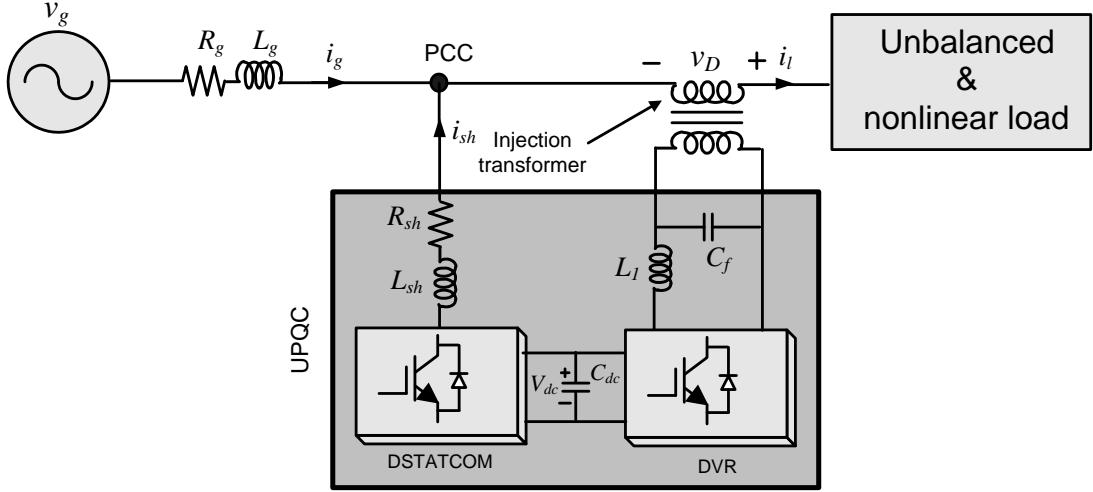


Figure 2.2: Single-line diagram of UPQC-L configuration

The flow of zero sequence current in the neutral wire is quite common in the 3P4W DG system. The VSI interfaced with such 3P4W systems must provide a path for the flow of zero-sequence current. Thus, the four-leg VSI topology is used for shunt compensator. The converter topology of series compensator can be either three-leg VSI or four-leg VSI based on the UPQC configuration. In [2, 51], two possible configurations of UPQC at the PCC have been discussed. One is the right shunt UPQC (UPQC-R), in which the shunt compensator is connected to the load side and the series compensator to the supply side, as shown in Fig. 2.1. The second one is the left shunt UPQC (UPQC-L), in which the shunt compensator is connected to the supply side and the series compensator to the load side, as shown in Fig. 2.2. In the UPQC-R configuration, the shunt VSI carries all the zero-sequence load current, while the series VSI does not carry any zero-sequence load current, making it possible to use a three-leg VSI for the series compensator. In contrast, there is a possibility of zero sequence current flow through series VSI in UPQC-L configuration and hence four-leg VSI has to be used in UPQC-L. Thus, UPQC-R requires less number of semiconductor switches compared to UPQC-L.

2.3 DUAL-OUTPUT CONVERTER

Currently, approximately 30% of all the electric power generated uses power electronics somewhere between the point of generation and distribution. Some analysts project that 80% of the energy will flow through power electronics in the near future, but that would require cost reductions in power electronics and power conversion systems. In line with this, recent research has been focused on high power density converter topologies. The high power density can be achieved by using wide-band semiconductor switches and/or reduced number of switches in a converter topology. This thesis focuses on the reduced switch count converter topologies for UPQC system. One of them is the dual-output converter (DOC). It is also called as nine-switch converter (NSC) in 3P3W systems as it contains only nine semiconductor switches. The NSC was introduced in [58] for the motor drive applications. In this section, a brief overview of the dual-output converter is presented including its topology characteristics and modes of operation.

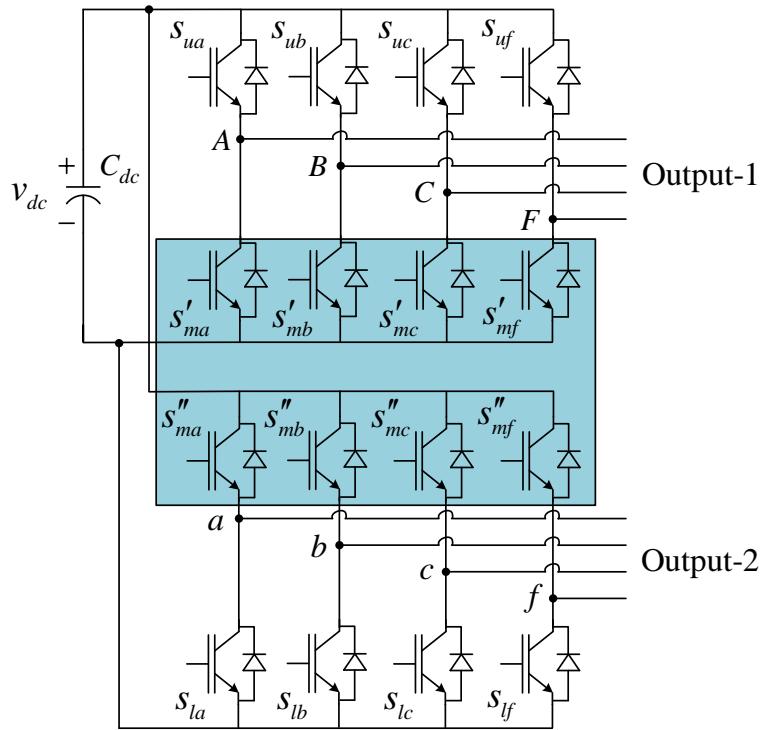


Figure 2.3: Back-to-back (BTB) converter configuration

The DOC is similar to conventional back-to-back (BTB) configuration in which bottom

switches of one converter and top switches of other converter combine to form middle switches of DOC. As a result of this new arrangement, the total number of switches are reduced from sixteen to twelve with respect to its counterpart. Moreover, both the BTB topology and the DOC are able to generate and control two sets of three-phase signals with different amplitude, frequency and phase shift. The DOC experiences its own structural limitations, however it is usually the case for converters with a reduced number of semiconductor switching devices. The structure of BTB topology and DOC are shown in Figs. 2.3 and 2.4, respectively. The DOC is actually built with a single capacitor at DC-link. However, the split-capacitor based DC-bus is shown in Fig. 2.4 to understand the switching states of DOC described below.

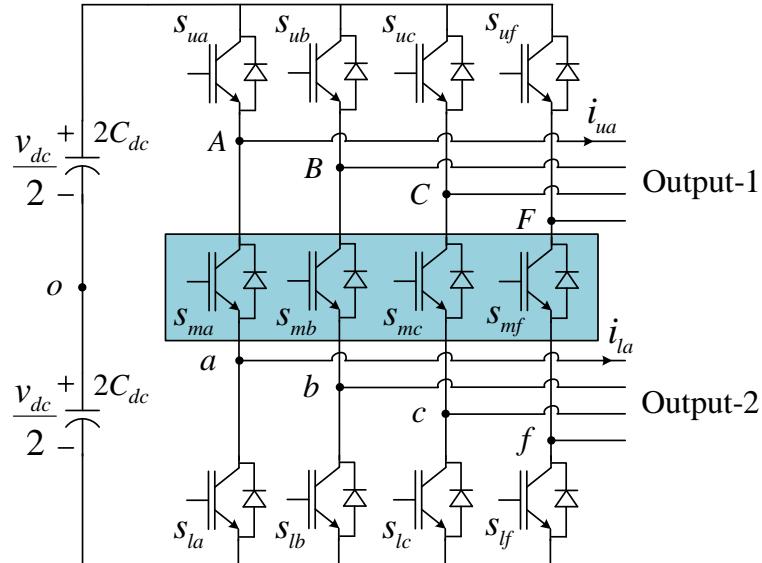


Figure 2.4: Dual-output converter (DOC) configuration

Consider phase - a leg of the converter shown in Fig. 2.4. There are eight possible switching states as it has three switches in a leg. In Table 2.1, the pole voltages (v_{Ao} , v_{ao}) are tabulated against each switching state for all possible directions of the currents. Among eight states, only the first three states listed in Table 2.1 are having a unique pole voltage irrespective of current directions and thus these three states are valid. From these valid states, it is observed that the state of middle switch can be generated using either logical NAND or XOR operation of upper and lower switch states.

Table 2.1: Possible switching states of dual output converter

			Direction				
S_{ua}	S_{ma}	S_{la}	v_{Ao}	v_{ao}	i_{ua}	i_{la}	$i_{ua} + i_{la}$
0	1	1	—	—	A	A	A
1	1	0	+	+	A	A	A
1	0	1	+	—	A	A	A
<hr/>			<hr/>			<hr/>	
0	1	0	+	+	A	A	N
			—	—	A	A	P
<hr/>			<hr/>			<hr/>	
			+	+	A	N	N
0	0	0	—	—	P	A	P
			+	—	N	P	A
<hr/>			<hr/>			<hr/>	
0	0	1	—	—	P	A	A
			+	—	N	A	A
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1	0	0	+	+	A	N	A
			+	—	A	P	A
<hr/>			<hr/>			<hr/>	
			+	+	P	P	P
1	1	1	—	—	N	A	A
			+	—	P	N	A

‘+’ : $\frac{V_{dc}}{2}$; ‘-’ : $-\frac{V_{dc}}{2}$; P : Positive; N : Negative; A : Any

In sinusoidal pulswidth modulation (SPWM), the elimination of invalid switching states is achieved by introducing offsets to the modulating signals of both the upper output (output-1) and lower output (output-2). This adjustment ensures that the upper signal is consistently higher than the lower signal, preventing the occurrence of undesirable switching states [58] as shown in Fig. 2.5. The state of upper switch (S_{ua}) is determined by comparing the upper output modulating signal (v_{Ao}^*) with the carrier signal (v_c). If $v_{Ao}^* > v_c$, S_{ua} is set to high, indicating that the top switch should be turned on. Similarly, the state of bottom switch (S_{la}) is determined by comparing the lower output modulating signal (v_{ao}^*) with the carrier signal (v_c). If $v_{ao}^* < v_c$, S_{la} is set to high, indicating that the bottom switch should be turned on. The state of the middle switch (S_{ma}) is determined by applying a logical XOR operation to the states of the lower and upper switches. By using XOR, the invalid switching state 000 is observed when $v_{Ao}^* < v_{ao}^*$. If the logical XOR was replaced with a NAND operation, then the invalid switching state 010 would be noticed for $v_{Ao}^* < v_{ao}^*$. According to Table 2.1, the state 000 has three possible voltage outputs $\{(+, +), (-, -), (+, -)\}$, whereas the state 010 has only two voltage possibilities $\{(+, +), (-, -)\}$. Therefore, NAND operation is

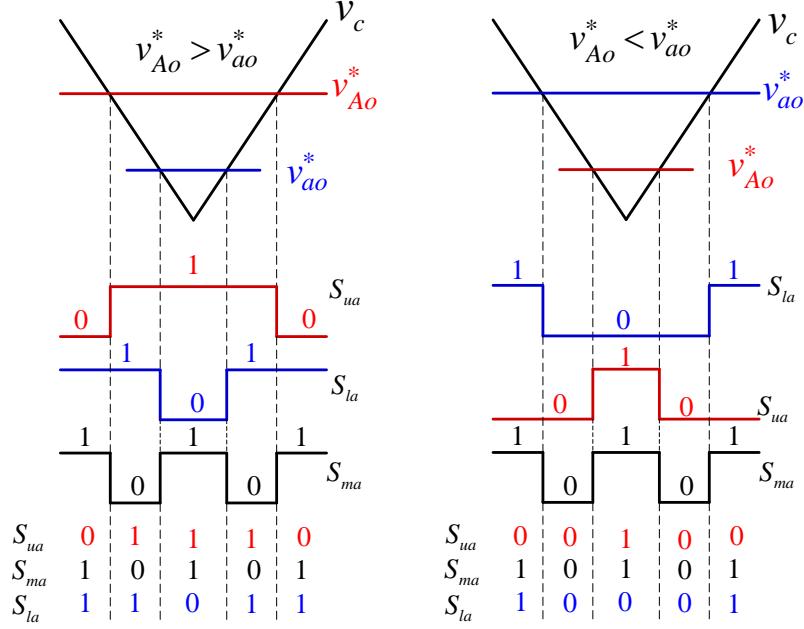


Figure 2.5: Switching diagram of SPWM for DOC

preferred to determine the state of the middle switch as it simplifies converter control by having the state with least voltage output possibilities.

In sliding mode (SM) PWM, the states of the upper and lower switches are determined based on the position of structured sliding surface trajectories. Let's consider a single-phase DOC designed for current control of two independent loads, as shown in Fig. 2.6(a) [46]. The filter inductance, load voltage and load neutral of upper output are denoted as L_u , v_u , and n , respectively. Similarly, the filter inductance, load voltage and load neutral of lower output are denoted as L_l , v_l , and n' , respectively. The sliding surface is structured as $\sigma_A = i_{ua} - i_{ua}^* = 0$ for the upper output and $\sigma_a = i_{la} - i_{la}^* = 0$ for the lower output. Here, i_{ua} and i_{ua}^* represent the actual and reference currents of the upper output, respectively, while i_{la} and i_{la}^* denote the actual and reference currents of the lower output, respectively. All these currents are associated with phase- a of their respective outputs. The switching logics are selected in a way that the sliding variable should be maintained at zero. To achieve this, the top switch is turned ‘OFF’ ($S_{ua} = 0$) when the trajectory of upper sliding variable (σ_A) reaches its upper hysteresis band ($+h_u$). Conversely, when the trajectory of σ_A reaches the lower band ($-h_u$), the top

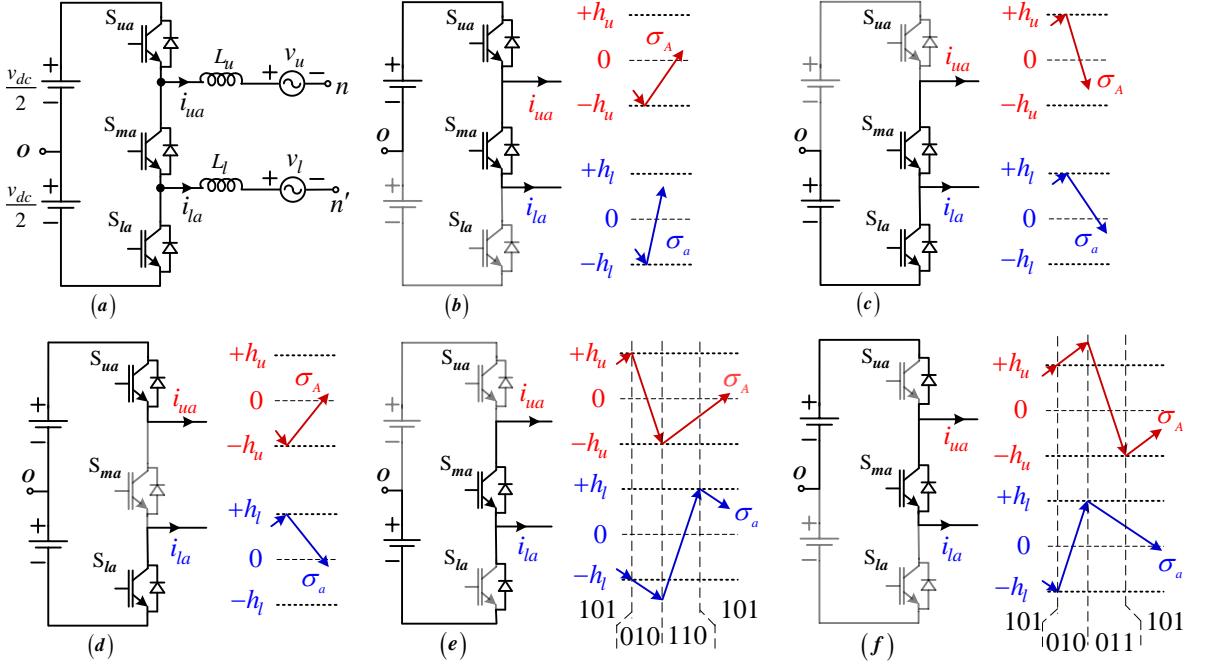


Figure 2.6: (a) 1- ϕ half bridge DOC; switching states: (b) 110, (c) 011, (d) 101, (e) 010 resembles as 011 due to net positive current, (f) 010 resembles as 110 due to net negative current

switch is turned ‘ON’ ($S_{ua} = 1$). Similarly, when the trajectory of the lower sliding variable (σ_a) reaches its upper band ($+h_l$), the bottom switch is turned ‘ON’ ($S_{la} = 1$). Conversely, when the trajectory of σ_a reaches the lower band ($-h_l$), the bottom switch is turned ‘OFF’ ($S_{la} = 0$).

Let’s analyze the operation of SM-PWM using four different instants, as depicted in Fig. 2.6(b)-(f). The first instant is considered when both sliding variables reach their lower hysteresis bands, as shown in Fig. 2.6(b). According to the discussed switching logics, the switching state 110 is applied. In this state, both pole voltages (v_{Ao} and v_{ao}) are set to $+\frac{v_{dc}}{2}$, causing the sliding variables to increase. This modulation helps to keep the sliding variables within their respective bands. Similar scenarios can be observed when σ_A and σ_a reach their upper hysteresis bands, as shown in Fig. 2.6(c), or when σ_A reaches its lower band and σ_a reaches its upper band, as shown in Fig. 2.6(d). According to the switching logics, the switching state 011 and 101 are applied, respectively.

In the last instant, σ_A reaches its upper band and σ_a reaches its lower band, as shown in Fig. 2.6(e)-(f). According to the discussed switching logics, the invalid switching state 010 is applied. When the net load current ($i_{ua} + i_{la}$) is positive, the freewheeling diode of bottom switch conducts and it resembles the 011 switching state, as shown in Fig. 2.6(e). In this state, both pole voltages are set to $-\frac{v_{dc}}{2}$, causing the sliding variables to decrease. As a result, σ_A stays within its band but σ_a deviates from its lower band and continues to deviate until σ_A reaches its lower band. A similar case is observed when the net load current is negative. In this situation, the freewheeling diode of top switch conducts and it resembles 110 switching state, as shown in Fig. 2.6(f). Both pole voltages are set to $+\frac{v_{dc}}{2}$, causing the sliding variables to increase. Consequently, σ_a stays within its band but σ_A deviates from its upper band and continues to deviate until σ_a reaches its upper band. In both the cases, to minimize the magnitude of sliding variables deviating from their bands, it is necessary to satisfy the below condition:

$$\dot{\sigma}_a > \dot{\sigma}_A. \quad (2.1)$$

Over a switching period, the reference currents are assumed to remain constant, considering a switching frequency that is much higher than the fundamental frequency. Therefore (2.1) can be rewritten as follows:

$$\begin{aligned} \dot{i}_{la} - \dot{i}_{la}^* &> \dot{i}_{ua} - \dot{i}_{ua}^*, \\ \Rightarrow \quad \dot{i}_{la} &> \dot{i}_{ua}, \\ \Rightarrow \quad \frac{v_{ao} - v_l - v_{n'o}}{L_l} &> \frac{v_{Ao} - v_u - v_{no}}{L_u}. \end{aligned} \quad (2.2)$$

The pole voltages (v_{Ao} and v_{ao}) are equal in both cases of the last instant. Assuming equal filter inductances, (2.2) can be updated as follows:

$$\begin{aligned} v_u + v_{no} &> v_l + v_{n'o}, \\ \Rightarrow v_{Ao}^* &> v_{ao}^*. \end{aligned} \quad (2.3)$$

It says that by consistently maintaining upper output pole voltage higher than the lower output pole voltage, the sliding variables can converge to their hysteresis bands within a finite time, even if the deviations occur. This condition is similar to that of SPWM, where it is necessary to avoid the invalid switching state. However, achieving this condition in SMPWM is not as straightforward as in SPWM. In SMPWM, it can be realized by using the external control degree of freedoms, i.e., common mode voltages v_{no} and $v_{n'o}$. These additional control parameters provide the means to ensure that the upper output pole voltage remains consistently higher than the lower output pole voltage, facilitating the convergence of the sliding variables to their respective hysteresis bands.

2.4 DUAL-OUTPUT CONVERTER BASED UPQC

The dual-output converter has been widely used in various applications, as reported in [46, 69–74]. However, many of these applications involve replacing the back-to-back converter with two shunt VSCs, which does not fully utilize the potential of this new topology. This issue was discussed in [75] and [59]. As a solution, it has been proposed to use the dual-output converter for replacing back-to-back converter in "series-shunt" systems such as UPQC-L. This design concept is illustrated in Fig. 2.7 for 3P3W distribution system.

Fig. 2.7 depicts the nine-switch UPQC configuration with the left shunt, where a single DC source is replaced with split-source for a better understanding of converter dynamics. The shunt and series passive filters were represented by L_{sh} and parallel L_1C_f , respectively. The switching mechanism of the nine-switch converter was explained in Section 2.3. The shunt and series terminals function similarly to those of a conventional UPQC, as mentioned in Section 2.2. However replacing BTB topology with the NSC, novel operating principles of the shunt and series terminals were introduced for normal and 20% sag conditions in [59].

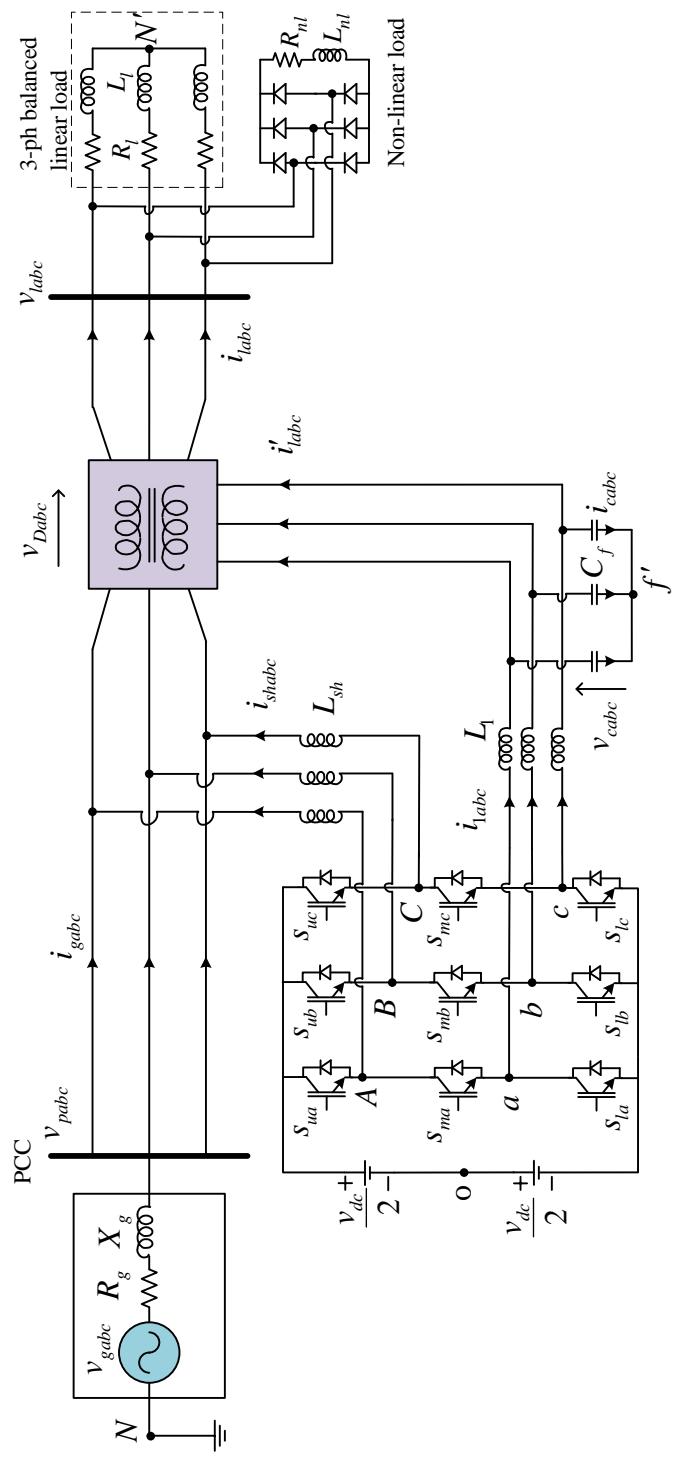


Figure 2.7: Nine-switch UPQC

The division of carrier range between the shunt and series terminals during normal operation and voltage sag conditions, as discussed in [59], is depicted in Fig. 2.8. In this scenario, the placement of upper and lower modulating references are for the shunt and series terminals, respectively. Under the normal voltage operating condition, the maximum existence of harmonics in supply voltage is about 5%. Thus, the carrier range is divided with a much wider vertical range h_1 for controlling the shunt terminal and a narrower h_2 for controlling the series terminal to compensate 5% harmonics.

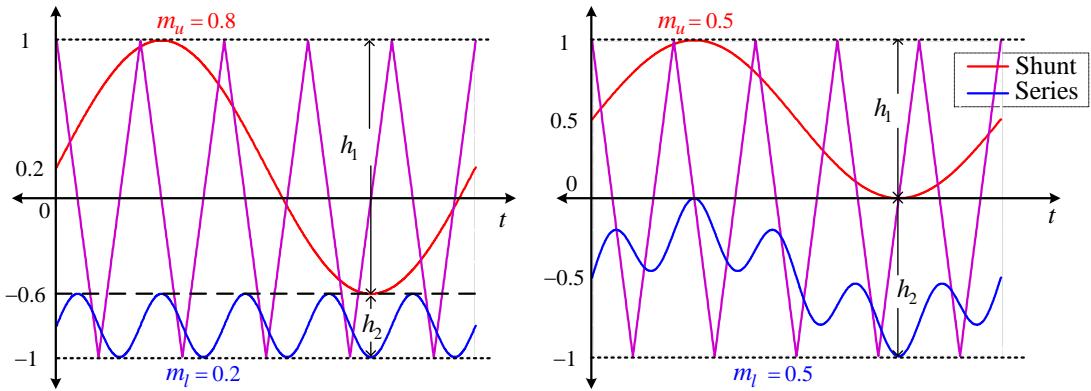


Figure 2.8: Modulating references during normal (left) and voltage sag (right) modes

Under voltage sag condition, the shunt terminal at the point of common coupling (PCC) experiences a reduced voltage. This reduction in voltage requires a corresponding reduction in h_1 , thereby freeing up more carrier space for the series reference to vary within, ensuring that interference between the shunt and series references is avoided.

If this carrier division approach is applied to UPQC-R configuration, then the carrier range of shunt terminal is fixed at $[-1,1]$ assuming series compensator functions normally and its terminal voltage is always at 1 pu. During severe sag conditions, such as a sag of 1 pu, the carrier range of series terminal is also $[-1,1]$. As a result, the DC-link voltage required for the UPQC-R configuration is twice as high as that required for the UPQC-L configuration. When applying the same approach to the UPQC-L configuration for compensating voltage swells, the shunt reference overlaps with the series reference at normal DC-link voltage. Consequently, a higher DC-link voltage is

required to ensure that the references do not interfere with each other.

Moreover, the appropriate control and modulation schemes developed for the nine-switch UPQC are presented in [59]. The 120° -discontinuous modulation technique is implemented for both the shunt and series terminals, and the control schemes with linear controllers are described for both terminals separately according to their main functions. The synchronous reference frame (SRF) theory was used for the generation of reference currents and voltages.

The design of the shunt terminal controller focuses on load current harmonic compensation, reactive power injection, and maintaining the DC-link voltage at the desired level. The sensed load currents are first transformed into d and q components by Park's transformation. Next, the harmonic components of load currents are obtained by passing the d -axis load current (i_d) through high-pass filter (HPF). This filtered signal of d -axis harmonics is added with a d -axis control reference of a DC-link proportional-integral (PI) regulator. The regulator compensates the losses and maintains the DC-link voltage constant. The q component of load current (i_q) contributes to the load reactive power compensation. Finally, the generated d and q reference components are transformed back to the abc natural frame, and the error between the shunt reference and measured currents is sent to a proportional-resonant (PR) controller that generates switching pulses. A block diagram of this control technique is shown in Fig. 2.9.

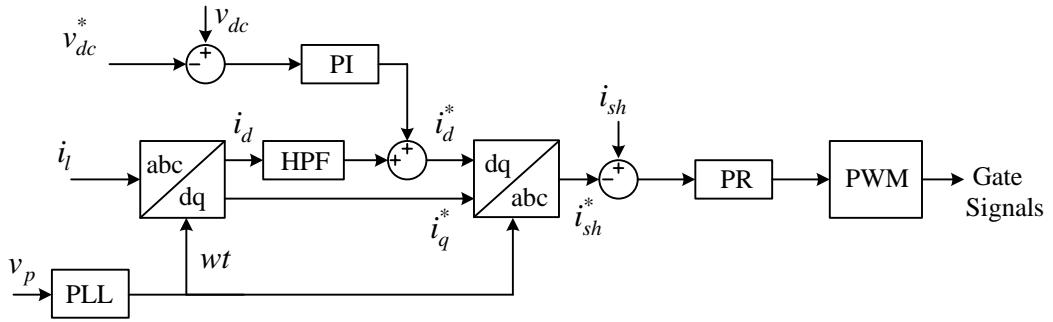


Figure 2.9: Conventional control circuit of shunt compensator [59]

The control scheme for the series terminal is depicted in Fig. 2.10, using a multi-loop control approach. Its primary functions are to compensate voltage harmonics in the utility grid or DG system and to maintain load voltage at the desired level during grid voltage variations. Selective harmonic compensation was implemented in the subsystem for voltage harmonic compensation, following the method described in [76]. The second part of the series terminal control system, i.e., the feed-forward PI regulator was designed with two degrees of freedom for detecting sags and accounting for voltage drops across the inductive components, including series transformers and inductors.

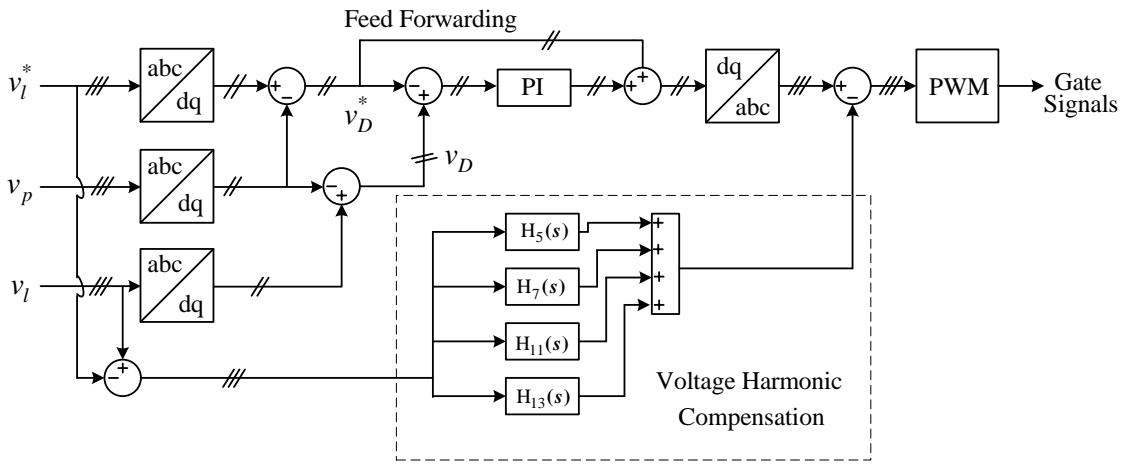


Figure 2.10: Conventional control circuit of series compensator [59]

The shunt and series terminal controllers were designed using linear control methods, which can cause some issues. Firstly, the reference waveforms for both terminals were generated using the SRF theory with the complicated Park's transformation. Secondly, to mitigate current/voltage harmonics, the PR controller needs to have cascaded resonant blocks that must be tuned for each desired harmonic frequency, making the controller complex and able to mitigate only the most prominent harmonics in the frequency spectrum [77]. Thirdly, the feed-forward path to compensate voltage drops across reactive elements requires the series terminal controller to be implemented in a multi-loop configuration. Also, due to the poor low-order harmonic mitigation capability of the PI controller, multiple resonant regulators were placed, resulting in slight transient sluggishness to maintain stability [59]. As the system order increases,

tuning of the PI and PR controllers becomes more complicated.

2.5 CONTROL OF UPQC

Generating reference quantities and realizing them using voltage source inverters (VSIs) are two crucial tasks in the control of any active power filter. This section presents various control algorithms for generating reference quantities and techniques for controlling the switching of VSIs.

2.5.1 Generation of Reference Quantities for DSTATCOM

The choice of a control strategy for generating reference quantities significantly impacts the compensation performance of an active filter. In the literature, several power theories have been presented for reference generation [24–27, 29, 78–86]. Among these, the instantaneous reactive power theory [24–26], generalized instantaneous reactive power theory [27], synchronous reference theory [84], and instantaneous symmetrical components theory [29, 82, 83] are commonly utilized. In this section, a concise overview of these theories are provided.

Instantaneous Reactive Power Theory [87]

"The Instantaneous Reactive Power Theory was initially proposed by Akagi H., Kanazawa Y., and Nabae A. in 1983-84 [24]. The primary objective of this theory is to establish a mathematical framework for calculating instantaneous reactive power, enabling the compensation of reactive power not only in steady-state but also during transient conditions. This theory is commonly employed to determine the reference current for a shunt active filter. It utilizes the instantaneous values of voltages and currents to derive the compensating quantities. To facilitate this process, the abc phase voltages and currents are transformed to the stationary $\alpha - \beta$ axis using the Clarke transformation, which is depicted in Fig. 2.11.

The instantaneous abc phase voltages are transformed into $\alpha-\beta-0$ coordinates to include

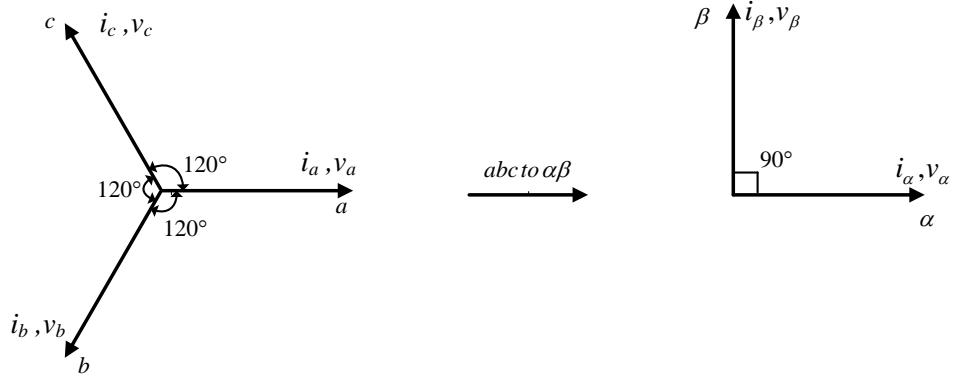


Figure 2.11: abc to $\alpha\beta$ transformation

the zero sequence components, as given below.

$$\begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}; \begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (2.4)$$

The instantaneous real power is defined as the product of the instantaneous voltage and the instantaneous current, both aligned along the same axis.

$$p = v_\alpha i_\alpha + v_\beta i_\beta \quad (2.5)$$

In abc coordinates it is given by,

$$p = v_a i_a + v_b i_b + v_c i_c.$$

The instantaneous reactive power is defined as the cross product of the instantaneous voltage along one axis and the instantaneous current along its quadrature axis.

$$q = \vec{v}_\alpha \times \vec{i}_\beta + \vec{v}_\beta \times \vec{i}_\alpha \quad (2.6)$$

$$q = v_\alpha i_\beta - v_\beta i_\alpha \quad (2.7)$$

Using (2.4) and (2.6), the expression for the same in *abc* coordinates is given below.

$$q = -\frac{1}{\sqrt{3}}[(v_a - v_b)i_c + (v_b - v_c)i_a + (v_c - v_a)i_b] \quad (2.8)$$

$$q = -\frac{1}{\sqrt{3}}[v_{ab}i_c + v_{bc}i_a + v_{ca}i_b] \quad (2.9)$$

The instantaneous zero sequence power is defined as $p_o = v_0 i_0$. The instantaneous powers in $\alpha\beta0$ - coordinates can be represented in the following matrix form.

$$\begin{bmatrix} p_0 \\ p \\ q \end{bmatrix} = \begin{bmatrix} v_0 & 0 & 0 \\ 0 & v_\alpha & v_\beta \\ 0 & -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} \quad (2.10)$$

It can be rearranged in the following form.

$$\begin{aligned} \begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} &= \begin{bmatrix} v_0 & 0 & 0 \\ 0 & v_\alpha & v_\beta \\ 0 & -v_\beta & v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} p_0 \\ p \\ q \end{bmatrix} \\ &= \frac{1}{v_0(v_\alpha^2 + v_\beta^2)} \begin{bmatrix} v_\alpha^2 + v_\beta^2 & 0 & 0 \\ 0 & v_0 v_\alpha & -v_0 v_\beta \\ 0 & v_0 v_\beta & v_0 v_\alpha \end{bmatrix} \begin{bmatrix} p_0 \\ p \\ q \end{bmatrix} \quad (2.11) \\ &= \begin{bmatrix} i_{0p} \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} 0 \\ i_{\alpha p} \\ i_{\beta p} \end{bmatrix} + \begin{bmatrix} 0 \\ i_{\alpha q} \\ i_{\beta q} \end{bmatrix} \end{aligned}$$

The various terms in the above equation are defined as follows.

Zero sequence current, $i_{0p} = p_0/v_0$,

α - axis instantaneous active current, $i_{\alpha p} = v_\alpha p/(v_\alpha^2 + v_\beta^2)$,

α - axis instantaneous reactive current, $i_{\alpha q} = -v_\beta q/(v_\alpha^2 + v_\beta^2)$,

β - axis instantaneous active current, $i_{\beta p} = v_{\beta}p/(v_{\alpha}^2 + v_{\beta}^2)$,

β - axis instantaneous reactive current, $i_{\beta q} = v_{\alpha}q/(v_{\alpha}^2 + v_{\beta}^2)$.

Using (2.11), the components of the filter current in terms of its powers and voltages can be expressed as shown below.

$$\begin{bmatrix} i_{f0} \\ i_{f\alpha} \\ i_{f\beta} \end{bmatrix} = \frac{1}{v_0(v_{\alpha}^2 + v_{\beta}^2)} \begin{bmatrix} v_{\alpha}^2 + v_{\beta}^2 & 0 & 0 \\ 0 & v_0v_{\alpha} & -v_0v_{\beta} \\ 0 & v_0v_{\beta} & v_0v_{\alpha} \end{bmatrix} \begin{bmatrix} p_{f0} \\ p_f \\ q_f \end{bmatrix} \quad (2.12)$$

Where, i_{f0} , $i_{f\alpha}$ and $i_{f\beta}$ represent the reference filter currents, while p_{f0} , p_f and q_f correspond to the powers that need to be compensated. The instantaneous real and reactive powers of the load are divided as follows.

$p_L = \bar{p}_L + \tilde{p}_L + p_{L0}$ and $q_L = \bar{q}_L + \tilde{q}_L$, where \bar{p}_L and \tilde{p}_L are the DC and AC components of the instantaneous real power, p_{L0} is the zero-sequence power and \bar{q}_L and \tilde{q}_L are the DC and AC components of the instantaneous reactive power. Here the subscript 'L' represents load in the system.

By selecting $p_f = \tilde{p}_L$, $p_{f0} = p_{L0}$ and $q_f = \bar{q}_L + \tilde{q}_L$, it becomes possible to compensate for the instantaneous harmonic active current, instantaneous zero-sequence current, instantaneous fundamental reactive current, and instantaneous harmonic reactive current. The compensation of instantaneous reactive currents leads to a unity displacement factor in both steady state and transient state. The zero sequence power is supplied to the load from the source through the compensator in order to maintain balanced source currents."

Modified p - q Theory [88, 89]

"In the modified p - q theory, the calculation of instantaneous real power and reactive power involves considering a three-dimensional voltage vector $v_{\alpha\beta 0}$ and a current vector

$i_{\alpha\beta 0}$. In this approach, the instantaneous real power includes the zero sequence power as well.

$$p = v_{\alpha\beta 0} \cdot i_{\alpha\beta 0} = v_\alpha i_\alpha + v_\beta i_\beta + v_0 i_0 \quad (2.13)$$

$$q = v_{\alpha\beta 0} \times i_{\alpha\beta 0} = \begin{bmatrix} q_\alpha \\ q_\beta \\ q_0 \end{bmatrix} = \begin{bmatrix} v_\beta & v_0 \\ i_\beta & i_0 \\ v_0 & v_\alpha \\ i_0 & i_\alpha \\ v_\alpha & v_\beta \\ i_\alpha & i_\beta \end{bmatrix} \quad (2.14)$$

In this case, the instantaneous reactive power is divided into three components: q_α , q_β , and q_0 . By expressing the above power definitions in matrix form, the following equation is derived.

$$\begin{bmatrix} p \\ q_\alpha \\ q_\beta \\ q_0 \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta & v_0 \\ 0 & -v_0 & v_\beta \\ v_0 & 0 & -v_\alpha \\ -v_\beta & v_\alpha & 0 \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} \quad (2.15)$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2 + v_0^2} \begin{bmatrix} v_\alpha & 0 & v_0 & -v_\beta \\ v_\beta & -v_0 & 0 & v_\alpha \\ v_0 & v_\beta & -v_\alpha & 0 \end{bmatrix} \begin{bmatrix} p \\ q_\alpha \\ q_\beta \\ q_0 \end{bmatrix} \quad (2.16)$$

Instantaneous zero sequence active current is defined as given in (2.17).

$$i_{0p} = \frac{v_0}{v_\alpha^2 + v_\beta^2 + v_0^2} p \quad (2.17)$$

Instantaneous zero sequence reactive current is defined as below.

$$i_{0q} = \frac{v_\beta}{v_\alpha^2 + v_\beta^2 + v_0^2} q_\alpha - \frac{v_\alpha}{v_\alpha^2 + v_\beta^2 + v_0^2} q_\beta \quad (2.18)$$

Instantaneous active current on the α axis is given by,

$$i_{\alpha p} = \frac{v_\alpha}{v_\alpha^2 + v_\beta^2 + v_0^2} p. \quad (2.19)$$

Instantaneous reactive current on the α axis is given below.

$$i_{\alpha q} = \frac{v_0}{v_\alpha^2 + v_\beta^2 + v_0^2} q_\beta - \frac{v_\beta}{v_\alpha^2 + v_\beta^2 + v_0^2} q_0 \quad (2.20)$$

Instantaneous active current on the β axis is given by,

$$i_{\beta p} = \frac{v_\beta}{v_\alpha^2 + v_\beta^2 + v_0^2} p. \quad (2.21)$$

Instantaneous reactive current on the β axis is given below.

$$i_{\beta q} = \frac{v_\alpha}{v_\alpha^2 + v_\beta^2 + v_0^2} q_0 - \frac{v_0}{v_\alpha^2 + v_\beta^2 + v_0^2} q_\alpha \quad (2.22)$$

The reference currents can be derived from the following equation.

$$\begin{bmatrix} i_{f\alpha} \\ i_{f\beta} \\ i_{f0} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2 + v_0^2} \begin{bmatrix} v_\alpha & 0 & v_0 & -v_\beta \\ v_\beta & -v_0 & 0 & v_\alpha \\ v_0 & v_\beta & -v_\alpha & 0 \end{bmatrix} \begin{bmatrix} p_f \\ q_{f\alpha} \\ q_{f\beta} \\ q_{f0} \end{bmatrix} \quad (2.23)$$

By selecting the required power components for the compensation and substituting them into (2.23), the reference filter currents can be computed. However, the $p - q$ theory has some inherent drawbacks in formulating power definitions. It assigns instantaneous active current even in circuits that consist solely of reactive elements. Similarly, it

attributes instantaneous reactive current in purely resistive circuits. Moreover, the instantaneous active and reactive currents exhibit triplen harmonics in linear circuits supplied by sinusoidal voltages. As a result, the $p - q$ theory fails to provide clear definitions for power terms, even under sinusoidal conditions [90]."

Generalized Instantaneous Reactive Power Theory [27, 89]

"Peng and Lai proposed a generalization of the instantaneous reactive power theory for three-phase systems by incorporating the contribution of zero sequence components to both non-active power and active power. In their approach, instead of initially decomposing the current into orthogonal components, they first defined the power components and then performed the current decomposition. The instantaneous phase voltages and currents are expressed as instantaneous space vectors in their formulation.

$$\mathbf{v} = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}; \quad \mathbf{i} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (2.24)$$

The instantaneous active power is defined as,

$$\mathbf{p} = \mathbf{v} \cdot \mathbf{i} = v_a i_a + v_b i_b + v_c i_c. \quad (2.25)$$

The instantaneous reactive power vector is defined as,

$$\mathbf{q} = \mathbf{v} \times \mathbf{i} = \begin{bmatrix} q_a \\ q_b \\ q_c \end{bmatrix} = \begin{bmatrix} v_b & v_c \\ i_b & i_c \\ v_c & v_a \\ i_c & i_a \\ v_a & v_b \\ i_a & i_b \end{bmatrix}. \quad (2.26)$$

The instantaneous active current is defined as,

$$\mathbf{i}_p = \begin{bmatrix} i_{ap} \\ i_{bp} \\ i_{cp} \end{bmatrix} = \frac{\mathbf{p}}{\mathbf{v} \cdot \mathbf{v}} \mathbf{v}. \quad (2.27)$$

The instantaneous reactive current vector is defined as,

$$\mathbf{i}_q = \begin{bmatrix} i_{aq} \\ i_{bq} \\ i_{cq} \end{bmatrix} = \frac{\mathbf{q} \times \mathbf{v}}{\mathbf{v} \cdot \mathbf{v}} \mathbf{v}. \quad (2.28)$$

The definition of active and reactive power on an instantaneous basis has been criticized due to the limitation of these definitions in determining the nature of the load. These definitions alone do not provide sufficient information to estimate the characteristics of the load [90]."

Synchronous Reference Frame Theory [84, 89]

"The synchronous reference frame (SRF) theory, also known as the *dq* theory, is a time-domain reference signal estimation technique introduced by R. H. Park in the 1920s. This method can be applied in both steady-state and transient conditions for various voltage and current waveforms. It enables real-time control of active power filters in power systems. The fundamental structure of a SRF controller includes direct *dq* and inverse *dq* Park transformations. The reference frame transformation converts the three-phase stationary system, represented by the *abc* coordinates, into a rotating coordinate system with the direct axis (*d*) and the quadrature axis (*q*). In the *abc* reference frame, the stationary axes are separated by 120° from each other, as shown in Fig. 2.12. The instantaneous space vectors, such as v_a and i_a on the *a*-axis, v_b and i_b on the *b*-axis, and v_c and i_c on the *c*-axis, can be easily transformed into the two-axis *dq0* rotating

reference frame. This algorithm facilitates the derivation of rotating current coordinates from the three-phase stationary coordinates, as illustrated below.

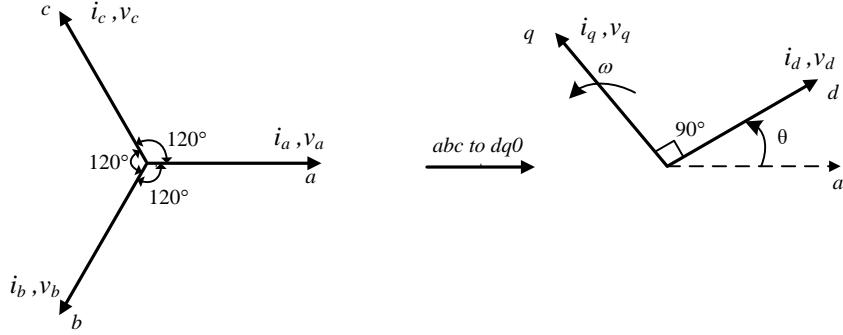


Figure 2.12: *abc* to *dq0* transformation

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} \text{ or } \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos \theta & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ -\sin \theta & -\sin(\theta - 2\pi/3) & -\sin(\theta + 2\pi/3) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \text{ or } \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (2.29)$$

The output signals of the *dq* transformation are dependent on the performance of the phase-locked loop (PLL). The PLL circuit determines the rotation speed (ω in rad/sec) of the rotating reference frame, where θ is the angle between the *a* and *q* axes for the *q*-axis alignment or the angle between the *a* and *d* axes for the *d*-axis alignment. Depending on the presence of fundamental, harmonic, and negative sequence components in voltages and currents, the *dq* components may have different frequencies. Analyzing these *dq* components and applying appropriate filtering techniques can facilitate the generation of current and voltage references needed for control purposes. The *dq* components typically comprise DC and AC components, as described below.

$$\begin{aligned} i_{Ld} &= \bar{i}_{Ld} + \tilde{i}_{Ld} \\ i_{Lq} &= \bar{i}_{Lq} + \tilde{i}_{Lq} \end{aligned} \quad (2.30)$$

The DC components \bar{i}_{Ld} and \bar{i}_{Lq} represent the fundamental positive sequence load currents, while the AC components \tilde{i}_{Ld} and \tilde{i}_{Lq} correspond to the load current harmonics. The component \bar{i}_{Lq} corresponds to the reactive power drawn by the load. The reference values for the compensator can be obtained as follows.

$$\begin{aligned} i_{fd}^* &= -\tilde{i}_{Ld} \\ i_{fq}^* &= -\bar{i}_{Lq} - \tilde{i}_{Lq} \\ i_{f0}^* &= -i_{L0} \end{aligned} \quad (2.31)$$

The shunt active filter references in *abc* reference frame are obtained as follows.

$$\begin{bmatrix} i_{fa}^* \\ i_{fb}^* \\ i_{fc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos \theta & -\sin \theta & \frac{1}{\sqrt{2}} \\ \cos(\theta - 2\pi/3) & -\sin(\theta - 2\pi/3) & \frac{1}{\sqrt{2}} \\ \cos(\theta + 2\pi/3) & -\sin(\theta + 2\pi/3) & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{fd}^* \\ i_{fq}^* \\ i_{f0}^* \end{bmatrix} \quad (2.32)$$

When the supply voltages are unbalanced or distorted, the accuracy of the transformation angle (θ) obtained from the PLL may be compromised. As a result, the performance of the *dq* transformation approach can be adversely affected in such situations. Moreover, this method involves complex transformations, and its implementation in digital signal processors (DSP) can be challenging [91, 92]."

Instantaneous Symmetrical Components Theory [29, 82, 83, 87]

"The theory of instantaneous symmetrical components is applicable for load balancing, harmonic suppression, and power factor correction. The control algorithm based on the instantaneous symmetrical component theory can partially or fully compensate for any type of load unbalance and harmonics. It achieves this by employing high-bandwidth current sources to track the filter reference currents. This control algorithm has been developed and elucidated in this section. According to the symmetrical component theory, any three-phase instantaneous quantities can be expressed in terms of positive,

negative, and zero sequences using the equation provided below [93].

$$\begin{bmatrix} i_{sa}^0 \\ i_{sa}^+ \\ i_{sa}^- \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix}; \quad \begin{bmatrix} v_{sa}^0 \\ v_{sa}^+ \\ v_{sa}^- \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \quad (2.33)$$

In (2.33), the symbols $+$, $-$ and 0 represent the positive, negative and zero sequence components, respectively. The complex operator ‘ a ’ is equal to e^{j120° . It should be noted that the instantaneous positive sequence (i_{sa}^+) and negative sequence (i_{sa}^-) components are complex conjugates of each other, while the zero sequence component (i_{sa}^0) is a real quantity that equals zero when the currents are balanced. Similar to the pq theory, it is assumed that the supply voltages are balanced.

The objective of a three-phase four-wire system is to ensure the provision of a balanced supply current in which the zero sequence component is zero. Consequently, the following condition is obtained.

$$i_{sa} + i_{sb} + i_{sc} = 0 \quad (2.34)$$

The angle between the positive sequence components of the source current (i_{sa}^+) and the source voltage (v_{sa}^+) is equal to the power factor angle (φ^+) between the balanced source currents and voltages. In the control algorithm, this power factor angle can be explicitly set to any desired value. However, in the previously described pq theory, the power factor angle is not directly expressed. Assuming that the phase of i_{sa}^+ lags behind that of v_{sa}^+ by an angle (φ^+), we obtain the following relationship.

$$\angle\{v_{sa} + av_{sb} + a^2v_{sc}\} = \angle\{i_{sa} + ai_{sb} + a^2i_{sc}\} + \varphi^+ \quad (2.35)$$

After substituting the values for a and a^2 into (2.35), it expands to the following

expression:

$$\angle \left\{ \left(v_{sa} - \frac{1}{2}v_{sb} - \frac{1}{2}v_{sc} \right) - j \frac{\sqrt{3}}{2}(v_{sb} - v_{sc}) \right\} = \angle \left\{ \left(i_{sa} - \frac{1}{2}i_{sb} - \frac{1}{2}i_{sc} \right) - j \frac{\sqrt{3}}{2}(i_{sb} - i_{sc}) \right\} + \varphi^+. \quad (2.36)$$

By equating the angles in the above equation, the following expression can be written.

$$\tan^{-1}(K_1/K_2) = \tan^{-1}(K_3/K_4) + \varphi^+ \quad (2.37)$$

Where,

$$\begin{aligned} K_1 &= \frac{\sqrt{3}}{2}(v_{sb} - v_{sc}) & K_2 &= \left(v_{sa} - \frac{1}{2}v_{sb} - \frac{1}{2}v_{sc} \right) \\ K_3 &= \frac{\sqrt{3}}{2}(i_{sb} - i_{sc}) & K_4 &= \left(i_{sa} - \frac{1}{2}i_{sb} - \frac{1}{2}i_{sc} \right). \end{aligned}$$

By taking the tangent of both sides of (2.37), the following is obtained.

$$\frac{K_1}{K_2} = \tan [\tan^{-1}(K_3/K_4) + \varphi^+] = \frac{K_3/K_4 + \tan \varphi^+}{1 - (K_3/K_4)\tan \varphi^+} \quad (2.38)$$

By substituting the values of K_1 , K_2 , K_3 , and K_4 into the above equation, the following is obtained.

$$\begin{aligned} (v_{sb} - v_{sc} - 3\gamma(v_{sa} - v_0))i_{sa} + (v_{sc} - v_{sa} - 3\gamma(v_{sb} - v_0))i_{sb} + \\ (v_{sa} - v_{sb} - 3\gamma(v_{sc} - v_0))i_{sc} = 0 \end{aligned} \quad (2.39)$$

Where $\gamma \equiv \tan \varphi^+ / \sqrt{3}$. For a unity power factor, $\varphi^+ = 0$, hence $\gamma = 0$. It is well known that in a balanced three-phase circuit, the instantaneous power remains constant, while in an unbalanced circuit, it exhibits a double-frequency component in addition to the DC or mean value. The presence of harmonics introduces higher-frequency oscillating components in the instantaneous power. The objective of the compensator is to supply the oscillating component of the instantaneous load power, while the source provides the

average value of the load power, P_{avg} . Therefore, the following expression is obtained.

$$v_{sa}i_{sa} + v_{sb}i_{sb} + v_{sc}i_{sc} = P_{avg} \quad (2.40)$$

Since the harmonic component in the load does not require any real power, the source only needs to supply the real power required by the load. The average load power can be calculated using a moving average filter. By combining equations (2.34), (2.39), and (2.40), we obtain the reference source currents as follows:

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = M^{-1} \begin{bmatrix} 0 \\ 0 \\ P_{avg} \end{bmatrix}. \quad (2.41)$$

Where,

$$M = \begin{bmatrix} 1 & 1 & 1 \\ (v_{sb} - v_{sc} - 3\gamma(v_{sa} - v_0)) & (v_{sc} - v_{sa} - 3\gamma(v_{sb} - v_0)) & (v_{sa} - v_{sb} - 3\gamma(v_{sc} - v_0)) \\ v_{sa} & v_{sb} & v_{sc} \end{bmatrix}.$$

The reference compensator currents are given as,

$$\begin{aligned} i_{fa}^* &= i_{la} - i_{sa}^* = i_{la} - \frac{(v_{sa} - v_0) + \gamma(v_{sb} - v_{sc})}{\Delta_1}(P_{avg}), \\ i_{fb}^* &= i_{lb} - i_{sb}^* = i_{lb} - \frac{(v_{sb} - v_0) + \gamma(v_{sc} - v_{sa})}{\Delta_1}(P_{avg}), \\ i_{fc}^* &= i_{lc} - i_{sc}^* = i_{lc} - \frac{(v_{sc} - v_0) + \gamma(v_{sa} - v_{sb})}{\Delta_1}(P_{avg}). \end{aligned} \quad (2.42)$$

Where,

$$\Delta_1 = \left[\sum_{j=a,b,c} v_{sj}^2 \right] - 3v_0^2, \quad v_0 = \frac{1}{3} \sum_{k=a,b,c} v_{sk}, \quad \gamma = \tan \varphi / \sqrt{3}. \quad (2.43)$$

When incorporating the inverter power loss P_{loss} into (2.42), the modified reference

currents of the compensator become:

$$\begin{aligned} i_{fa}^* &= i_{la} - i_{sa}^* = i_{la} - \frac{(v_{sa} - v_0) + \gamma(v_{sb} - v_{sc})}{\Delta_1} (P_{lavg} + P_{loss}), \\ i_{fb}^* &= i_{lb} - i_{sb}^* = i_{lb} - \frac{(v_{sb} - v_0) + \gamma(v_{sc} - v_{sa})}{\Delta_1} (P_{lavg} + P_{loss}), \\ i_{fc}^* &= i_{lc} - i_{sc}^* = i_{lc} - \frac{(v_{sc} - v_0) + \gamma(v_{sa} - v_{sb})}{\Delta_1} (P_{lavg} + P_{loss}). \end{aligned} \quad (2.44)$$

In the described system, the term P_{lavg} represents the average power required by the load, which is obtained using a simple moving average filter over a half cycle. The oscillating part of the real power has a frequency that is double the system frequency. The term P_{loss} is obtained from a proportional-integral (PI) controller. The error between the DC voltage reference and the actual DC voltage is processed through the PI controller to obtain P_{loss} . This control mechanism helps to regulate the DC-link voltage by adjusting the small amount of real power absorbed by the shunt inverter. The reference current of the shunt active filter contains not only reactive and harmonic components but also some amount of active current as compensating current. This active compensating current flows through the shunt active filter and helps to regulate the DC capacitor voltage [29]. The shunt active filter draws this active current from the AC source, to recharge the DC capacitor. It should be noted that when the source voltages are balanced, the zero sequence voltage v_0 is equal to zero in the above equations.

When the source voltages used for generating the shunt filter current references are unbalanced and distorted, it can lead to erroneous compensation using the conventional shunt algorithm [94]. To overcome this limitation, an improved approach is proposed where the fundamental positive sequence voltages $v_{sa1}^+(t)$, $v_{sb1}^+(t)$ and $v_{sc1}^+(t)$ of the PCC voltages are extracted. These extracted voltages are then used in the shunt algorithm to

generate the reference compensator currents, as given below.

$$\begin{aligned} i_{fa}^* &= i_{la} - i_{sa}^* = i_{la} - \frac{v_{sa1}^+ + \gamma^+(v_{sb1}^+ - v_{sc1}^+)}{\Delta_1^+} (P_{lavg} + P_{loss}) \\ i_{fb}^* &= i_{lb} - i_{sb}^* = i_{lb} - \frac{v_{sb1}^+ + \gamma^+(v_{sc1}^+ - v_{sa1}^+)}{\Delta_1^+} (P_{lavg} + P_{loss}) \\ i_{fc}^* &= i_{lc} - i_{sc}^* = i_{lc} - \frac{v_{sc1}^+ + \gamma^+(v_{sa1}^+ - v_{sb1}^+)}{\Delta_1^+} (P_{lavg} + P_{loss}) \end{aligned} \quad (2.45)$$

Where,

$$\Delta_1^+ = \sum_{j=a,b,c} (v_{sj1}^+)^2; \quad \gamma^+ = \tan \varphi^+ / \sqrt{3}. \quad (2.46)$$

Out of various theories discussed above, the instantaneous symmetrical component theory with the extraction of fundamental positive sequence components offers a simple and clear formulation for power system control. It eliminates ambiguity in definitions of various power terms and provides flexibility in handling various load and voltage conditions. Its compactness makes it suitable for implementation in digital signal processors, enabling real-time and effective compensation [94, 95]."

2.5.2 Generation of Reference Quantities for DVR

The voltage compensation method can be chosen based on factors such as the dynamic voltage restorer's (DVR) power rating, load characteristics, operating conditions, the load's susceptibility to phase angle jumps, and fault types [96]. There are three main voltage injection/compensation strategies that can be employed.

Pre-Sag Compensation

"In order to keep the load voltage at the pre-sag level, the pre-sag compensation method continually monitors the supply voltage and generates a compensation voltage. It is particularly suitable for sensitive loads that are adversely affected by sudden changes in phase angle. However, supplying both active and reactive powers from the VSI is

required for this technique, which also demands for a higher-rated DVR. Due to the fact that this scheme uses active power from the VSI, DVR requires a large energy storage capacity.

The per phase phasor diagram of the pre-sag compensation shows that the pre-sag and post-sag voltages are at the same position, i.e., $V_{pre-sag} = V_{post-sag}$. In the phasor diagram, the change in phase angle of the grid terminal voltage V_{tsag} is denoted as θ , the load current is denoted as I_l and the load power factor angle is denoted as ϕ . The phasor angles are defined with respect to load current. In order to adjust the load voltage to its pre-sag value as part of the compensation, a voltage of $V_{dvr} = V_{inj}$ is injected. Phase-locked loops (PLLs) must be used with this technique in order to synchronise with the load voltages. The magnitude and phase angle (α) of the DVR injection voltage, as well as the active and reactive power associated with load voltage compensation, are calculated based on the phase jump of the grid voltage and sag depth. The equations for these calculations are given in (2.47) - (2.50)."

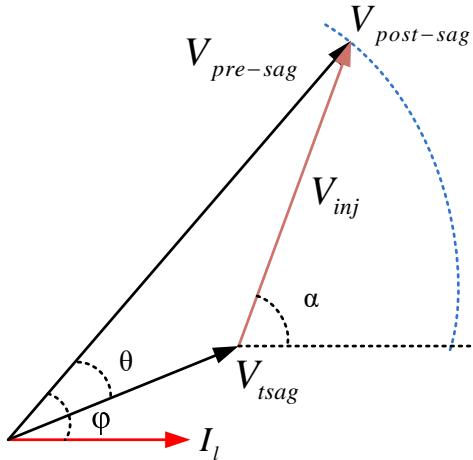


Figure 2.13: Per phase phasor diagram for pre-sag compensation [97]

$$|V_{dvr}| = \sqrt{V_{pre-sag}^2 - 2V_{pre-sag}V_{tsag} \cos \theta + V_{tsag}^2} \quad (2.47)$$

$$\angle V_{dvr} = \alpha = \tan^{-1} \left(\frac{V_{pre-sag} \sin \phi - V_{tsag} \sin(\phi - \theta)}{V_{pre-sag} \cos \phi - V_{tsag} \cos(\phi - \theta)} \right) \quad (2.48)$$

$$P_{dvr} = |V_{dvr}| I_l \cos \alpha \quad (2.49)$$

$$Q_{dvr} = |V_{dvr}| I_l \sin \alpha \quad (2.50)$$

In-Phase Compensation

"The supply voltage and the injected voltage are in phase with one another when using the in-phase compensation method. This method aims to reduce the required injection voltage, which allows for a lower voltage rating of the storage unit or DC-link bus. However, this method has to account for active power injection. It is important to note that the in-phase compensation method only mitigates the load voltage magnitude but not the phase jump. Therefore, it is not appropriate for loads that are sensitive to phase jumps. The phasor diagram in Fig. 2.14 can be used to determine the magnitude of the DVR injection voltage as well as the active and reactive powers related to compensation of load voltages. The specific calculations are as follows:"

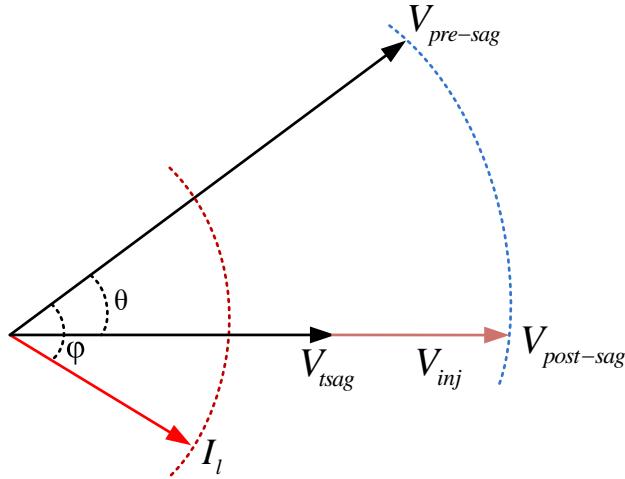


Figure 2.14: Per phase phasor diagram for in-phase compensation [97]

$$|V_{dvr}| = |V_{pre-sag}| - |V_{tsag}|, \quad (2.51)$$

$$P_{dvr} = |V_{dvr}| I_l \cos(\phi - \theta), \quad (2.52)$$

$$Q_{dvr} = |V_{dvr}| I_l \sin(\phi - \theta). \quad (2.53)$$

Energy Optimized Compensation

"The energy optimized compensation technique is employed to minimize the active power requirement of the DVR circuit. In this method, the DVR is controlled to ensure that the compensation voltages are perpendicular to the load currents, resulting in supply of zero active power by the DVR. The main objective is to absorb as much active power as possible from the grid during voltage sag, reducing the reliance on the DVR for active power compensation. While this technique minimizes the energy requirement for load voltage restoration, it does not address the phase jump that occurs during sag events. Furthermore, there is a limitation on the minimum sag depth that can be compensated without active power supply. If the grid terminal voltage drops below a certain threshold, the compensation technique will require active power supply to restore the load voltage.

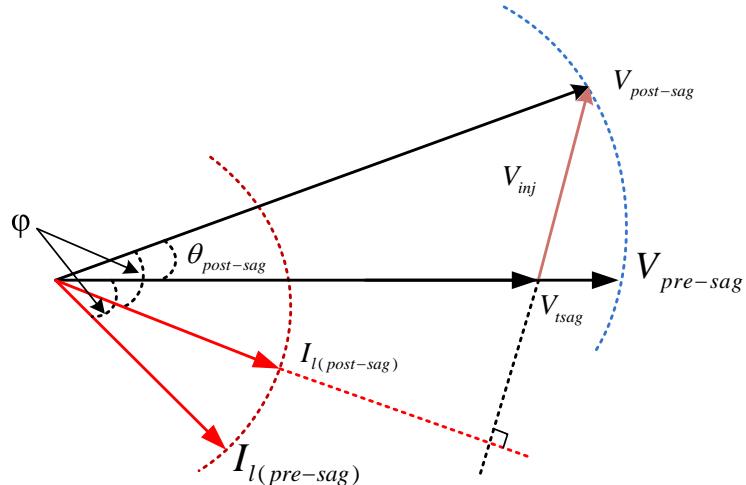


Figure 2.15: Per phase phasor diagram for energy optimized load voltage compensation

The magnitude of the DVR injection voltage, as well as the active and reactive powers related to the compensation of load voltages, can be calculated from the phasor diagram illustrated in Fig. 2.15. The specific calculations are as follows:"

$$|V_{dvr}| = \sqrt{V_{pre-sag}^2 - 2V_{pre-sag}V_{tsag} \cos \theta_{post-sag} + V_{tsag}^2}, \quad (2.54)$$

$$\angle V_{dvr} = \alpha = 90^\circ, \quad (2.55)$$

$$P_{dvr} = 0, \quad (2.56)$$

$$Q_{dvr} = |V_{dvr}| I_l. \quad (2.57)$$

2.5.3 Switching Control Techniques

In Section 2.4, various drawbacks were identified for the shunt and series control circuits that were based on linear controllers. These limitations sparked the exploration of alternative control techniques. This section aims to review the most commonly used control methods that have been developed for DSTATCOM, DVR, and conventional UPQC.

A. Hysteresis Control

Hysteresis control is a non-linear control technique that aims to make a measured signal follow its reference by using a non-linear feedback loop. This is achieved by adding a defined error of the measured signal to its reference waveform, creating upper and lower boundaries, also known as a hysteresis band. The switching actions of a converter keep the measured signal within this band [98]. Hysteresis control can be designed in different reference frames and can control current as well as voltage [99–101].

The key benefits of hysteresis control over linear controllers include its ease of implementation, minimal tracking errors, robustness, independence from changes in load parameters, and good dynamics. However, there are some drawbacks. One is that in systems without a neutral connection, the instantaneous error of the measured signal can reach double due to the interaction between three phases [102], and hence the three phases must be decoupled. Another drawback is that the hysteresis control produces varying switching frequency during the fundamental period, which can cause an increase in switching losses and difficulty in designing input filters.

B. Constant Switching Frequency Hysteresis Controllers

Several design solutions were developed to overcome the main drawback of variable switching frequency inherent in hysteresis control methods. Although the functional principle of hysteresis controllers with constant switching frequency is typically the same as for conventional hysteresis techniques, the switching frequency is fixed. The first solution is a ramp controller without hysteresis [103], where the measured signal is compared with a modulated reference created by adding a fixed amplitude and frequency triangular carrier. Implementation of three 120° phase-shifted triangular carriers is also possible [98]. However, this method generates errors in amplitude and phase of the measured signal [98], and experiences over-crossing and under-crossing effects [103]. The second solution is the addition of hysteresis to the ramp controller, which eliminates problems with measured signal errors and requires lower carrier frequency for overcoming crossing effects [103]. In systems without a neutral connection, these techniques significantly degrade in performance, particularly if a DC-offset is required, as in the case of the nine-switch UPQC. As a result, these control techniques are unsuitable for replacing linear controllers. Finally, an adaptive hysteresis-band or a variable-band hysteresis controller is another solution for providing constant switching frequency, which changes the hysteresis bandwidth to provide an optimal switching frequency that remains nearly constant [104]. Although the simplicity of this hysteresis method is lost in comparison to the conventional hysteresis controller, it still provides all other advantages. This control method was implemented as a fuzzy-logic controller in the conventional UPQC to control its current and voltage [105], and its applicability for controlling current was demonstrated in systems without a neutral connection [106].

C. Sliding Mode Control

Several control techniques were proposed based on the sliding mode concept, which are designed to control both current and voltage. These controllers include sliding

mode control (SMC) [107], sliding mode pulse width modulation (SMPWM) [108], and hysteresis-modulation sliding mode pulse width modulation (HM-SMPWM) [46], all of which are designed in the *abc* natural frame.

One of the main advantages of the sliding mode concept is its ability to provide a coherent mathematical model for decoupling interactive three-phase signals of power systems without a neutral connection. This model was proposed for controlling current in the three-phase system without a neutral connection [108]. Another study proposed the use of the sliding mode concept to control two sets of three-phase currents of the nine-switch converter [46]. The SMC controller proposed in [107] was based on the SMC theory for controlling voltage in the 3P3W system. However, it did not apply the decoupling technique based on the sliding mode concept. Instead, it connected the DC-link mid-point to the neutral point of star-connected series transformers, which nullified the interaction between three-phase voltages and the use of DC-offsets/neutral-point voltages. Consequently, this control method is unsuitable for providing proper operation of the nine-switch UPQC.

2.6 SUMMARY

This chapter provides an overview of the conventional unified power quality conditioner (UPQC), including the operation of the dual-output converter and its advantages and limitations compared to the back-to-back topology. It also discusses the previously designed nine-switch converter based UPQC. The performance of the nine-switch UPQC depends greatly on the accurate selection of its operation modes under different working conditions, as well as the control methods used for the shunt and series terminals.

The chapter examines the control methods that have already been applied in the nine-switch UPQC, which utilize linear controllers and have shown satisfactory results.

However, these methods have certain drawbacks that have prompted the search for alternative solutions. Non-linear control methods have been presented for controlling two sets of three-phase currents in the nine-switch converter. However, no potential replacement has been found for the series terminal controller. Additionally, the generation of reference quantities requires an accurate estimation of the grid voltage phase angle. Therefore, Chapter 3 discusses the performance comparison of advanced phase-locked loops (PLLs). Furthermore, Chapter 4 presents the proposed sliding mode control for the four-leg distribution static synchronous compensator (DSTATCOM), Chapter 5 focuses on the four-leg dynamic voltage restorer (DVR), and Chapter 6 covers the four-leg dual-output converter based UPQC.

CHAPTER 3

A PERFORMANCE COMPARISON OF ADVANCED PLLs FOR GRID SYNCHRONIZATION

3.1 INTRODUCTION

In Chapter 2, a comprehensive discussion on the operating principle of the UPQC has been provided, specifically focusing on the implementation of both back-to-back and dual-output converters. Additionally, an extensive literature survey exploring various control strategies for generating reference quantities and control techniques has been included. The accurate estimation of the grid voltage phase angle is crucial for generating reference quantities, and the widely used method for this is the synchronous reference frame phase-locked loop (SRF-PLL). However, it is important to note that the dynamic performance of the SRF-PLL is optimal only when the grid voltages are balanced and free from distortion [109]. With the increasing integration of renewable energy sources (RESs) and the utilization of nonlinear loads in the distribution system, issues such as phase angle jumps, harmonics, and distortions in grid voltage can arise. Under such conditions, the dynamic performance of the SRF-PLL with high bandwidth deteriorates. To address this problem, one possible approach is to select a low bandwidth for improved performance, but this compromises the response speed, resulting in slower dynamic response.

To accurately extract phase angle information from the distorted grid voltages, while maintaining zero steady-state error and achieving a fast response, it is necessary to pass the fundamental frequency positive sequence (FFPS) components through the SRF-PLL. In the literature, there are various methods available for extracting FFPS components, which can be broadly classified into two categories.

The first method is based on notch filters using the instantaneous symmetrical components theory (ISCT). By employing notch filters, the fundamental and quadrature components of the signals are extracted, and then the positive sequence components are derived using the ISCT. The second method utilizes delay operators, which inherently possess filtering capabilities. In this approach, quadrature signals can be generated by applying delay operators to each phase. However, it is worth noting that this method may result in increased execution time for digital simulators due to the higher demand for delay operators. Examples of the former method include enhanced PLL (EPLL) and second-order generalized integrator (SOGI). On the other hand, examples of the latter method include cascaded delayed signal cancellation (CDSC) and multiple delayed signal cancellation (MDSC) methods.

In [110], three EPLLs are employed, one for each phase, to extract the FFPS components. A fourth EPLL is employed to extract the phase angle of the grid voltage. The EPLL's performance remains robust in the face of frequency variations due to its frequency adaptive notch filter characteristics. To reduce the number of EPLLs employed, a dual EPLL (DEPLL) is proposed in the $\alpha\beta$ reference frame [111]. This proposal assumes that the $\alpha\beta$ components of grid voltages are quadrature to each other. However, this assumption is no longer valid in unbalanced grid systems. To overcome this limitation, the second-order generalized integrator (SOGI) is suggested as a quadrature signal generator (QSG) [112]. In recent years, PLLs based on SOGI, CDSC, and MDSC have gained popularity due to their individual advantages. However, each PLL approach has its own drawbacks. This chapter provides a concise review of these PLLs, explaining their basic principles, concepts and performance comparison.

3.2 REVIEW ON ADVANCED PLLs

This section presents a brief overview of SOGI, CDSC and MDSC based PLLs.

3.2.1 Second Order Generalized Integrator Based PLL

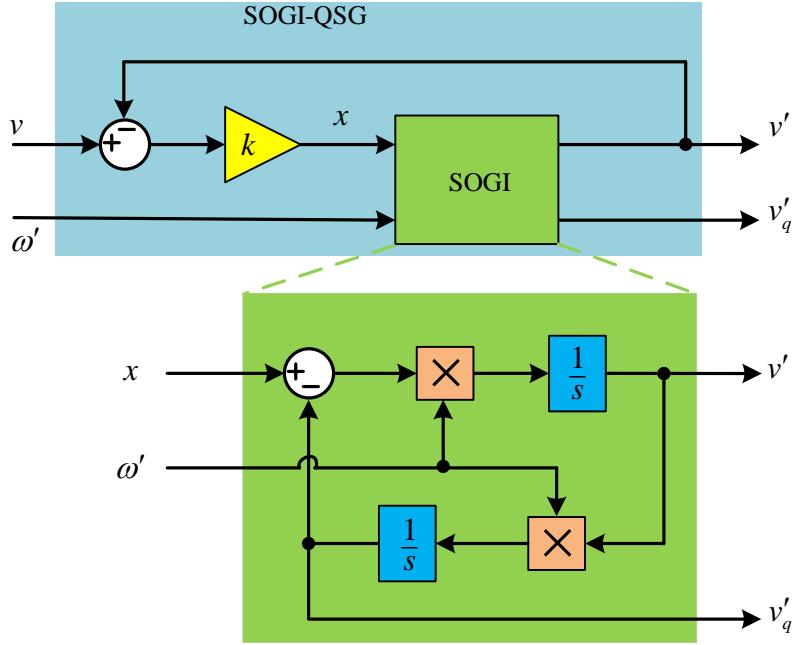


Figure 3.1: General structure for SOGI based QSG

A general structure for SOGI based QSG is shown in Fig. 3.1. The transfer functions of input signal (v) to its in-phase filtered signal (v'), and input signal (v) to its filtered quadrature signal (v'_q) are respectively given in (3.1) and (3.2).

$$\begin{aligned} \frac{v'(s)}{v(s)} &= \frac{k\omega's}{s^2 + k\omega's + \omega'^2} \\ \left| \frac{v'}{v} \right| &= \frac{k\omega'\omega}{\sqrt{(\omega'^2 - \omega^2)^2 + (k\omega'\omega)^2}} \\ \angle \frac{v'}{v} &= \frac{\pi}{2} - \tan^{-1} \left(\frac{k\omega'\omega}{(\omega'^2 - \omega^2)^2} \right) \end{aligned} \quad (3.1)$$

$$\begin{aligned} \frac{v'_q(s)}{v(s)} &= \frac{k\omega'^2}{s^2 + k\omega's + \omega'^2} \\ \left| \frac{v'_q}{v} \right| &= \frac{k\omega'^2}{\sqrt{(\omega'^2 - \omega^2)^2 + (k\omega'\omega)^2}} \\ \angle \frac{v'_q}{v} &= -\tan^{-1} \left(\frac{k\omega'\omega}{(\omega'^2 - \omega^2)^2} \right) \end{aligned} \quad (3.2)$$

Where, ω' is the resonant or natural frequency of the system, ω is the frequency of input signal, and k is the gain which decides the transient response of a system. It is evident from (3.1) and (3.2) that SOGI-QSG offers band pass and low pass filtering features for

v' and v'_q , respectively. Furthermore, few more conclusions are derived from (3.1) and (3.2) as follows:

- Discrepancy between resonant frequency and the fundamental frequency of input signal doesn't meet the requirement of SOGI-QSG in accurately extracting the fundamental frequency signal and its quadrature signal. To address this limitation and achieve frequency adaptability, SRF-PLL is employed in conjunction with the SOGI-QSG, as depicted in Fig. 3.2. The SRF-PLL estimates the fundamental frequency of the input signal and provides it as the resonant frequency input to the SOGI-QSG [113]. This integration of the SRF-PLL enables the SOGI-QSG to dynamically adjust and align its resonant frequency with the fundamental frequency of the input signal, thereby ensuring accurate extraction of the fundamental frequency signal and its quadrature signal.
- The bandpass filtering characteristic of the SOGI-QSG allows it to selectively pass signals at the resonant frequency while attenuating other frequency signals. Consequently, when applied to a distorted grid with dominant lower-order harmonics, the output signal v' of the SOGI-QSG exhibits a non sinusoidal shape. This distortion in the waveform introduces errors in both phase angle and frequency estimation when v' is used as an input to the SRF-PLL. Further, the SOGI-QSG is capable of completely removing the DC component of the input signal in the output signal v' .
- The SOGI-QSG exhibits a low-pass filtering characteristic for the filtered quadrature signal, v'_q . This means that it allows signals with frequencies up to the resonant frequency to pass through, while attenuating signals with frequencies beyond the resonant frequency. Consequently, when applied to a distorted grid voltage containing dominant lower-order harmonics, the resulting v'_q waveform may exhibit a non sinusoidal shape. In addition to the distortions caused by the lower-order harmonics, the presence of DC signal in the sensed grid voltages, which can arise due to voltage sensor errors, further distorts the v'_q waveform.

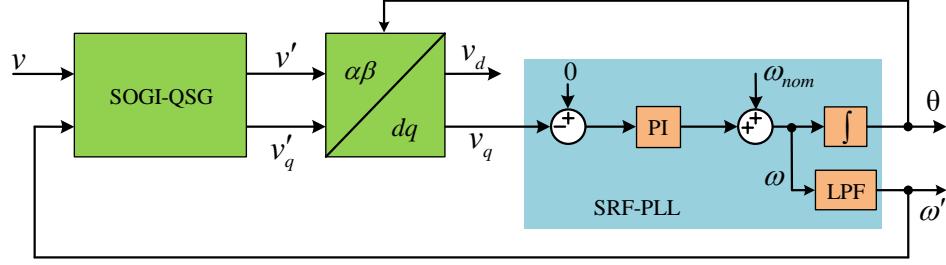


Figure 3.2: General structure for frequency adaptive 1-ph SOGI-PLL

This distortion introduces errors in both phase angle and frequency estimation when the distorted v'_q is utilized as an input to the SRF-PLL.

- v'_q always lags v' by 90° irrespective of the resonant frequency and gain k [111].

In a three-phase system, three individual SOGI-QSGs are utilized, with one dedicated to each phase. These SOGI-QSGs are responsible for extracting the fundamental frequency signal and its orthogonal signal for each respective phase. The extracted signals are then used to calculate the FFPS components based on the ISCT, as described in (3.3). These FFPS components are subsequently fed into the SRF-PLL as shown in Fig. 3.3. The calculation of FFPS components are shown in figure inside the positive sequence components (PSC_{abc}) blockset.

$$\begin{aligned}
 v_a'^+ &= \frac{1}{3} \left[\left\{ v_a' - \frac{1}{2}(v_b' + v_c') \right\} - \frac{\sqrt{3}}{2} \left\{ v_{bq}' - v_{cq}' \right\} \right] \\
 v_b'^+ &= -v_a'^+ - v_c'^+ \\
 v_c'^+ &= \frac{1}{3} \left[\left\{ v_c' - \frac{1}{2}(v_a' + v_b') \right\} - \frac{\sqrt{3}}{2} \left\{ v_{aq}' - v_{bq}' \right\} \right]
 \end{aligned} \tag{3.3}$$

By analyzing system signals in the $\alpha\beta$ reference frame, the number of required SOGI-QSGs can be reduced to two, resulting in a dual SOGI (DSOGI) based PLL. This approach is depicted in Fig. 3.4. This configuration also helps to estimate phase angle even in the presence of DC offsets. The zero sequence components or DC offsets in the three-phase input signals are not fed to SOGI operators, thereby DSOGI is insensitive to the DC offsets. The positive sequence components in the $\alpha\beta$ reference frame ($PSC_{\alpha\beta}$)

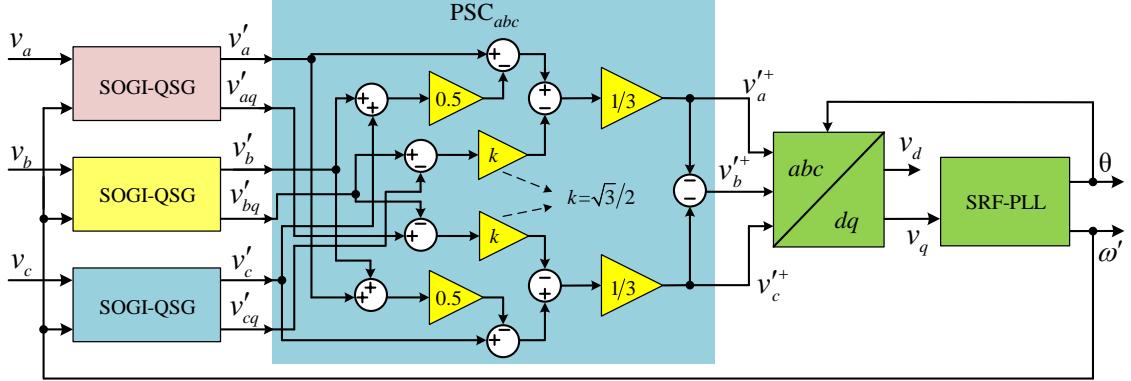


Figure 3.3: General structure for frequency adaptive 3-ph SOGI-PLL

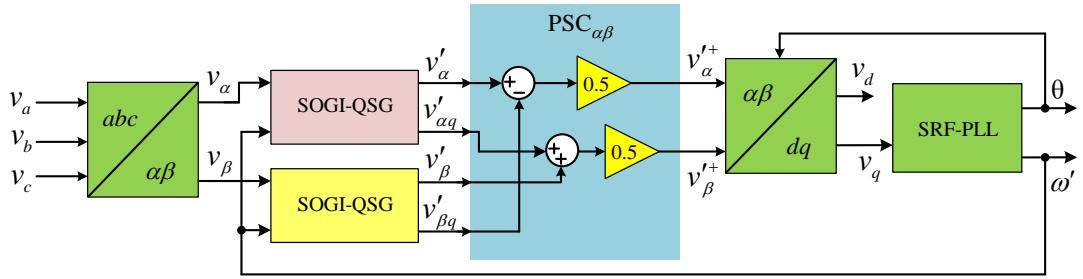


Figure 3.4: General structure for frequency adaptive DSOGI-PLL

can also be obtained using the ISCT, which is expressed as follows [113].

$$\begin{aligned} v'_\alpha^+ &= \frac{1}{2} (v'_\alpha - v'_{\beta q}) \\ v'_\beta^+ &= \frac{1}{2} (v'_{\alpha q} + v'_\beta) \end{aligned} \quad (3.4)$$

In power systems, it is often necessary to extract specific harmonic frequency signals for fault analysis and designing control systems like PR controllers for custom power devices. To meet this requirement, a multiple SOGI (MSOGI) based PLL is employed, as illustrated in Fig. 3.5 [114, 115].

Each SOGI-QSG within the MSOGI is responsible for extracting a particular harmonic frequency signal. However, it is crucial to ensure that the SOGI-QSG intended for a specific harmonic frequency does not receive signals with frequencies lower than that particular harmonic. This is because SOGI-QSG employs a low-pass filter for the quadrature signal (v'_q). Fig. 3.5 demonstrates this concept, where the input signal

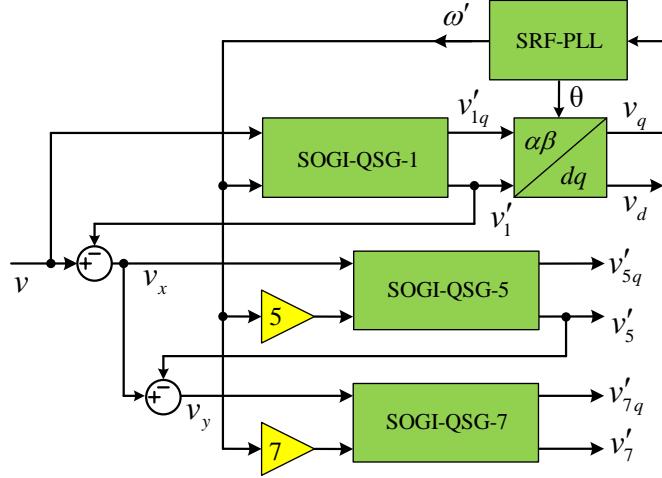


Figure 3.5: General structure for frequency adaptive 1-ph MSOGI-PLL

for SOGI-QSG-7 is obtained by subtracting the outputs of the preceding SOGI-QSGs (corresponding to $h = 1$ and 5) from the actual input signal. It should be noted that if the actual input signal contains any of the 2^{nd} , 3^{rd} , 4^{th} , or 6^{th} harmonic frequencies, the extracted 7^{th} harmonic frequency signal will not be accurate. This discrepancy arises due to the lowpass filter characteristics of the SOGI.

Furthermore, the bandpass filter characteristics of the SOGI result in the output of each SOGI-QSG-h predominantly containing the h^{th} harmonic frequency signals, along with partial components of other frequencies. For instance, in Fig. 3.5, the output of SOGI-QSG-1 includes the fundamental frequency component, as well as a fraction of the 5^{th} and 7^{th} harmonic frequency components. As a result, this inaccurate input signal affects the performance of subsequent SOGI-QSG-hs (for $h = 5$ and 7). To mitigate this issue to some extent, the input signal for each SOGI-QSG is calculated by subtracting the output of all other SOGI-QSGs from the original input signal [114, 115]. This approach helps minimize the undesired components and enhances the accuracy of the extracted harmonic frequency signals.

3.2.2 Cascaded Delayed Signal Cancellation Based PLL

To eliminate a specific frequency signal $v_h(t)$ from a given signal, the delayed signal cancellation (DSC) operator is used [116]. The out-of-phase signal of $v_h(t)$ can be

obtained by introducing a time delay of $\frac{T}{n}$, where T is the fundamental time period and n is an integer. By adding the given signal to the delayed signal as given below, the specific frequency signal can be eliminated from the given signal.

$$DSC_n = \frac{1}{2} [v_h(t) + v_h(t - T/n)]$$

The choice of the delay time $\frac{T}{n}$ depends on the specific frequency signal to be eliminated. The minimum time delay required for the DSC_n operator is the period from time $t = 0$ to the time at which the negative zero crossing of the signal occurs. In general, the possible delay times $(\frac{T}{n})$ to eliminate the h^{th} harmonic frequency signal can be calculated as follows:

$$\frac{T}{n} = \frac{T}{2h} + k \frac{T}{h} \quad \forall \ k < h - 0.5 \ \& \ k \in N_0. \quad (3.5)$$

For example, to eliminate a 4^{th} harmonic frequency signal, the possible delay times are $\frac{T}{8}, (\frac{T}{8} + \frac{T}{4}), (\frac{T}{8} + \frac{2T}{4}),$ and $(\frac{T}{8} + \frac{3T}{4}),$ as shown in Fig. 3.6.

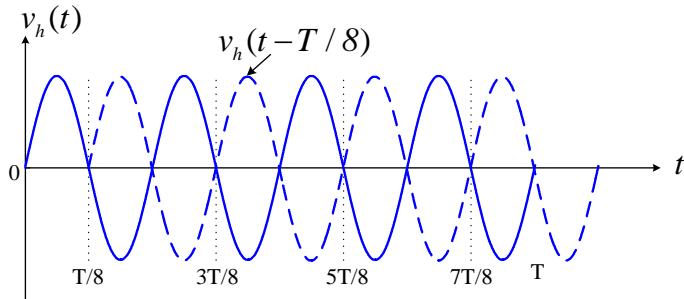


Figure 3.6: Fourth order frequency signal and its delayed signal

In other words, for a known delay time, all the eliminated harmonics are obtained from (3.5) and is given as,

$$h = nk + \frac{n}{2} \quad \forall \ k, h \in N_0.$$

Based on the above equation, the harmonics eliminated by the DSC operators $DSC_2, DSC_4, DSC_8, DSC_{16}$ and DSC_{32} are $2k + 1, 4k + 2, 8k + 4, 16k + 8$ and

$32k + 16$, respectively. These operators are commonly used because they ensure that no single harmonic signal is eliminated by any two operators. The harmonics that are passed without attenuation through these DSC operators are $2k, 4k, 8k, 16k$ and $32k$, respectively. To eliminate all lower order harmonics effectively, these DSC operators are cascaded in such a way that no signal is attenuated by any individual DSC operator. This results in a new operator called the cascaded delayed signal cancellation (*CDSC*) operator [117–122]. It is important to note that while this operator is designed for use in the dq reference frame, if applied in the abc frame, it will eliminate the fundamental frequency component that is necessary for grid synchronization using an SRF-PLL.

Table 3.1: Harmonic order and nature in abc and dq frames at a rotating speed of ω

Harmonic order (h) in abc frame $\forall k \in N_0$			Harmonic order (h) in dq frame $\forall k \in N_0$	
h	sequence	nature	h	nature
$6k + 1$	positive	odd, balanced	$6k$	even
		odd, unbalanced	$6k \& 6k + 2$	
$6k - 1$	negative	odd, balanced	$6k$	even
		odd, unbalanced	$6k \& 6k - 2$	
$3(2k + 1) + 1$	positive	even, balanced	$3(2k + 1)$	odd
		even, unbalanced	$3(2k + 1) \& 3(2k + 1) + 2$	
$3(2k - 1) - 1$	negative	even, balanced	$3(2k + 1)$	odd
		even, unbalanced	$3(2k + 1) \& 3(2k + 1) - 2$	
$3k \ \forall k \in N$	zero	odd/even, balanced	No dq components present	
		odd/even, unbalanced	$3k + 1 \& 3k - 1$	even/odd
0	—	DC, balanced	No dq components present	
		DC, unbalanced	+1	odd

The dq reference frames in vector space have the flexibility to be rotated at any frequency and in any direction. Typically, they are rotated at the fundamental frequency and in synchronism with the rotation of the resultant vector. As a result, the balanced fundamental frequency components in the abc frame appear as a DC quantity in the dq frame.

Table 3.1 provides the relationship between the harmonic orders in the abc and dq frames. It can be observed that odd-order frequency signals in the abc frame appear as even-order harmonics in the dq frame, and vice versa. The $CDSC_{2,4,8,16,32}$ operator

in the dq frame passes all $32k$ harmonic order frequency signals, corresponding to harmonic order signals of $32k \pm 1$ in the abc frame. Therefore, the $CDSC_{2,4,8,16,32}$ operator in the dq frame effectively extracts the equivalent fundamental frequency component in the abc frame .

The total delay time of the $CDSC_{2,4,8,16,32}$ operator is $31T/32$. To reduce the total delay time to $15T/16$, a $CDSC_{2,4,8,16}$ operator is used. However, the $CDSC_{2,4,8,16}$ operator fails to eliminate all $16k$ harmonic frequency signals in the dq frame, corresponding to harmonic order signals of $16k \pm 1$ in the abc frame. As a result, when the $CDSC_{2,4,8,16}$ operator is fed to the SRF-PLL for grid synchronization, a lower bandwidth SRF-PLL is required compared to when $CDSC_{2,4,8,16,32}$ operator is fed to the SRF-PLL.

Additionally, the CDSC operator in the dq frame introduces a time delay into the control loop of the SRF-PLL. This in-loop delay can have an adverse effect on the dynamic performance of the PLL. To ensure high stability of the SRF-PLL, the equivalent of the CDSC operator in the dq frame should be relocated into the $\alpha\beta$ frame using the following expression [118].

$$\begin{bmatrix} DSC_n[v_{\alpha h}] \\ DSC_n[v_{\beta h}] \end{bmatrix} = \begin{bmatrix} \cos h^* \theta & -\sin h^* \theta \\ \sin h^* \theta & \cos h^* \theta \end{bmatrix} * \begin{bmatrix} DSC_n[v_{dh}] \\ DSC_n[v_{qh}] \end{bmatrix} \quad (3.6)$$

where, $DSC_n[v_{dqh}] = \frac{1}{2}[v_{dq}h(\omega t) + v_{dq}h(\omega t - T/n)]$, ω is the fundamental angular frequency, h is the harmonic order, $h^* = \pm h$ is the required positive sequence harmonic frequency component to be extracted by the CDSC operator. The positive sign ‘+’ is used for positive sequence signals, while the negative sign ‘-’ is used for negative sequence signals. The variable θ is defined as $\theta = \omega t$. The simplified expression of (3.6) can be written as below.

$$\begin{bmatrix} DSC_n[v_{\alpha h}] \\ DSC_n[v_{\beta h}] \end{bmatrix} = \frac{1}{2} \begin{bmatrix} v_{\alpha}h(\omega t) + v_{\alpha}h(\omega t - \frac{T}{n}) \cos \frac{2\pi h^*}{n} - v_{\beta}h(\omega t - \frac{T}{n}) \sin \frac{2\pi h^*}{n} \\ v_{\beta}h(\omega t) + v_{\beta}h(\omega t - \frac{T}{n}) \cos \frac{2\pi h^*}{n} + v_{\alpha}h(\omega t - \frac{T}{n}) \sin \frac{2\pi h^*}{n} \end{bmatrix} \quad (3.7)$$

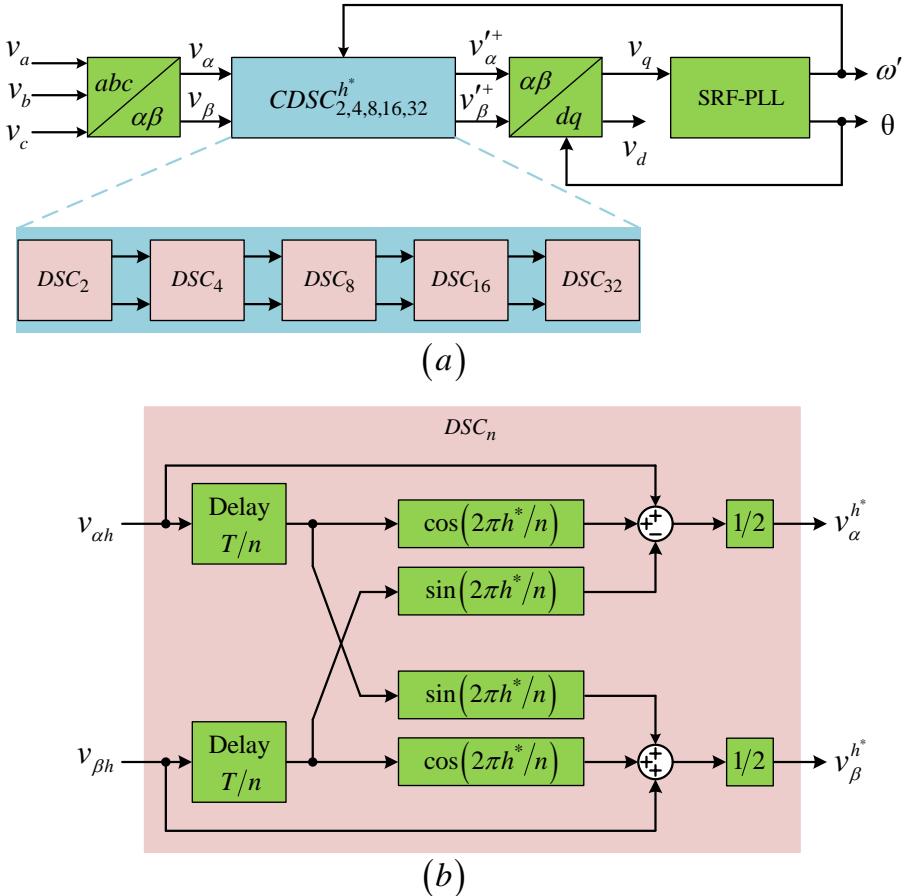


Figure 3.7: (a) General structure for frequency adaptive 3-ph CDSC-PLL, and (b) Time domain implementation of DSC_n operator

The CDSC operator is known for its efficiency in execution, as it involves simple operations such as transport delay, multiplication, and summation in the digital controller. However, it may encounter a small discretization error when non-integer samples are used for the delay operation in any DSC operator [117, 120]. To obtain integer samples for the delay operation, the total number of samples in a fundamental time period T must be chosen as an integer multiple of 32. In many applications, including aircraft power systems, the fundamental time period T is not constant and needs to be continuously updated for accurate delay operation. This update is achieved using a SRF-PLL, as depicted in Fig. 3.7. However, the updating of T may result in non-integer samples in the delay operation, leading to small discretization errors. To mitigate

this discretization error and enhance the performance of CDSC, a linear interpolation method is proposed in [117].

To transform the CDSC operator into a quadrature signal generator (QSG) suitable for single-phase systems, the concept of anticonjugate decomposition (ACD) is introduced in [123]. By utilizing this approach, the α component of the CDSC input is set to 0, while the actual single-phase signal is assigned to the β component. Consequently, the desired frequency signal and its quadrature signals are obtained at the β and α output terminals of the CDSC, respectively, with a 50% attenuation. This ACD-based CDSC configuration enables its application in single-phase systems, and the corresponding general diagram is illustrated in Fig. 3.8.

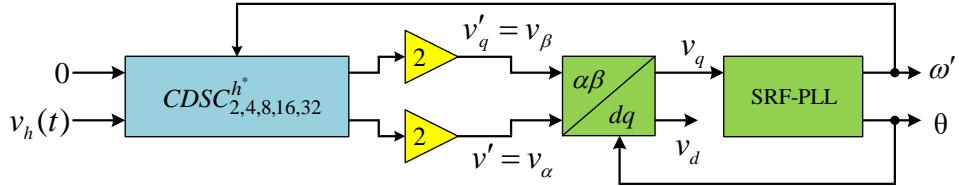


Figure 3.8: General structure for frequency adaptive 1-ph ACD-CDSC-PLL

3.2.3 Multiple Delayed Signal Cancellation Based PLL

The MDSC operator, introduced in [124], offers a reduced delay time and storage requirement compared to the CDSC operator. The MDSC operator delays the test signal multiple times using various delay times in such a way that the sum of the test signal and the delayed signals becomes zero. These delay times are chosen as integer multiples of $T/15$, ensuring that the delay does not exceed the fundamental time period T . The resulting operator, denoted as $MDSC_{15}$, has a total delay time of $14T/15$, which is shorter than the delay time of $CDSC_{2,4,8,16}$.

In the dq frame, the $MDSC_{15}$ operator eliminates all harmonic frequency signals except the $15k$ frequency signals, which correspond to $15k \pm 1$ frequency signals in the abc frame. Notably, $MDSC_{15}$ passes lower-order harmonics of 14 and 16, which are even,

whereas $CDSC_{2,4,8,16}$ passes odd harmonics of 15 and 17. Given that even harmonics are typically absent in power system applications, the bandwidth of the SRF-PLL can be chosen to be higher for $MDSC_{15}$ compared to $CDSC_{2,4,8,16}$, providing greater flexibility in SRF-PLL design.

The dq equivalent of $MDSC_{15}$ operator can be transformed onto the $\alpha\beta$ frame using the below equation.

$$\begin{bmatrix} MDSC_{15}[v_{\alpha h}] \\ MDSC_{15}[v_{\beta h}] \end{bmatrix} = \begin{bmatrix} \cos h^*\theta & -\sin h^*\theta \\ \sin h^*\theta & \cos h^*\theta \end{bmatrix} \begin{bmatrix} MDSC_{15}[v_{dh}] \\ MDSC_{15}[v_{qh}] \end{bmatrix} \quad (3.8)$$

Where,

$$MDSC_{15}[v_{dqh}] = \frac{1}{15} \sum_{l=0}^{14} [v_{dq}h(\omega t - Tl/15)].$$

The above expression is simplified as given below.

$$\begin{bmatrix} MDSC_{15}[v_{\alpha h}] \\ MDSC_{15}[v_{\beta h}] \end{bmatrix} = \frac{1}{15} \begin{bmatrix} v_{\alpha}h(\omega t) + \sum_{l=0}^{14} \left\{ v_{\alpha}h(\omega t - \frac{Tl}{15}) \cos \frac{2\pi h^* l}{15} - v_{\beta}h(\omega t - \frac{Tl}{15}) \sin \frac{2\pi h^* l}{15} \right\} \\ v_{\beta}h(\omega t) + \sum_{l=0}^{14} \left\{ v_{\beta}h(\omega t - \frac{Tl}{15}) \cos \frac{2\pi h^* l}{15} + v_{\alpha}h(\omega t - \frac{Tl}{15}) \sin \frac{2\pi h^* l}{15} \right\} \end{bmatrix} \quad (3.9)$$

3.3 PERFORMANCE EVALUATION OF ADVANCED PLLs

To assess the individual performance of the DSOGI, $CDSC_{2,4,8,16}$, and $MDSC_{15}$ operators under different grid conditions, MATLAB simulations are conducted with the same bandwidth settings for their respective SRF-PLLs. The evaluation of these advanced PLLs is primarily based on the accuracy of tracking the frequency, f in the SRF-PLL. A high-quality PLL is characterized by zero steady-state error in the phase angle extracted by the PLL when subjected to a ripple-free frequency input applied to the PLL's integrator. The performance evaluation aims to determine the ability of these advanced PLLs to achieve precise frequency tracking with minimal error.

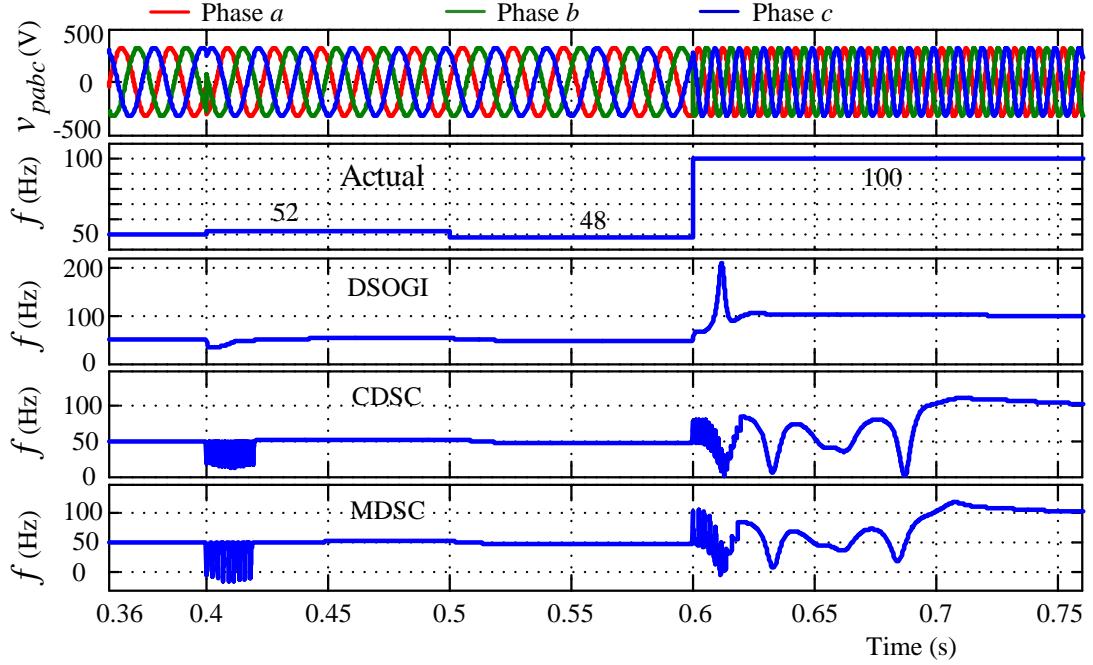


Figure 3.9: Simulation results: Frequencies of advanced PLLs under grid frequency variations

3.3.1 Frequency Jump

The frequency of the system is manipulated in the simulation to evaluate the performance of the DSOGI, CDSC_{2,4,8,16}, and MDSC₁₅ PLLs. Initially, the frequency is increased from 50 Hz to 52 Hz at $t = 0.4$ s, then it is decreased to 48 Hz at $t = 0.5$ s, and finally, it rapidly rises to 100 Hz at $t = 0.6$ s, as depicted in Fig. 3.9.

Analyzing the frequency variation of the PLLs, it can be observed that for a significant jump in frequency, all PLLs exhibit good steady-state tracking performance. However, the DSOGI-PLL demonstrates superior tracking speed compared to the other two PLLs. On the other hand, for small changes in frequency, all PLLs exhibit similar tracking accuracy and speed.

3.3.2 Voltage Disturbances without Harmonics

The balanced voltage sag of 0.5 pu is introduced from time $t = 0.4$ s to $t = 0.5$ s as shown in Fig. 3.10. And, the unbalanced voltage sag is introduced from time $t = 0.5$ s

to $t = 0.6$ s and the per unit voltages of phases a , b and c are respectively 1, 1 and 0.5. From the figure, it can be concluded that although all PLLs exhibit good steady-state performance, CDSC and MDSC based PLLs have better transient performance in terms of overshoot and settling time. The similar response is noticed during both balanced and unbalanced voltage swell conditions as shown in Fig. 3.11. The balanced voltage swell of 1.2 pu is introduced at time $t = 0.6$ s and the unbalanced voltage swell in phase- a ($v_{pa} = 1.2$ pu) is introduced at $t = 0.7$ s.

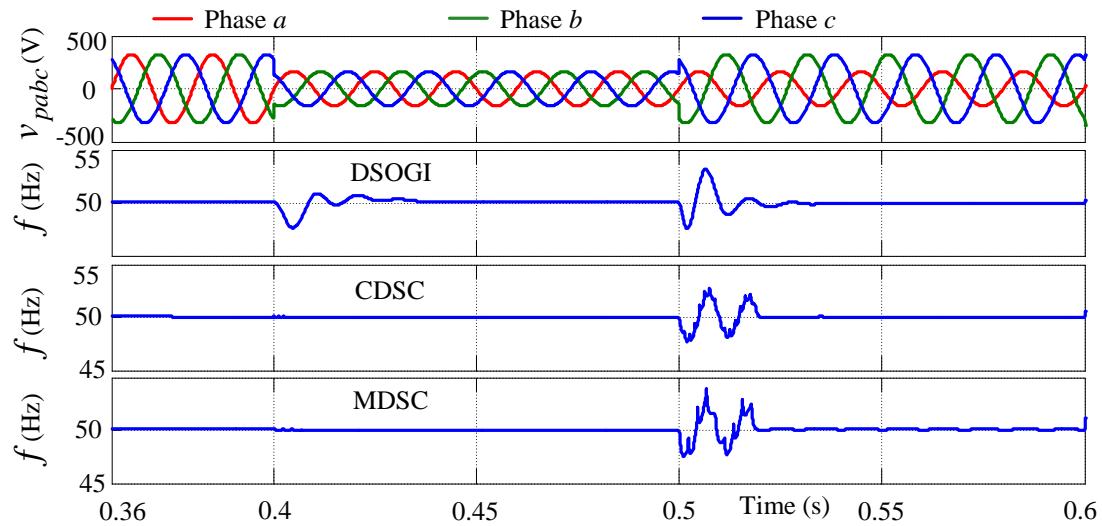


Figure 3.10: Simulation results: Frequencies of advanced PLLs under voltage sag conditions

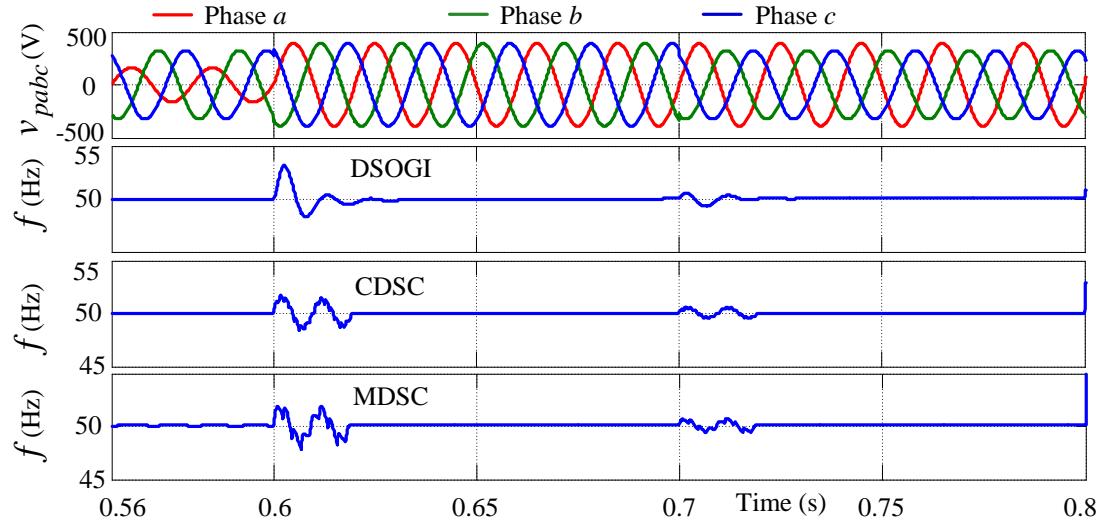


Figure 3.11: Simulation results: Frequencies of advanced PLLs under voltage swell conditions

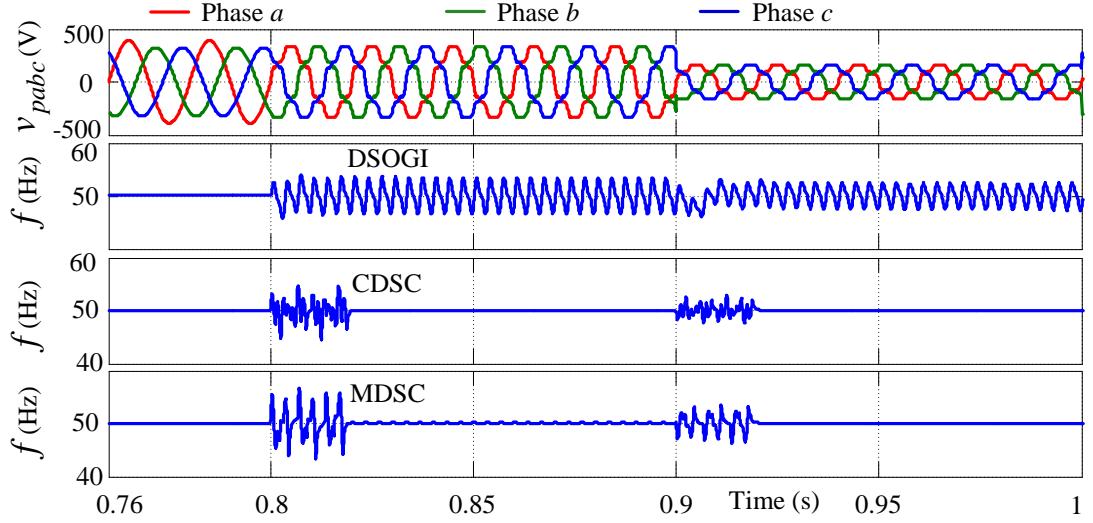


Figure 3.12: Simulation results: Frequencies of advanced PLLs under balanced voltage sag conditions with harmonics

3.3.3 Voltage Disturbances with Harmonics

The percentage of unbalance in the fundamental voltage remains the same as in the previous case. Additionally, 5th, 7th, 11th, and 13th harmonics are added to the voltage waveform, resulting in a total harmonic distortion (THD) of approximately 14%. This is depicted in Figs. 3.12-3.14. The nominal voltage with harmonics at $t = 0.8$ s and balanced voltage sag with harmonics at $t = 0.9$ s are introduced, as shown in Fig. 3.12. The unbalanced voltage sag with harmonics at $t = 1$ s and balanced voltage swell with harmonics at $t = 1.1$ s are introduced, as shown in Fig. 3.13. The unbalanced voltage swell with harmonics is introduced at $t = 1.2$ s, as shown in Fig. 3.14. In all these cases, the ripple in frequency is observed only for DSOGI, indicating an error in its phase angle tracking. Therefore, the performance of CDSC and MDSC is superior to DSOGI in the presence of harmonics. The CDSC experiences less ripple in magnitude compared to MDSC.

3.3.4 Phase Angle Jump

In the given scenario, a maximum jump in phase angle of 180° is set at time $t = 0.4$ s as shown in Fig. 3.15(a). The enlarged view of Fig. 3.15(a) is shown in Fig. 3.15(b)

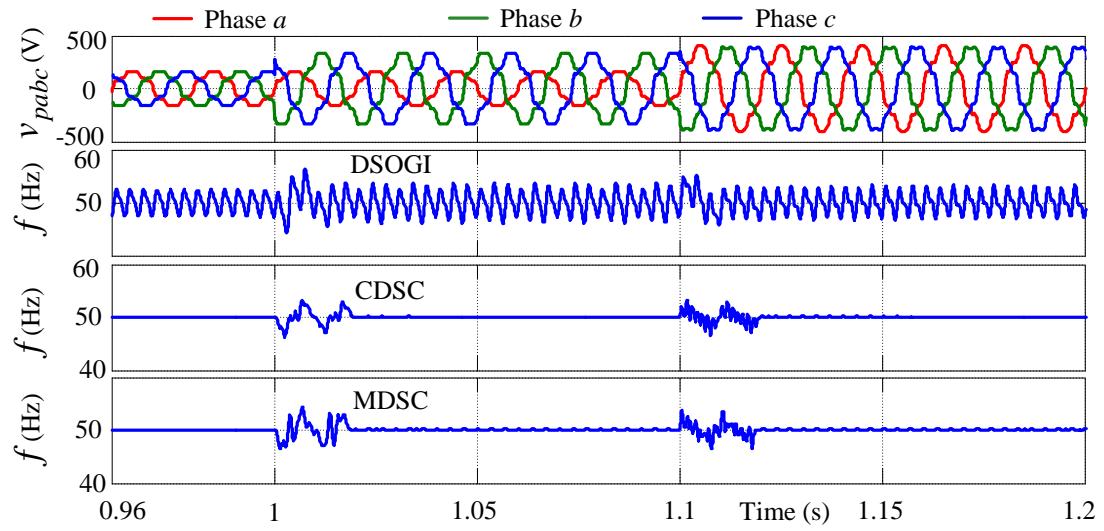


Figure 3.13: Simulation results: Frequencies of advanced PLLs under unbalanced voltage sag and balanced voltage swell conditions with harmonics

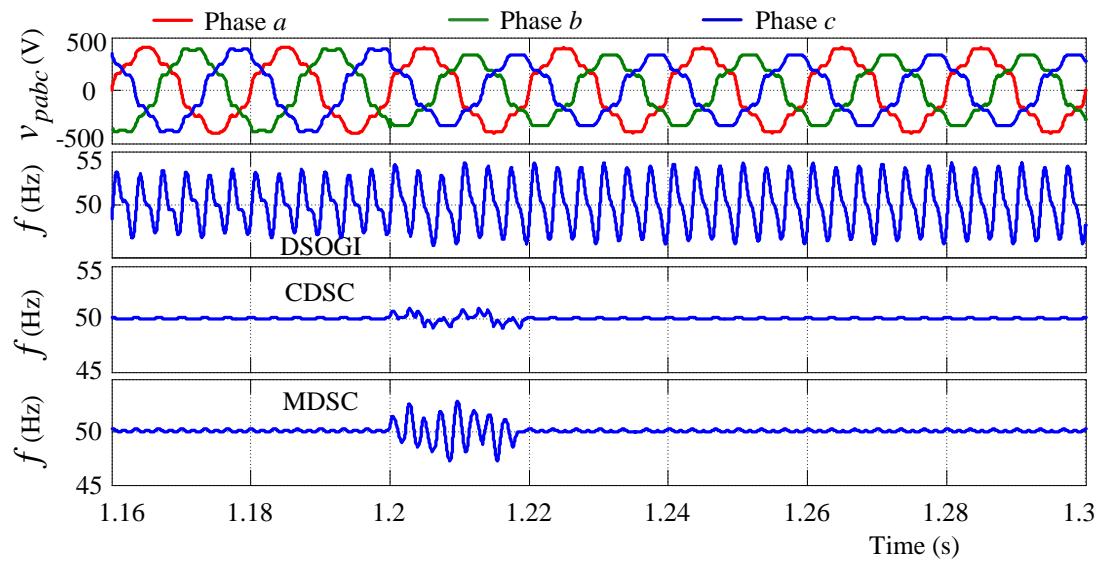


Figure 3.14: Simulation results: Frequencies of advanced PLLs under unbalanced voltage swell condition with harmonics

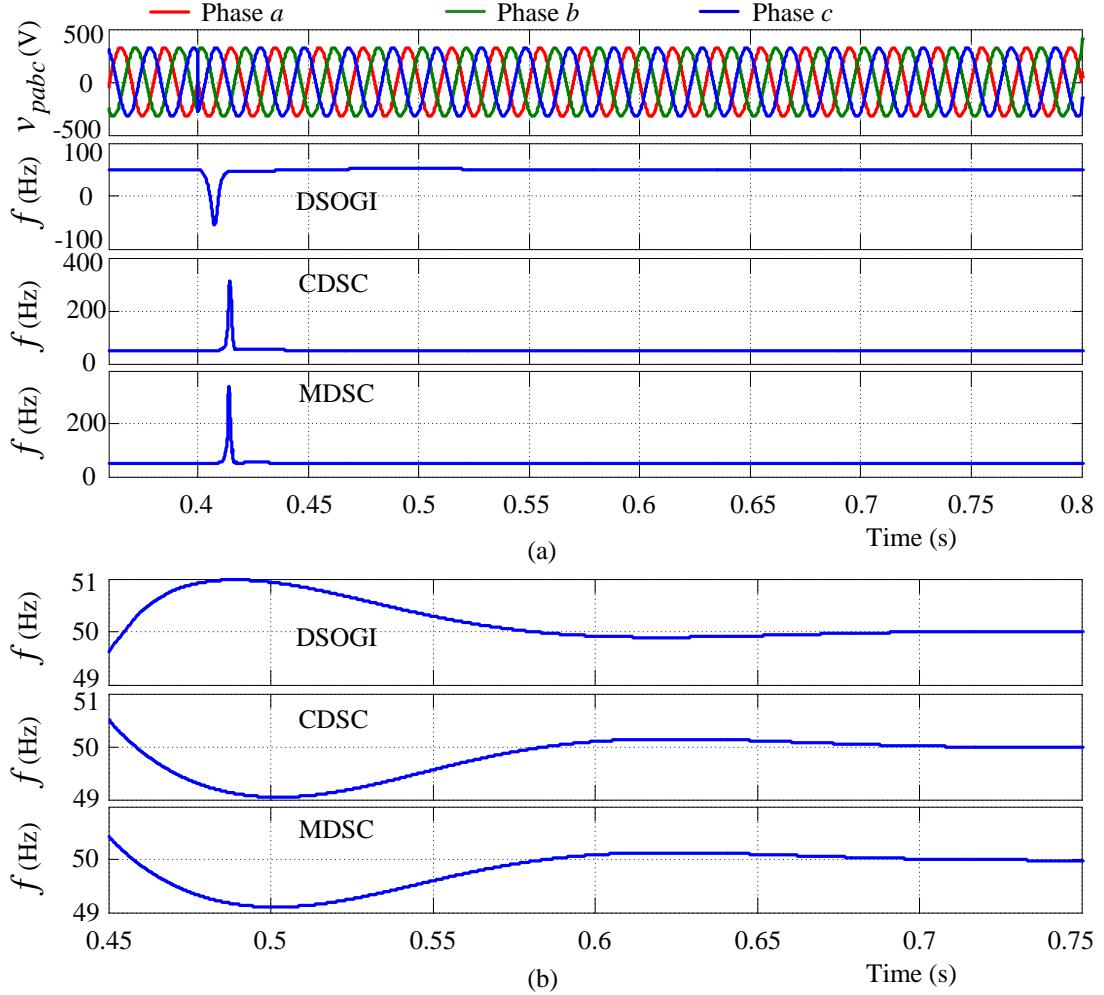


Figure 3.15: Simulation results: (a) Frequencies of advanced PLLs under voltage phase jump of 180° , and (b) Enlarged view of (a)

to observe the settling time and peak over/undershoot magnitudes. It is observed that all the PLLs exhibit similar response during phase jump. All the PLLs show no ripple in frequency at steady-state. Therefore, the phase angle tracking performance of these PLLs is not affected by the phase angle jump, indicating their ability to accurately track the phase angle under such conditions.

3.3.5 Presence of DC Components

In the scenario where the grid voltages are sensed and processed in a controller for power electronic converter control, it is possible for DC components to be added to

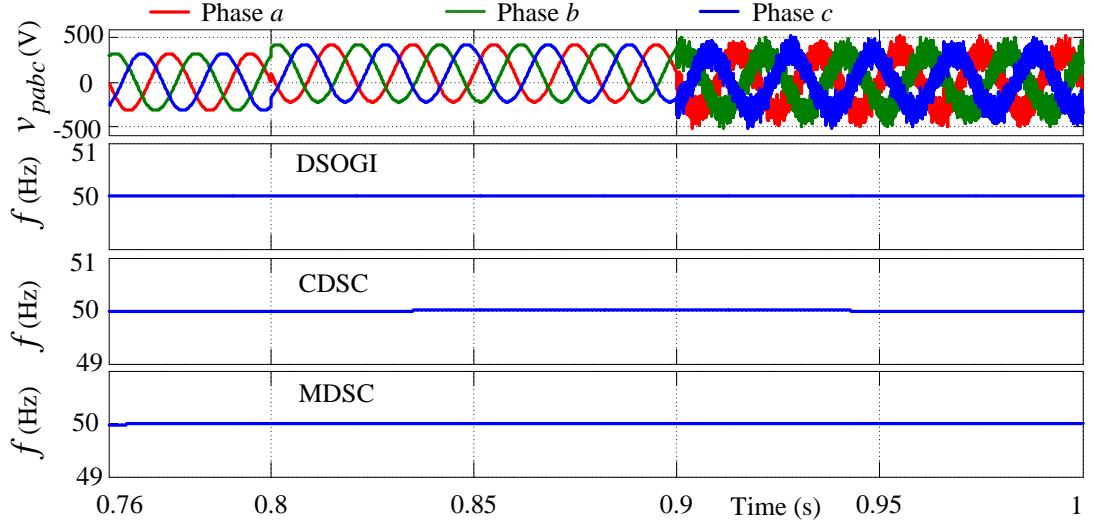


Figure 3.16: Simulation results: Frequencies of advanced PLLs under voltage with DC offset and voltage distortion conditions

the sensed values. In this case, the performance of PLLs is evaluated for the presence of DC components in the fundamental balanced voltages, as shown in Fig. 3.16 from time $t = 0.8\text{ s}$ to $t = 0.9\text{ s}$. It can be observed that all the PLLs provide ripple free frequency, consequently, the performance of all PLLs in tracking the phase angle remains satisfactory even in the presence of DC offsets in the three-phase PCC voltages.

3.3.6 Voltage Distortions

In the given scenario, distorted balanced voltages are applied from time $t = 0.9\text{ s}$ to $t = 1\text{ s}$, as shown in Fig. 3.16. It can be observed that the distortions in the voltage waveforms do not have any significant effect on the frequency, as there is no visible ripple in the frequency response of all PLLs. Consequently, the performance of all PLLs in tracking the phase angle remains satisfactory even in the presence of distorted unbalanced voltages.

It is important to note that the change in frequency even during the transients must be within the allowable range. This allowable frequency threshold is generally quite less unlike in this simulation study. However, this study is presented to understand the

behavior of three different operators DSOGI, CDSC and MDSC. To limit the frequency change to the allowable threshold, a special attention is required in the design of SRF-PLL but not in the design of these three operators.

3.4 SUMMARY

In this chapter, a comprehensive review of advanced PLLs, including SOGI, CDSC, and MDSC based PLLs, is presented for the accurate extraction of FFPS components. MATLAB simulations are conducted to evaluate the performance of these PLLs under various grid conditions.

The SOGI-based PLL exhibits attenuation of harmonics but fails to completely nullify them, resulting in unsatisfactory phase angle tracking performance in the presence of harmonics and DC components in grid voltages. On the other hand, the CDSC and MDSC based PLLs employ delay operators that are carefully chosen to completely eliminate specific sets of harmonics. As a result, the performance of CDSC and MDSC based PLLs is found to be satisfactory for all grid conditions, as long as the grid does not have dominant harmonics that cannot be eliminated by these PLLs.

Based on these findings, it is concluded that CDSC and MDSC based PLLs are more preferable than SOGI based PLL for power system applications. These advanced PLLs provide improved performance in terms of accurate phase angle tracking, making them suitable choices for custom power devices. In comparison to MDSC, the CDSC operator requires fewer delay operations, making it computationally less intensive. Therefore, the CDSC operator will be employed in the following chapters for controlling custom power devices.

CHAPTER 4

DESIGN OF A DECOUPLED SLIDING MODE CONTROL FOR FOUR-LEG DISTRIBUTION STATIC COMPENSATOR

4.1 INTRODUCTION

In the previous chapters, the performance characteristics of dual-output converter based UPQC and its control are presented. The control scheme for DOC should incorporate the control of neutral-point voltage (NPV) or common mode voltage (CMV) in addition to the control of inverter currents or voltages. It is also well known that the UPQC is a combination of DSTATCOM and DVR. As an initial step, the control scheme which incorporates the control of NPV is developed for DSTATCOM, later this is applied for shunt terminal of DOC based UPQC in Chapter 6.

It is common that three-phase four-wire distribution system experiences unbalance in the load or source, which results in an increased neutral current, thereby resulting in increased power loss and undesirable operation of loads. To control the neutral current or zero sequence and DC currents, the four-leg voltage source converter (FL-VSC) is the best-suited topology as it requires lower DC-link voltage, smaller DC-link capacitor, and simpler control requirement compared to split capacitor three-phase four-wire inverter [125–127].

For efficient performance of DSTATCOM, an appropriate algorithm comprising the generation of compensator reference currents, and the controller is required. Various theories are discussed in Chapter 2 for the generation of compensator reference currents. It is also discussed that designing the complete control algorithm in the natural reference frame (*abc* frame) makes it insensitive to the signal transformation errors and free from

computational burden to some extent. Nonlinear controllers are best choice in the abc frame as their reference tracking capability is unaltered irrespective of the signal frequency. In this chapter, the sliding mode controller is considered due to its robustness against model inaccuracies and lesser computational burden on digital processor as compared to the model predictive controller. Also among the theories presented in Chapter 2, ISCT is the only choice to design in abc frame. There are other theories in the literature such as least-mean-square (LMS) method [126, 128], variable forgetting factor recursive least square (VFFRLS) [129] and kernel incremental meta-learning (KIM) [130] algorithms for generation of compensator reference currents in abc frame. However, ISCT is considered in this chapter due to its less computation requirement.

In the natural reference frame, the current dynamics of a DSTATCOM are coupled through converter pole voltages due to either load neutral-point voltage (NPV) or filter inductance of the converter fourth-leg. This coupling among a, b, c phases leads to cross-coupling in the sliding variable equations with respect to four manipulated input variables, when the conventional sliding surface is chosen. This is why, the controller is generally implemented either in $\alpha\beta$ or dq or $\gamma\theta$ frame [44, 45, 131], thereby the coupling effect is avoided. Further, in the conventional SMC and hysteresis current control (HCC) schemes, the currents through the four legs of a DSTATCOM converter are controlled based on corresponding phase current error. However, the four currents in a four-wire system can not be independently controlled variables and hence the role of one of the four controllers is redundant in the conventional control schemes. Considering the coupling issue and the controller redundancy, in this chapter, a new sliding surface is proposed in the natural reference frame itself to get a decoupled feature with respect to the manipulated inputs. It is ensured that the proposed sliding surface is a function of load NPV, thereby the control of NPV is achieved which is useful for the control of DOC based UPQC.

Finally, the performance of a DSTATCOM with the proposed control scheme under

various operating conditions is demonstrated through detailed simulation study and validated with experimental results obtained from a laboratory prototype of the four-leg DSTATCOM.

4.2 SYSTEM MODELING AND CONVENTIONAL SLIDING MODE CONTROL

The figure provided in Fig. 4.1 depicts the schematic of a DSTATCOM with a four-leg voltage source converter, which is connected to a three-phase four-wire distribution system. In this section, the mathematical model of a four-leg DSTATCOM in the natural reference frame is reviewed. The objective is to analyze the presence of cross-coupling in the sliding variable equations in relation to the four manipulated input variables.

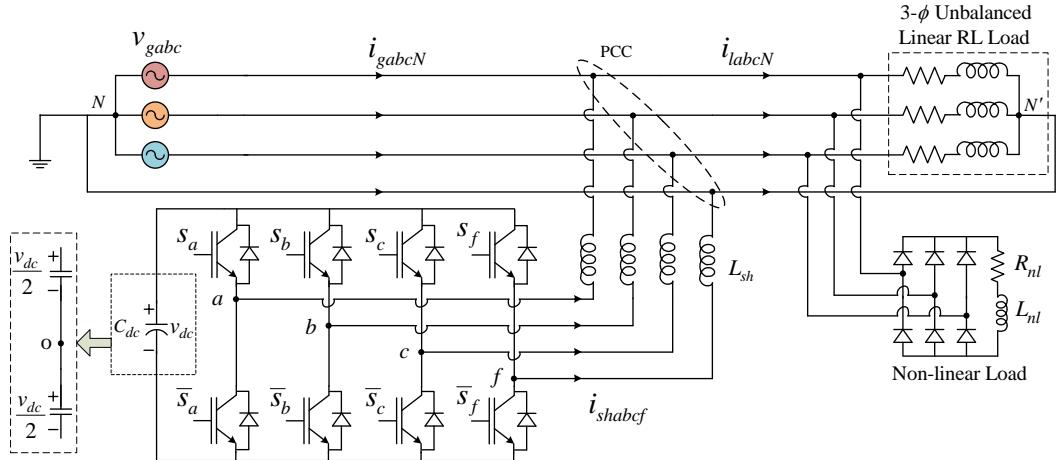


Figure 4.1: Schematic diagram of four-leg voltage source converter based DSTATCOM

4.2.1 Modeling of Four-leg DSTATCOM

To gain a better understanding of the system's dynamic equations given below, Fig. 4.1 illustrates the extended split capacitor-based DC-link configuration.

$$v_{jo} = L_{sh} \frac{di_{shj}}{dt} + v_{gj} + v_{No} + d_j \quad (4.1)$$

$$i_{shf} = - \sum_{i=\{a,b,c\}} i_{shi}$$

Where $j \in \{a, b, c, f\}$, v_{jo} is the pole voltage of four-leg converter, measured disturbance (v_{gj}) is grid voltage, controlled variable (i_{shj}) and L_{sh} are current and filter inductance

of DSTATCOM respectively. Note that $v_{gf} = 0$ and unmeasured disturbance (d_j) represents the un-modeled dynamics, model mismatch, and variations in model parameters and signal estimations. The load NPV, v_{No} is the voltage between grid neutral ‘ N ’ or load neutral ‘ N' to the DC-link midpoint ‘ o ’. The expression for load NPV is obtained by summing up all pole voltages of (4.1).

$$v_{No} = \frac{1}{4} \sum_j (v_{jo} - v_{gj} - d_j) \quad (4.2)$$

The pole voltage, v_{jo} , always remains within the limits of $\pm 0.5v_{dc}$, where v_{dc} represents the voltage of the DC-link capacitor. Mathematically, this constraint can be expressed as $v_{jo} = u_j \frac{v_{dc}}{2}$, where u_j is a manipulated input variable. Specifically, when the top switch of the j^{th} leg (S_j) is turned ON and its corresponding bottom switch (\bar{S}_j) is turned OFF, u_j is assigned a value of +1. Conversely, when the top switch is OFF and the bottom switch is ON, u_j is assigned a value of -1. With this understanding, (4.2) can be modified as follows.

$$v_{No} = \frac{1}{4} \sum_j \left(\frac{v_{dc}}{2} u_j - v_{gj} - d_j \right) \quad (4.3)$$

Taking into account the constraint that the four-wire system has only three independent controlled currents and substituting (4.2) into (4.1), the following expression is obtained.

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} 2 & 1 & 1 \\ 1 & 2 & 1 \\ 1 & 1 & 2 \end{bmatrix} L_{sh} \begin{bmatrix} \dot{i}_{sha} \\ \dot{i}_{shb} \\ \dot{i}_{shc} \end{bmatrix} + \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} + \begin{bmatrix} d_a - d_f \\ d_b - d_f \\ d_c - d_f \end{bmatrix} + v_{fo} \quad (4.4)$$

The controller determines the values of the three converter pole voltages based on the dynamics of three independent currents when the value of v_{fo} is known. Typically, v_{fo} is set to zero by switching the fourth leg at a user-defined frequency with a 50% duty cycle

[132]. However, in some studies, v_{fo} is deliberately considered as a triplen harmonic signal. This configuration allows for the utilization of space vector modulation using carrier-based pulse-width modulation (PWM), providing additional advantages [133].

4.2.2 Conventional SMC

In the conventional sliding mode control (SMC) or hysteresis current control (HCC), the sliding variable x_j is typically defined as the current error variable, as given below.

$$x_j = i_{shj} - i_{shj}^* \quad (4.5)$$

Where i_{shj}^* is compensator reference current. Based on the polarity of current error, the conventional control law/input is defined as given below.

$$u_j = -\text{sgn}(x_j) \quad (4.6)$$

Where $\text{sgn}(\cdot)$ is a signum function. If the defined control law satisfies the Lyapunov stability criteria, the system trajectory will ultimately converge to the sliding surface, $x_j = 0$ within a finite time.

To ensure global asymptotic stability according to the Lyapunov stability criteria, the Lyapunov function $V(x_j)$ must satisfy the following properties:

1. $V(x_j) = 0$ if and only if $x_j = 0$
2. $V(x_j) > 0$ if and only if $x_j \neq 0$
3. $\dot{V}(x_j) < 0 \quad \forall x_j \neq 0$

The time derivative of any signal, say $V(x_j)$ is denoted as $\dot{V}(x_j)$ in this paper. Now, the Lyapunov function is selected as below such that the first two properties are satisfied.

$$V(x_j) = \frac{1}{2}x_j^2 \quad (4.7)$$

To verify the final property, the condition below needs to be satisfied.

$$\dot{V}(x_j) = x_j \dot{x}_j < 0 \quad (4.8)$$

By substituting the derivative of sliding variable using (4.4) and (4.5) into (4.8), the following is obtained.

$$\dot{V}(x_j) = x_j \frac{1}{4L_{sh}} \left\{ \left[3 \left(u_j \frac{v_{dc}}{2} - v_{gj} - d_j \right) - \sum_{\substack{i=\{a,b,c,n\} \\ i \neq j}} \left(u_i \frac{v_{dc}}{2} - v_{gi} - d_i \right) \right] - 4L_{sh} \dot{i}_{shj}^* \right\} < 0 \quad (4.9)$$

The condition mentioned above can be satisfied by selecting appropriate manipulated input variables (u_a, u_b, u_c, u_f). It is evident from (4.9) that the dynamics of the sliding variable in a specific phase are coupled with the manipulated input variables of other phases. In other words, in order to generate a switching pulse for the converter switches of the phase- a leg, the controller relies on the state of switches in the other three legs. To achieve a decoupled characteristic in terms of the manipulated variables, a new sliding variable is introduced in this chapter.

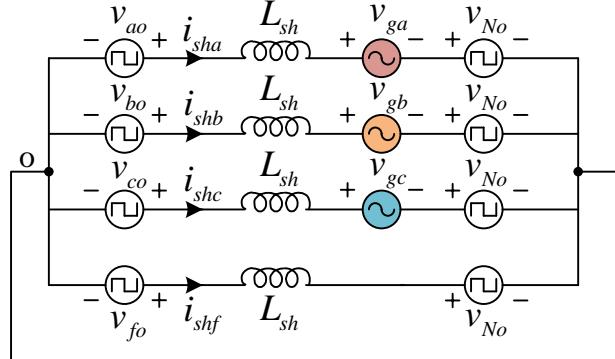
4.3 PROPOSED SLIDING MODE CONTROL SCHEME

In this section, the system dynamic equations considering four independent controlled variables and the design of a decoupled sliding mode control are presented.

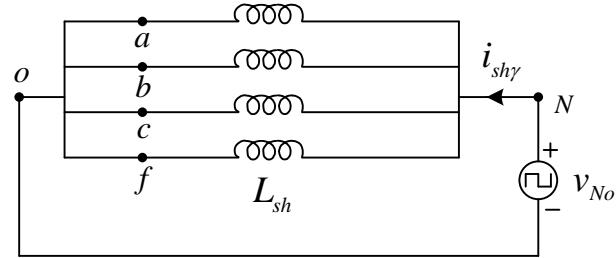
The equivalent circuit of four-leg DSTATCOM based on (4.1) is shown in Fig. 4.2(a). The Thevenin's equivalent impedance observed at the load NPV terminals is shown in Fig. 4.2(b). The current due to Thevenin's equivalent load NPV, $i_{sh\gamma}$ is given as,

$$i_{sh\gamma} = \frac{4}{L_{sh}} \int v_{No} dt. \quad (4.10)$$

By substituting (4.10) in (4.1), the model equations with four independently controlled



(a)



(b)

Figure 4.2: Four-leg DSTATCOM system: (a) Equivalent circuit, and (b) Thevenin's equivalent impedance seen by load NPV terminals

variables as given below.

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \\ v_{fo} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0.25 \\ 0 & 1 & 0 & 0.25 \\ 0 & 0 & 1 & 0.25 \\ -1 & -1 & -1 & 0.25 \end{bmatrix} L_{sh} \begin{bmatrix} \dot{i}_{sha} \\ \dot{i}_{shb} \\ \dot{i}_{shc} \\ \dot{i}_{sh\gamma} \end{bmatrix} + \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \\ 0 \end{bmatrix} + \begin{bmatrix} d_a \\ d_b \\ d_c \\ d_f \end{bmatrix} \quad (4.11)$$

Although the fourth controlled variable, $i_{sh\gamma}$ is a function of load NPV, the load NPV (v_{No}) can be estimated using (4.3) under the assumption that $d_j = 0$. However, it is important to consider the mismatch in the estimation of v_{No} and include it in the system dynamic equations presented in (4.11). In the conventional DSTATCOM control algorithms, the measurement of grid and DC-link voltages is necessary. Therefore, the proposed algorithm does not require an additional sensor for measuring v_{No} .

4.3.1 SMC Derivation

In general, the sliding surface is determined based on the controlled variables. From (4.11), it is evident that the converter pole voltage of each phase is influenced by the dynamics of the corresponding phase current and $i_{sh\gamma}$. By selecting a sliding surface for each phase as a combination of the respective phase current and $0.25i_{sh\gamma}$, a decoupled characteristic can be achieved with respect to the manipulated inputs. Therefore, the sliding variable is defined as follows.

$$\sigma_j = (i_{shj} + 0.25i_{sh\gamma}) - (i_{shj}^* + 0.25i_{sh\gamma}^*) \quad (4.12)$$

The sliding surface is defined as $\sigma_j = 0$. The process of generating compensator reference current (i_{shj}^*) and the reference current due to load NPV ($i_{sh\gamma}^*$) is explained later in this section. To verify the Lyapunov stability condition stated in (4.8), the derivative of sliding variable ($\dot{\sigma}_j$) is calculated using (4.1), (4.10), (4.11), and (4.12).

The expression for the derivative is given below.

$$\begin{aligned} \dot{\sigma}_j &= \frac{1}{L_{sh}} \left\{ v_{jo} - (L_{sh} \dot{i}_{shj}^* + v_{gj} + v_{No}^*) - d_j \right\} \\ &= \frac{1}{L_{sh}} \left\{ u_j \frac{v_{dc}}{2} - v_{jo}^* - d_j \right\} \end{aligned} \quad (4.13)$$

Where $i_{shf}^* = -\left(\sum_{i=a,b,c} i_{shi}^*\right)$ and v_{No}^* is the load NPV reference. Equation (4.13) clearly demonstrates that the dynamics of sliding variable associated with a specific phase is entirely decoupled from the manipulated inputs of the other phases. This decoupling property is advantageous for controller design as it allows for the independent evaluation of each component (a, b, c , and f) of the four-leg voltage source converter.

The conventional control law defined in (4.6) can result in variable and high switching frequency, a phenomenon known as chattering. To mitigate chattering and achieve fixed switching frequency operation, an equivalent control law on the sliding mode can be

derived by solving the invariance condition, $\dot{\sigma}_j = 0$ [134]. By solving the invariance condition $\dot{\sigma}_j = 0$, the resultant equivalent voltage reference signal (v_{jo}^{eq}) can be obtained as follows.

$$v_{jo}^{eq} = v_{jo} = (L_{sh}\dot{i}_{shj}^* + v_{gj} + v_{No}^*) + d_j \quad (4.14)$$

In the above equation, it is not possible to compute v_{jo}^{eq} directly because the instantaneous value of d_j is unknown. To address this issue, the un-modeled dynamics (d_j) are replaced with a control law $[-kf(\sigma_j)]$, and the modified converter reference voltage (v_{jo}^{con}) is computed as given below,

$$v_{jo}^{con} = (L_{sh}\dot{i}_{shj}^* + v_{gj} + v_{No}^*) - kf(\sigma_j), \quad (4.15)$$

where k is the control gain and $f(\sigma_j)$ is generally a signum function. The signum function provides a high gain even when the state trajectory is close to the surface $\sigma_j = 0$. This causes the trajectory to move faster and enables it to cross the surface in less time. Consequently, the value of the signum function changes rapidly, resulting in multiple switchings within the designated switching period. To avoid these multiple switchings, the signum function is substituted with a hyperbolic tangent ($tanh$) function

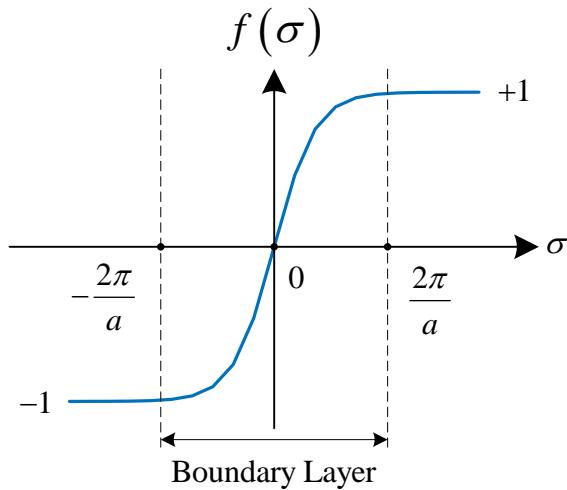


Figure 4.3: Hyperbolic tangent control law

as given below.

$$f(\sigma_j) = \tanh\left(\frac{a\sigma_j}{2}\right) \quad \forall a > 0 \quad (4.16)$$

In the above equation, the parameter a determines the width of the boundary layer for the \tanh function, as illustrated in Fig. 4.3. A lower value of a results in a smoother \tanh function, eliminating multiple switchings. This leads to reduced switching losses and improved switch lifespan. The proposed SMC computes the four reference voltages using (4.15) and compares them with a triangular carrier wave of user-defined frequency. This comparison generates the gate pulses for the four-leg DSTATCOM converter switches.

4.3.2 Selection of The Proposed SMC Parameters

Based on Lyapunov stability criteria, the parameters of equivalent control concept of SMC are selected. To verify the stability condition given in (4.8), the derivative of sliding variable $\dot{\sigma}_j$ is obtained as below by substituting v_{jo} of (4.13) with v_{jo}^{con} of (4.15).

$$\begin{aligned} \dot{\sigma}_j &= \frac{1}{L_{sh}} \left\{ -kf(\sigma_j) - d_j \right\} \\ &= -\frac{k}{L_{sh}} \tanh\left(\frac{a\sigma_j}{2}\right) - \frac{d_j}{L_{sh}} \end{aligned} \quad (4.17)$$

Substituting (4.17) into (4.8) gives,

$$\begin{aligned} \dot{V}(\sigma_j) &= -\frac{k}{L_{sh}} \sigma_j \tanh\left(\frac{a\sigma_j}{2}\right) - \sigma_j \frac{d_j}{L_{sh}} \\ &\leq \frac{|\sigma_j|}{L_{sh}} \left\{ |d_j| - k \operatorname{sgn}(\sigma_j) \tanh\left(\frac{a\sigma_j}{2}\right) \right\}. \end{aligned} \quad (4.18)$$

For a system trajectory beyond the boundary layer, $\operatorname{sgn}(\sigma_j) \tanh\left(\frac{a\sigma_j}{2}\right) = 1$ and as a result, (4.18) becomes similar to that of the signum function, as given below:

$$\dot{V}(\sigma_j) \leq \frac{|\sigma_j|}{L_{sh}} \left\{ |d_j| - k \right\}. \quad (4.19)$$

When the value of k is chosen to be greater than the estimated uncertainties $|d_j|$, the final property of Lyapunov stability criteria, $\dot{V}(\sigma_j) < 0$, is satisfied. This ensures global asymptotic stability. However, inside the boundary layer, this stability property fails for the same value of k , as $k \operatorname{sgn}(\sigma_j) \tanh\left(\frac{a\sigma_j}{2}\right) < |d_j|$. This means that the controller loses its robustness within the boundary layer, and the system dynamics become unpredictable. Consequently, state trajectories always converge to the boundary layer, but they may or may not converge to the surface $\sigma_j = 0$. In a pessimistic scenario where state trajectories always diverge within the boundary layer, a steady-state error proportional to the width of the boundary layer arises. It can be inferred that a higher value of a leads to a lower steady-state error. However, increasing the parameter a also increases the number of switchings within the designed switching period, as explained in Section 4.3.1. Therefore, the selection of a involves a trade-off between tracking error and multiple switchings.

4.3.3 Generation of Compensator Reference Quantities and Switching Pulses

The reference compensator currents are generated using instantaneous symmetrical component theory (ISCT) [94] as given below,

$$i_{shj}^* = i_{lj} - \frac{v_{g1j}^+}{\sum_{k=a,b,c} (v_{g1k}^+)^2} (P_{lavg} + P_{closs_avg}), \quad (4.20)$$

where P_{lavg} and P_{closs_avg} are average load power and converter power losses, respectively. The converter power loss is determined by the error in the DC-link voltage, which is regulated using a PI controller. To extract the fundamental positive sequence component of the grid voltages v_{g1j}^+ , the cascaded delayed signal cancellation (CDSC) operator, introduced in [116], is employed. The CDSC operator has been shown to outperform the commonly used second-order generalized integrator (SOGI) [135].

The reference current $i_{sh\gamma}^*$, corresponding to the Thevenin's equivalent load NPV, is determined by integrating v_{No}^* based on (4.10) and it is mathematically expressed as

below:

$$i_{sh\gamma}^* = \frac{4}{L_{sh}} \int v_{No}^* dt. \quad (4.21)$$

The load NPV reference v_{No}^* is a user-defined zero-sequence voltage that depends on the specific application of the converter. In certain cases, such as in a dual-output converter based power quality conditioner, v_{No}^* can be a positive DC offset for an upper port or a negative DC offset for a lower port [60]. Alternatively, in other applications, v_{No}^* can be chosen as triplen harmonics to take advantage of a space vector pulse width modulation (PWM) scheme using a simple carrier-based PWM scheme [133]. In this chapter, the proposed control scheme's performance is evaluated by considering both DC offset and triplen harmonics for v_{No}^* .

The generated reference quantities are utilized to compute the converter reference voltage v_{jo}^{con} using (4.15). These reference voltages are then fed into a sinusoidal pulse width modulator (SPWM) to generate gate pulses for the power switches of the four-leg DSTATCOM. The control block diagram of the proposed sliding mode control (SMC) scheme for the four-leg DSTATCOM is depicted in Fig. 4.4.

4.3.4 Design of Filter Inductance

The design of filter inductance (L_{sh}) is same as the conventional approaches as given below.

Consider an equivalent circuit of four-leg DSTATCOM as shown in Fig. 4.2(a). When the top switch of phase-*a* leg is turned ON, then the dynamic equation of DSTATCOM is defined as follows:

$$L_{sh} \frac{\Delta i_{sha}}{T_{on}} = \frac{v_{dc}}{2} - v_{ga} - v_{No}, \quad (4.22)$$

where T_{on} is the ON time of top switch, and Δi_{sha} is the change in phase-*a* current of DSTATCOM or DSTATCOM ripple current in phase-*a*. Similarly, when the top switch of phase-*a* leg is turned OFF, then the dynamic equation of DSTATCOM is defined as

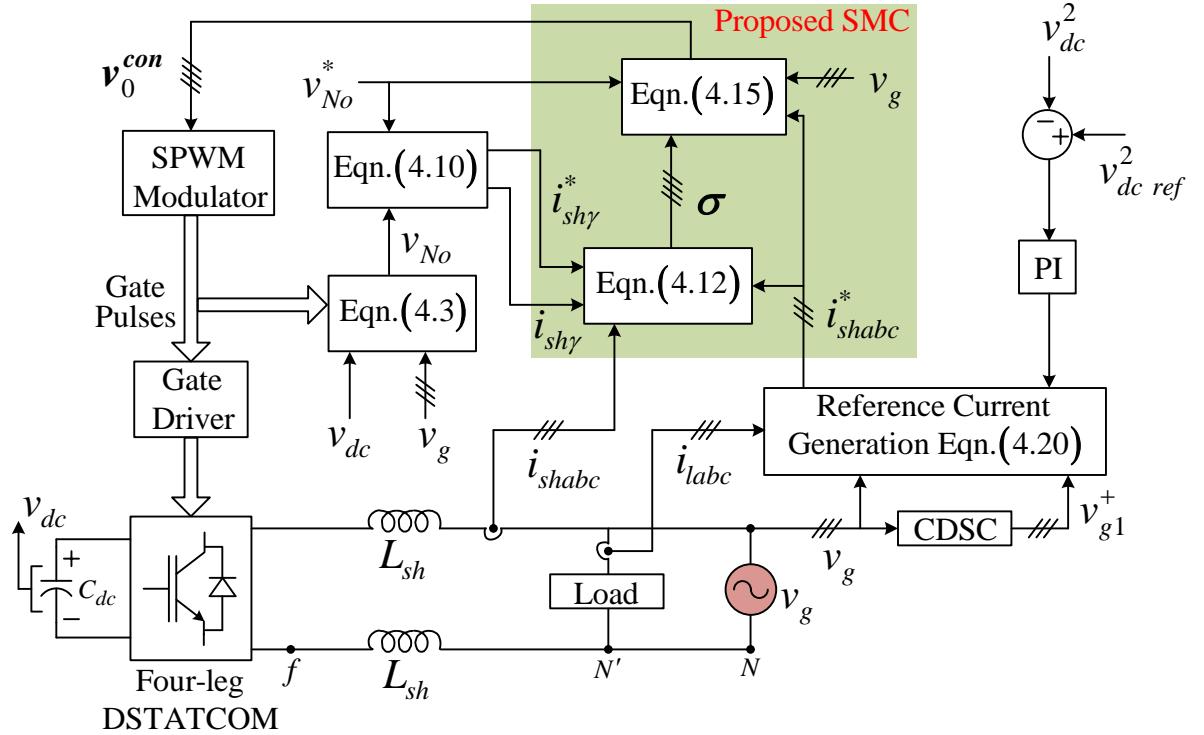


Figure 4.4: Block diagram of the proposed SMC control scheme for DSTATCOM

follows:

$$L_{sh} \frac{\Delta i_{sha}}{T_{off}} = \frac{v_{dc}}{2} + v_{ga} + v_{No}. \quad (4.23)$$

The duty ratio (D^*) of the sinusoidal pulse-width modulation (SPWM) scheme for the known or reference NPV is given as below.

$$D^* = 0.5 + \frac{v_{ga} + v_{No}^*}{v_{dc}} \quad (4.24)$$

Using (4.22), (4.23), and (4.24), the switching period (T_{sw}) is obtained as below.

$$\begin{aligned} T_{sw} &= T_{on} + T_{off} \\ &= L_{sh} \frac{\Delta i_{sha}}{v_{dc}} \left\{ \frac{1}{0.5 - \frac{v_{ga} + v_{No}}{v_{dc}}} + \frac{1}{0.5 + \frac{v_{ga} + v_{No}}{v_{dc}}} \right\} \\ &= L_{sh} \frac{\Delta i_{sha}}{v_{dc}} \left\{ \frac{1}{1 - D} + \frac{1}{D} \right\} \end{aligned} \quad (4.25)$$

From the above expression, the ripple in filter current (Δi_{sha}) is obtained as follows:

$$\Delta i_{sha} = \frac{v_{dc}(1 - D)D}{f_{sw}L_{sh}}, \quad (4.26)$$

where f_{sw} is the switching frequency. From (4.26), it is evident that the ripple current, Δi_{sha} is a function of duty ratio (D). Thus using maxima and minima concepts, the maximum value of ripple current, $(\Delta i_{sha})_{max}$ is found at $D = 0.5$. Substituting $D = 0.5$ in (4.26), the following is obtained.

$$L_{sh} = \frac{0.25 v_{dc}}{f_{sw}(\Delta i_{sha})_{max}} \quad (4.27)$$

This is the minimum value of inductance required for a maximum allowable peak to peak ripple current. The above expression evidences that the higher value of L_{sh} is required for low power loads and lower value for high power loads.

Now as per IEEE standard 519-2014, the total current demand distortion for a $I_{sc}/I_L < 20$ is 5%. I_{sc} refers to short circuit current and I_L is the nominal load current. Therefore, $(\Delta i_{sha})_{max}$ is considered as $0.05 \times i_{shp}$, where i_{shp} is the peak of rated filter current, i.e., peak of the load current for DSTATCOM study.

4.4 SIMULATION STUDIES

The simulation study presented in [136] focuses on the hysteresis current control for a four-leg DSTATCOM, utilizing the system parameters specified in Table 4.1. For effective validation of the proposed SMC, a simulation study is carried out in this chapter using the same system parameters given in Table 4.1. Both the HCC and proposed SMC control schemes are evaluated with a simulation step time of 10 μ s. The DC-link voltage controller gains in the proposed system are computed based on a fast-acting DC-link voltage controller described in [137]. The controller gains are determined as follows: $k_p = 0.0525$ and $k_i = 0.026$. These values are chosen to

Table 4.1: System parameters for simulation study

System parameters	Values
Base quantities	$S_b = 16 \text{ kVA}$, $V_b = 230 \text{ V}$ (L-N RMS)
Filter parameters	$L_{sh} = 22.5 \text{ mH}$
DC-link voltage	$V_{dc} = 900 \text{ V}$
DC-link capacitor	$C_{dc} = 1050 \mu\text{F}$
Linear load (full load)	$Z_a = 100 + j30 \Omega$ $Z_b = 30 + j27.5 \Omega$ $Z_c = 15 + j12.5 \Omega$
Nonlinear load (full load)	3- ϕ diode bridge rectifier with $R_{nl} = 20 \Omega$, $L_{nl} = 0.25 \text{ H}$

achieve the desired performance of the DC-link voltage control loop in the system. In the process of selecting the SMC parameters, a simulation is initially performed using a signum function to assess the presence of uncertainties in the model. Satisfactory results are obtained with a signum function when the parameter k is set to 15 or higher. The value of k is chosen as the minimum value that yields satisfactory results, which in this case is $k = 15$. Once the value of k is determined, the signum function is replaced with a hyperbolic tangent (\tanh) function. The parameter a of the \tanh function is then varied to achieve limited multiple switchings. In the simulation, it is observed that reduced multiple switchings occur when $a = 10$. Therefore, for the proposed SMC in the simulation, the parameters are chosen as $k = 15$ and $a = 10$ to achieve satisfactory performance with limited multiple switchings.

In Figs. 4.5-4.6, various waveforms and frequency spectra are presented to validate the performance of the proposed SMC for the four-leg DSTATCOM. The waveforms are expressed in per unit (p.u.) with respect to base values, while the load NPV and sliding variables are shown in their actual units. The base values are considered as 16 kVA (3-ph) and 230 V (L-N RMS).

Fig. 4.5 depicts the transition of grid voltages from a normal condition to a distorted condition at $t = 1 \text{ s}$. In this simulation, the reference load NPV v_{No}^* is set as a triplen harmonic signal. On the other hand, Fig. 4.6 shows the case where v_{No}^* is set to zero. At

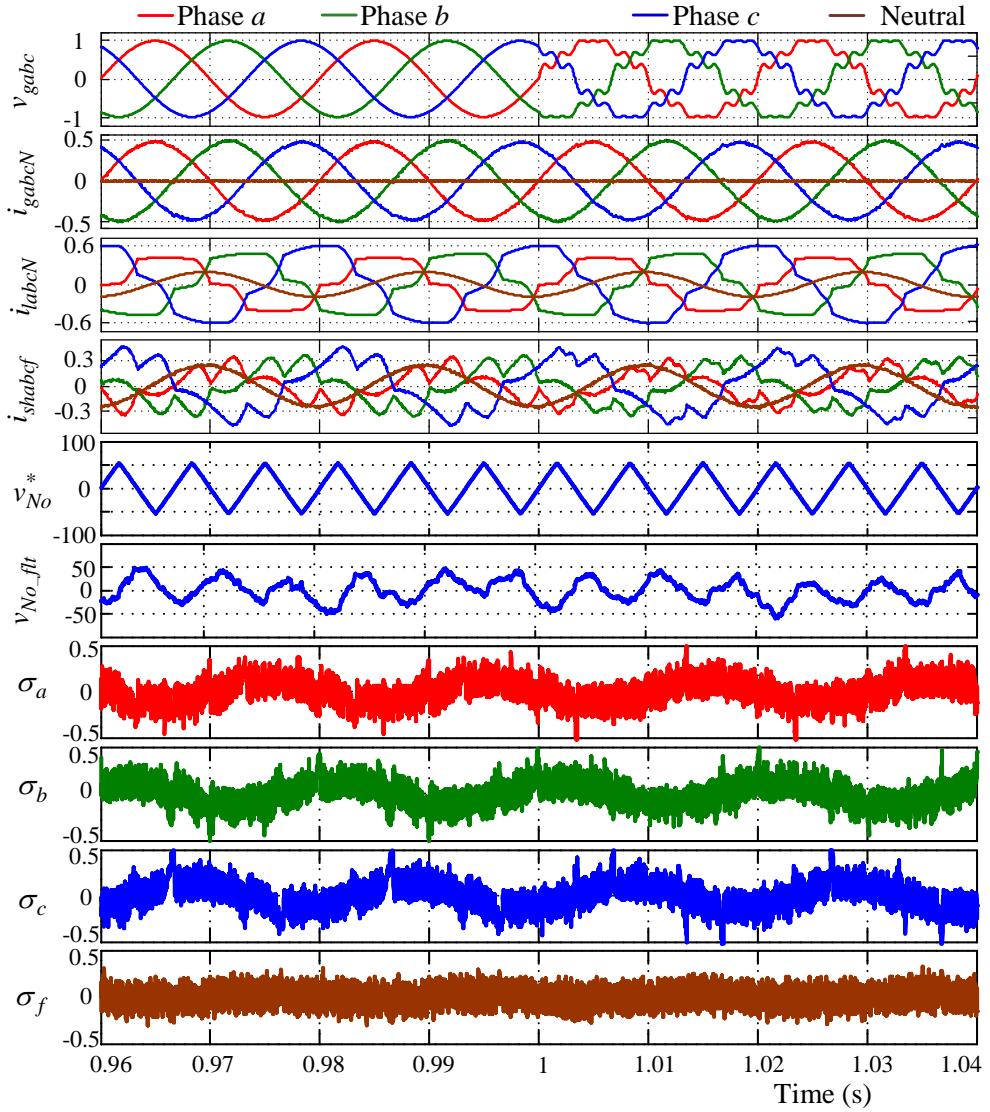


Figure 4.5: Simulation results of grid voltages (v_{gabc}), and currents of grid, load and DSTATCOM (i_{gabcN} , i_{labcN} , i_{shabcf}) in per unit, load NPV reference (v_{No}^*) in volts, filtered load NPV (v_{No_flt}) in volts and sliding variables (σ_{abcf}) in amps during grid voltage variations

$t = 1.5$ s, load curtailment is introduced. During all the conditions: load curtailment, normal and distorted conditions, the compensated grid currents are resulted as balanced and in-phase with the grid voltages. The grid neutral current becomes zero, indicating that the DSTATCOM has supplied all load components except the fundamental positive sequence component.

The load NPV is a high-frequency pulsed waveform, therefore it is passed through a low pass filter (LPF) with a desired cut-off frequency of 150 Hz. The filtered

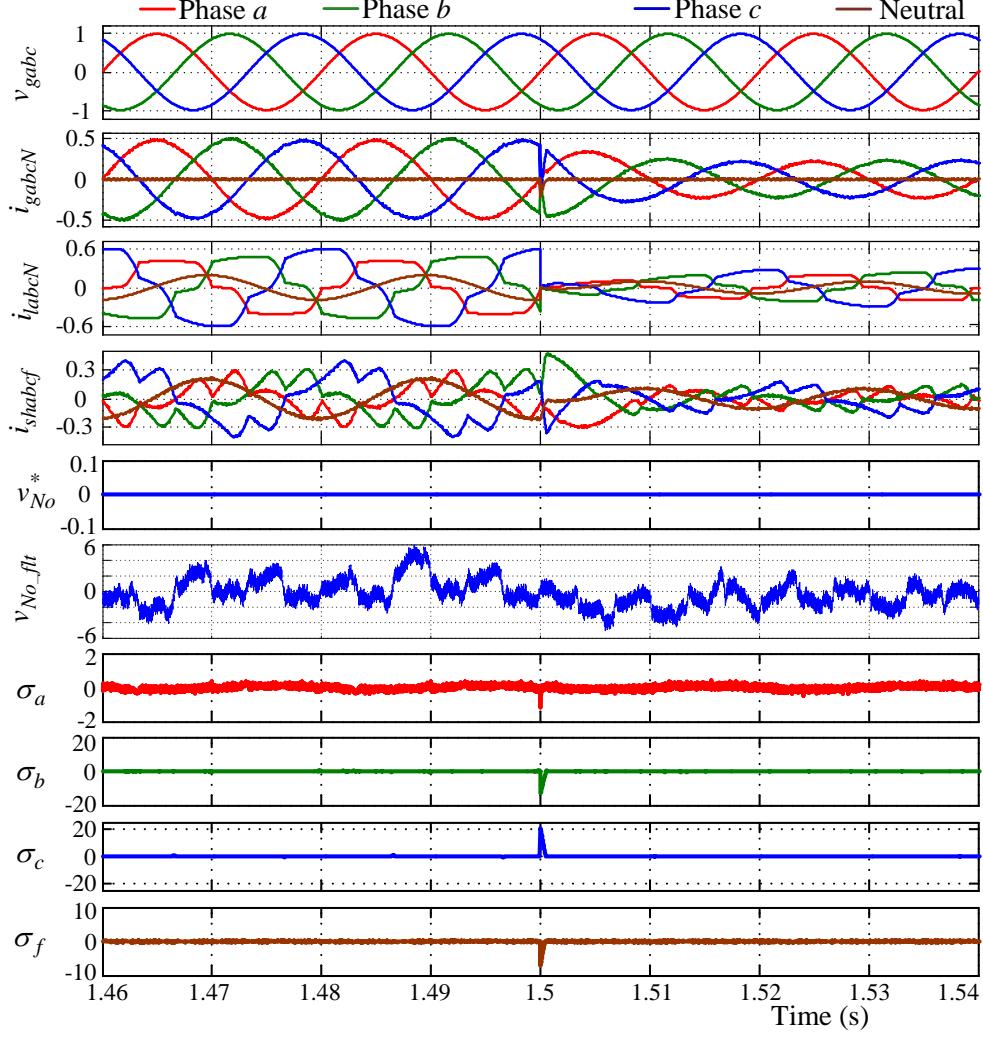


Figure 4.6: Simulation results of grid voltages (v_{gabc}), and currents of grid, load and DSTATCOM (i_{gabcN} , i_{labcn} , i_{shabcf}) in per unit, load NPV reference (v_{No}^*) in volts, filtered load NPV (v_{No_flt}) in volts and sliding variables (σ_{abcf}) in amps during load curtailment

load NPVs, v_{No_flt} , shown in Figs. 4.5-4.6, successfully track the reference load NPV signals, whether they are zero or triplen harmonics. This demonstrates the ability of the proposed algorithm to track both compensator reference currents and load NPVs accurately under various system conditions. The sliding variables σ_{abcf} are observed to be close to zero for different system conditions, indicating a good reference tracking accuracy of the proposed algorithm.

In Figs. 4.7-4.8, the frequency spectra of the grid current i_{ga} for both HCC and the proposed SMC-based four-leg DSTATCOM are compared. Fig. 4.7 represents the

spectrum during half load condition, while Fig. 4.8 represents the spectrum during one-fourth load condition. It can be observed that the spectrum of HCC spreads uniformly up to 10 kHz, whereas the spectrum of the proposed SMC spreads dominantly at integral multiples of 10 kHz. This indicates that HCC operates with a variable switching frequency, while the proposed SMC achieves a constant switching frequency operation.

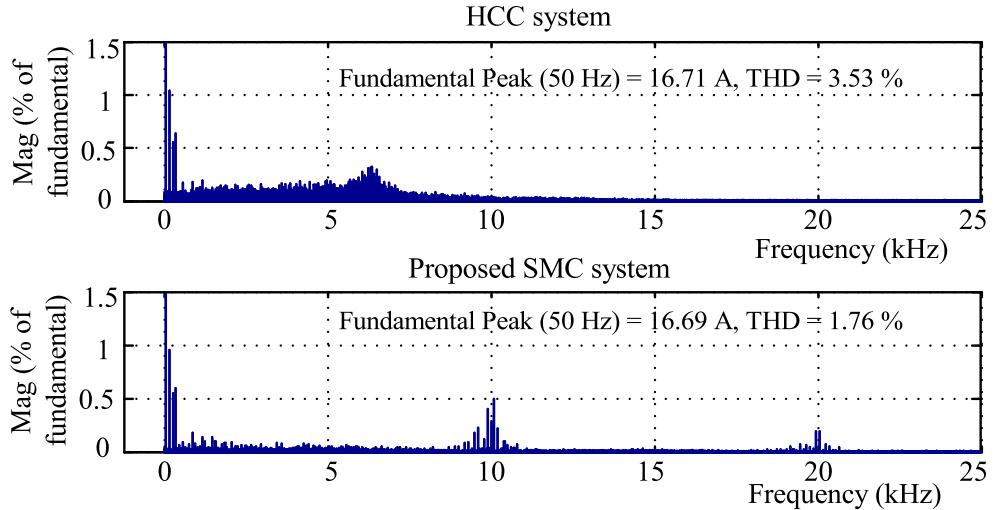


Figure 4.7: Simulation results of THD spectrum for phase-a grid current during half load

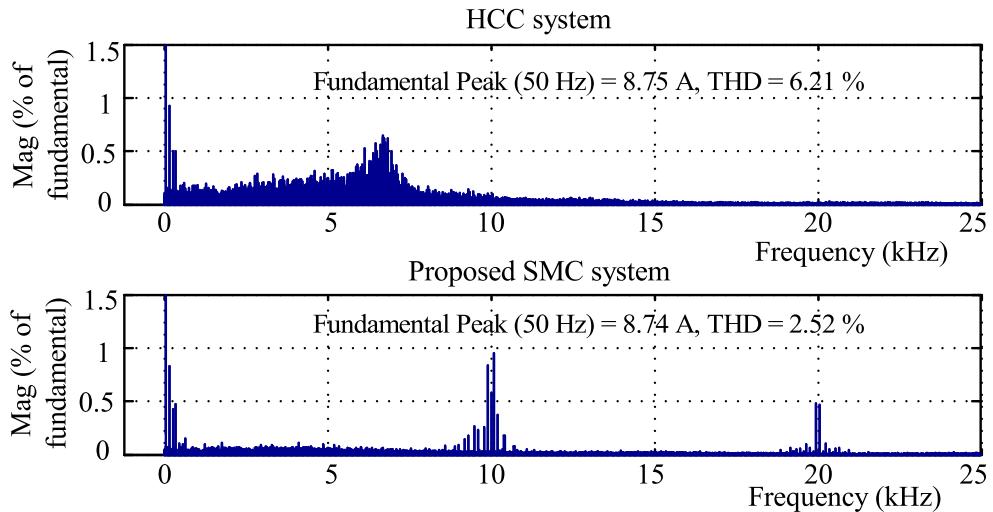


Figure 4.8: Simulation results of THD spectrum for phase-a grid current during one fourth load

In Figs. 4.9-4.10, a comparison is made between the performance of the conventional

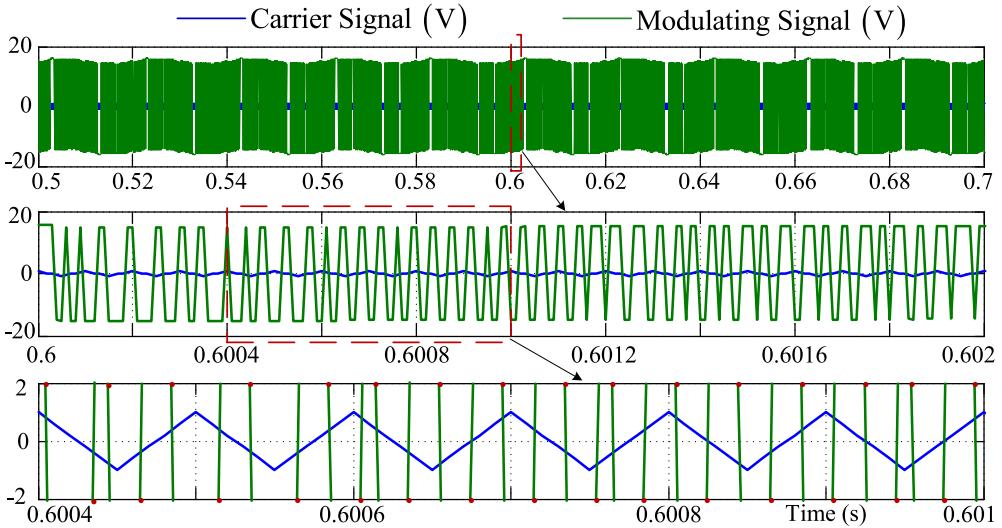


Figure 4.9: Converter modulating signal of phase- a for sgn function

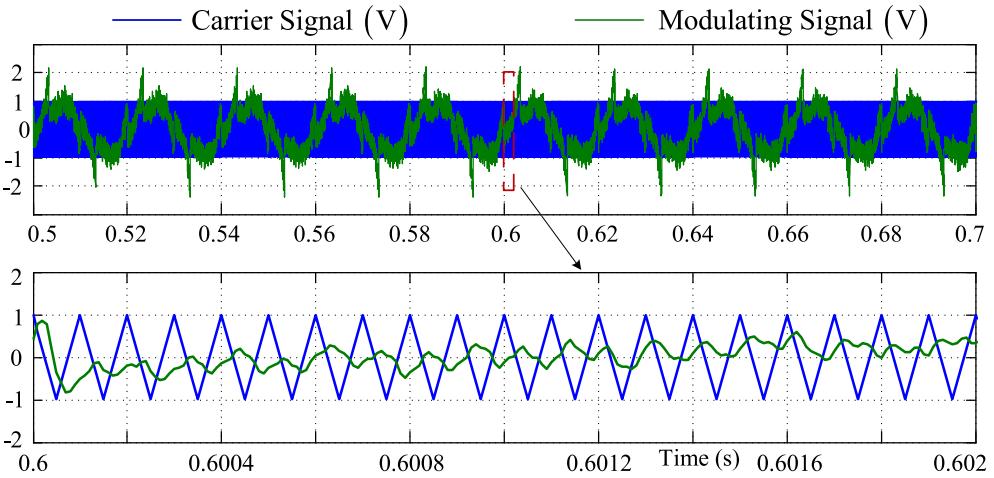


Figure 4.10: Converter modulating signal of phase- a for \tanh function

signum function and the \tanh function in terms of the switching pattern for a normal grid condition. Fig. 4.9 shows the modulating signal (m_a), which is a scaled version of the converter reference voltage of phase- a (v_{a0}^{con}) with a carrier wave using the signum function. Fig. 4.10 represents the same for the \tanh function. For both functions, the value of k in (4.15) is set to 15, while the value of a for the \tanh function is set to 10. It is worth noting that the signum function can be considered as an equivalent of the \tanh function with $a = \infty$. By comparing the two plots, it is evident that the signum function exhibits multiple crossings between m_a and the carrier wave, as observed in the zoomed view in Fig. 4.9. Conversely, no such multiple crossings are observed in Fig. 4.10.

The total harmonic distortions (THDs) of the compensated grid currents i_{ga} , i_{gb} , i_{gc} are recorded as 1.62%, 1.72%, 1.6% with the signum function, and 1.76%, 1.96%, 1.87% with the $tanh$ function, respectively. These results indicate that the $tanh$ function avoids multiple switchings at the expense of slightly higher ripples in the compensated currents compared to the signum function. However, the THDs of the currents remain within the limits specified by IEEE Std. 519. Additionally, it is observed that lower values of a lead to higher THDs, implying higher steady-state errors and fewer multiple switchings. Thus, the selection of a involves a trade-off between steady-state error and multiple switchings.

To compare the performance of the proposed control scheme with HCC, the THDs of load and grid currents are presented in Fig. 4.11 for various system conditions and parameter variations. In this study, the investigation of controller robustness focuses on two parameters: load power and filter inductance. The THDs of the compensated grid currents shown in Fig. 4.11 under normal grid, distorted grid, full load, half load, and one-fourth load conditions are obtained using a filter inductance of the nominal value, i.e., $L_{sh} = 22.5$ mH. The THDs of the compensated grid currents in Fig. 4.11 for the other two cases provide insights into the robustness of the proposed algorithm against variations in the filter inductance. The variations in the filter inductance considered for this study are $L_{sh} \pm 10$ mH, where the nominal inductance L_{sh} is 22.5 mH. The indicated inductance values in Fig. 4.11 are used in the controller for an actual filter inductance of 22.5 mH. It is observed that the proposed SMC exhibits significantly reduced THDs of grid currents during both normal and distorted grid conditions, indicating its superior performance over HCC and a substantial reduction in chattering. Moreover, both control schemes demonstrate less sensitivity to variations in load power and filter inductance due to their belonging to the variable structure system (VSS) category, which is known for its robustness against unmodeled dynamics. However, the proposed SMC offers greater flexibility with additional control laws, resulting in lower THDs in the

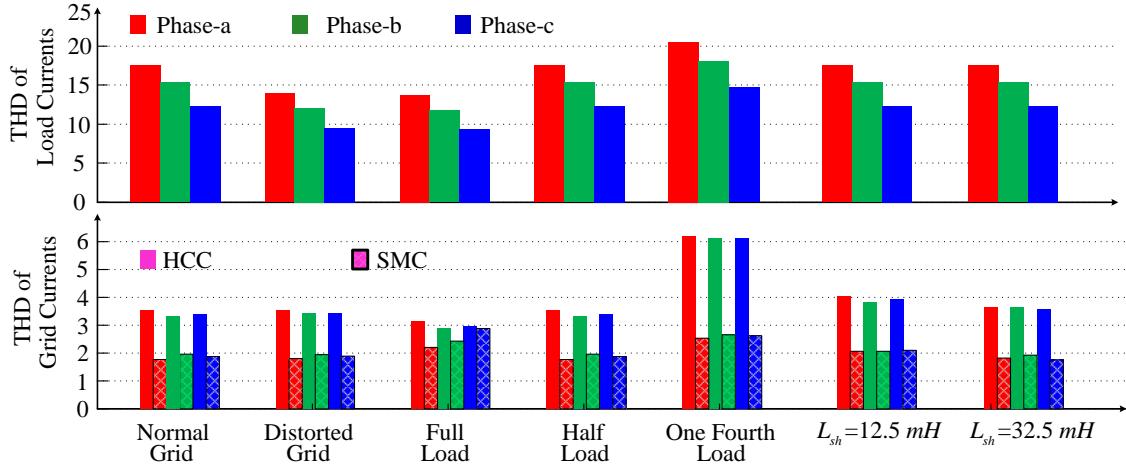


Figure 4.11: Performance comparision of HCC and proposed SMC for various system conditions and parameter variations

compensated grid currents.

4.5 EXPERIMENTAL STUDIES

A prototype of the four-leg DSTATCOM system, as shown in Fig. 4.4, has been developed to compare the performance of the proposed SMC with the HCC system. The experimental study utilizes the system parameters listed in Table 4.2. The hardware setup is depicted in Fig. 4.12. The four-leg voltage source inverter (VSI) is implemented using IGBT-based SEMIKRON stack. Each leg of the inverter is connected to a similar interfacing inductor. Voltage and current signals are sensed using hall effect transducers and fed to the real-time controller Opal-RT OP4510 (main) and OP4520 (auxiliary) through their analog to digital conversion (ADC) ports. The control algorithm is programmed with a step time of $10 \mu\text{s}$ using the RT-LAB software installed on the host PC. Communication between the real-time controller and the host PC is established via an Ethernet cable, enabling the modification of system parameters such as k , a , and v_{No}^* during the execution of the real-time model.

In the experimental setup, a three-phase power supply is stepped down to 50 V (1 pu) per phase using a three-phase auto transformer, as depicted in Fig. 4.13(a). To evaluate

Table 4.2: System parameters for experimental study

System parameters	Values
Base quantities	$S_b = 350 \text{ VA}$, $V_b = 50 \text{ V}$ (L-N RMS)
Filter parameters	$L_{sh} = 20 \text{ mH}$
DC-link voltage	$V_{dc} = 200 \text{ V}$
DC-link capacitor	$C_{dc} = 2350 \mu\text{F}$
Linear RL load	$Z_a = 17 + j55.67 \Omega$, $Z_b = 50 + j58.72 \Omega$, $Z_c = 42 + j121.2 \Omega$.
Resistive load	$R_a = 48.5 \Omega$, $R_b = 32 \Omega$, $R_c = 54 \Omega$
Nonlinear load	3- ϕ diode bridge rectifier with $R_{nl} = 92 \Omega$, $L_{nl} = 85.7 \text{ mH}$
SMC parameters	$a = 20$, $k = 125$

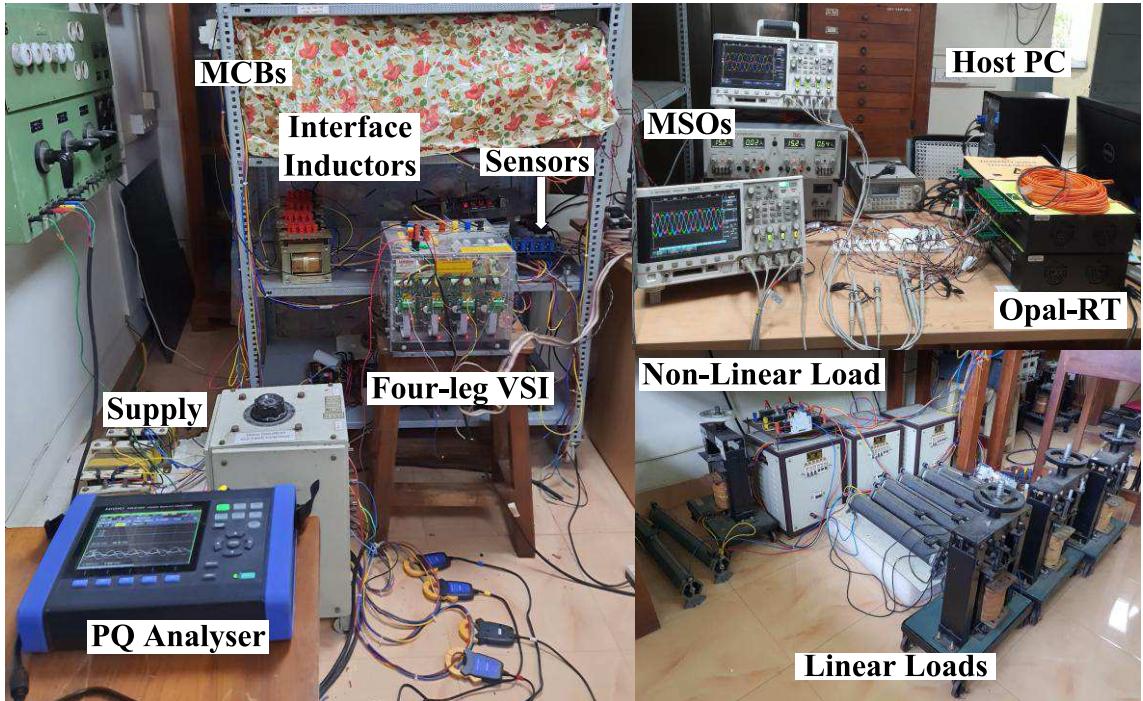


Figure 4.12: Experimental prototype of the four-leg DSTATCOM

the dynamic performance of the four-leg DSTATCOM, a resistive load is suddenly disconnected at time $t = t_1$, as shown in Fig. 4.13(b). The balanced compensated grid currents in Fig. 4.13(c) demonstrate the robustness of the proposed control scheme against load variations. Fig. 4.13(d) displays the DSTATCOM currents, where the current through the fourth leg is similar to the load neutral current, resulting in zero current flow through the grid neutral. The reference load NPV (v_{No}^*) is set to zero, as

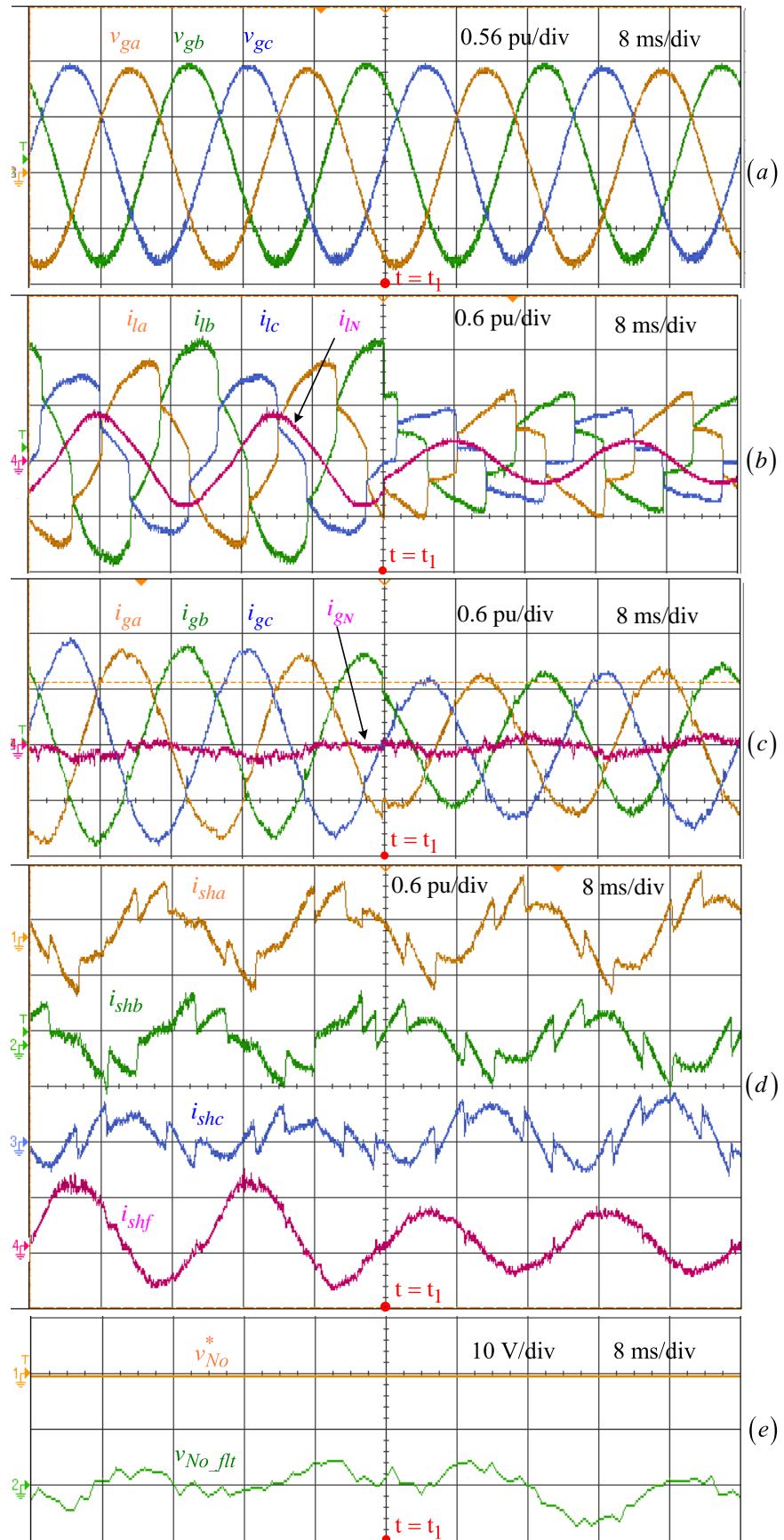


Figure 4.13: Experimental results during load curtailment: (a) Grid voltages, (b) Load currents, (c) Grid currents, (d) DSTATCOM currents, and (e) Load neutral-point-voltages

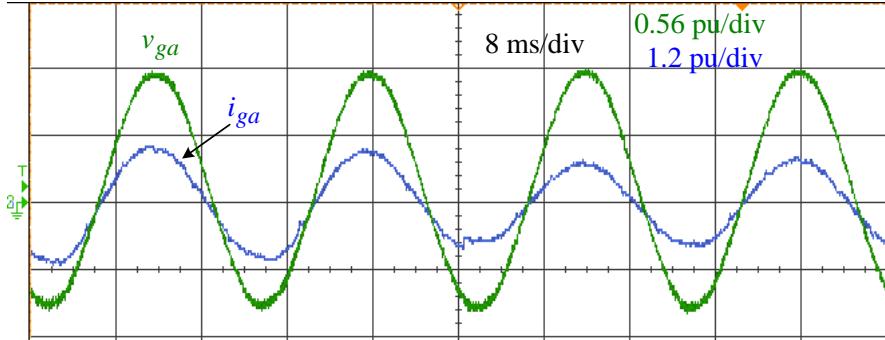


Figure 4.14: Experimental result: grid voltage and current after compensation

shown in Fig. 4.13(e). The load NPV, which is a high-frequency pulsed waveform, is passed through a low-pass filter (LPF) with a cut-off frequency of 150 Hz. The filtered load NPV, denoted as v_{No_flt} in Fig. 4.13(e), tracks its reference load NPV of 0 V. This indicates that the proposed algorithm is capable of tracking both the compensator reference currents and the reference load NPV. Fig. 4.14 illustrates that the phase difference between the grid voltage and grid current is nearly zero, implying that unity power factor at the grid is achieved by the proposed control scheme. The percentage THDs of the load currents are 14.1% (wire *a*), 11.18% (wire *b*), 14.23% (wire *c*), and 10.01% (wire *f*). The frequency spectrum of the compensated grid current, i_{ga} , is depicted in Fig. 4.15 for both the HCC and proposed SMC schemes. It can be observed that the proposed SMC achieves a lower THD compared to the HCC scheme, indicating improved current quality.

In Fig. 4.16, the performance of the four-leg DSTATCOM at full load condition is demonstrated for a change in the reference load NPV from 50 V to 0 V. Fig. 4.16(a) shows that the averaged load NPV, v_{No_flt} , tracks the reference load NPV of 50 V and 0 V. The load currents, grid currents, and DSTATCOM currents for the variation in reference load NPV are depicted in Figs. 4.16(b)-(d), respectively. The balanced grid currents indicate that the compensator with the proposed algorithm has supplied the fundamental reactive and harmonic load currents. Thus, it can be concluded from Fig. 4.16 that the proposed algorithm is capable of tracking the reference load NPVs in

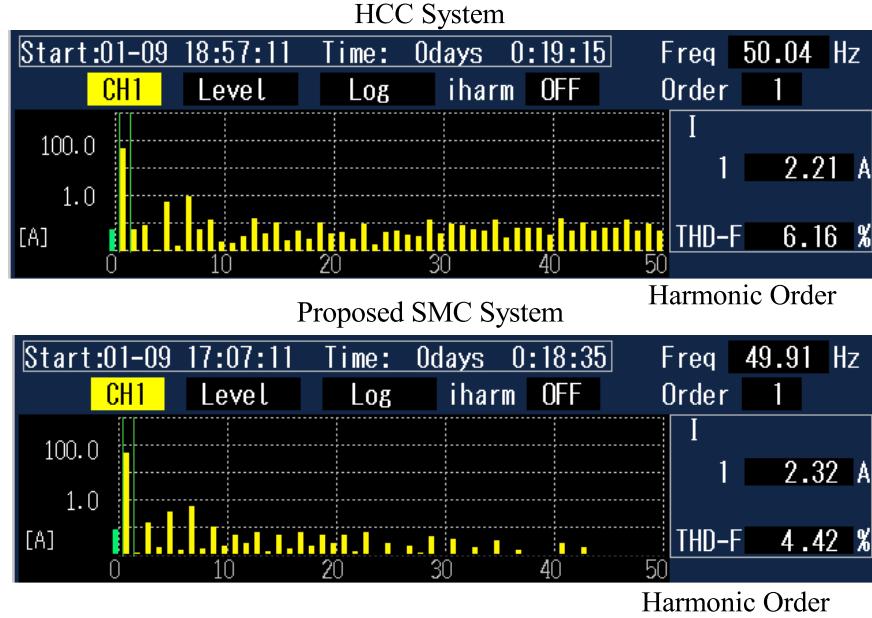


Figure 4.15: Experimental result: frequency spectrum of grid current i_{ga}

addition to the compensator reference currents.

4.6 STATE-OF-THE-ART AND PROPOSED METHOD COMPARISONS

Table 4.3 provides a comparison of the proposed method with state-of-the-art techniques. The method presented in [38] has a drawback in that it involves the dq-transformation of various signals and requires multiple PR controllers, each one is responsible for compensating a specific frequency component of the reference currents. However, when the estimation of the grid voltage phase angle is not accurate, the use of dq-transformation introduces errors and inaccuracies in reference tracking. To overcome the limitations of linear controllers, researchers have explored non-linear controllers in the literature. These non-linear controllers aim to achieve robust performance across a wide range of operating conditions.

In the natural reference frame, the current dynamics of a three-wire three-leg or four-leg converter-based DSTATCOM are interconnected through the converter pole voltages, which is a result of the load's neutral-point voltage (NPV). In order to achieve a

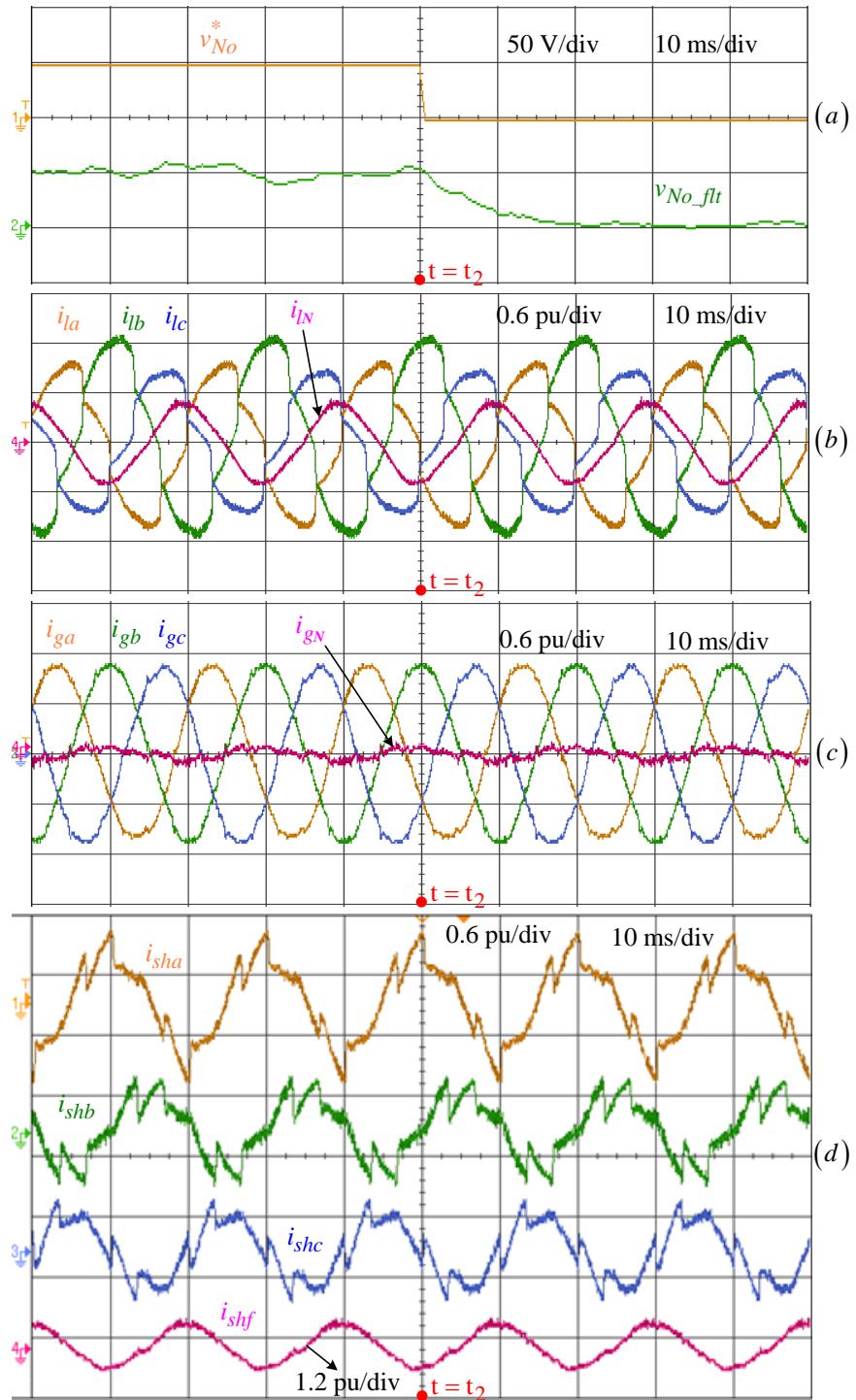


Figure 4.16: Experimental results during full load condition: (a) Load NPVs, (b) Load currents, (c) Grid currents, and (d) DSTATCOM currents

decoupled characteristic, signals are transformed into a new $\gamma\theta$ -frame as described in [45]. However, this transformation is susceptible to transformation errors. In contrast, the coupling mentioned above is absent in [138] due to the implementation of a split-capacitor based three-leg converter topology. However, this converter topology has certain limitations compared to the four-leg converter topology mentioned in [125]. Additionally, the absence of load NPV in the split-capacitor based three-leg converter topology makes it unsuitable for dual-output converter based power quality conditioners.

In the study conducted in [136], one of the four controllers designed is redundant because a four-wire system only has three independent currents. Moreover, the control of load NPV is crucial for dual-output converter based power quality conditioners, as the absence of such control can lead the converter to enter an invalid switching state, resulting in undesired performance. Therefore, the proposed method incorporates load NPV control, whereas it is not incorporated in [38, 45, 136], and [138]. The control scheme presented in this chapter can be utilized for the control of dual-output converter based power quality conditioners.

Table 4.3: A comparison between the proposed method and the existing techniques

Comparison category	[38]	[45]	[136]	[138]	Proposed method
Converter topology	Three-wire three-leg converter	Three-wire three-leg converter	Four-wire four-leg converter	Four-wire three-leg converter	Four-wire four-leg converter
Generation of compensator reference currents	SRF theory	Based on DC-link voltage control	ISC	IRP	ISC
Control strategy	Linear PR	SMC	HCC	Second Order SMC	SMC
Controller implementation in	dq -frame	$\gamma\theta$ -frame	Natural frame	Natural frame	Natural frame
Constant switching frequency operation	Yes	Yes	No	Yes	Yes
Ability of load balancing	Yes	Yes	Yes	Yes	Yes
Ability of load NPV control	No	No	No	No	Yes

4.7 SUMMARY

This chapter presents the design of a decoupled sliding mode control scheme for the control of a four-leg DSTATCOM in the natural reference frame. In conventional control schemes, the dynamics of sliding variables are coupled through the manipulated input variables. However, in the proposed scheme, this coupling is eliminated by introducing a new sliding surface function. The redundant current controller found in conventional schemes is utilized in the proposed scheme to control the fourth independent variable, which is the current due to Thevenin's equivalent load NPV. The design of the proposed scheme, which includes load NPV control, is also applicable to the control of dual-output converter based power quality conditioners.

By employing the proposed control scheme, accurate control of load NPV is achieved under various system conditions without compromising the common functionalities of a DSTATCOM. The effectiveness of the proposed scheme is validated through detailed simulations and experimental studies conducted on a four-leg DSTATCOM system. The results of these studies indicate that the proposed control scheme offers the following advantages: (a) robust performance against variations in filter inductances and load powers; (b) operation at a constant switching frequency; and (c) reduced total harmonic distortions (THDs) in the compensated grid currents.

CHAPTER 5

SLIDING MODE CONTROL OF A FOUR-LEG DYNAMIC VOLTAGE RESTORER IN A NATURAL REFERENCE FRAME

5.1 INTRODUCTION

Chapter 4 explores the performance of the proposed sliding mode control (SMC) on a four-leg distribution static compensator (DSTATCOM). The control scheme introduced in Chapter 4 enables regulation of the neutral-point voltage (NPV) and DSTATCOM currents. With the inclusion of NPV control, this scheme can be applied to the shunt terminal of the dual-output converter (DOC)-based unified power quality conditioner (UPQC). In this chapter, a control scheme incorporating NPV control is developed for the dynamic voltage restorer (DVR), which can later be extended to the series terminal of the DOC-based UPQC.

The presence of single-phase loads in a distribution system can lead to uneven loading among phases, resulting in load voltage imbalance. Furthermore, intermittent distributed energy resources can cause voltage disturbances, necessitating the use of a DVR to ensure a reliable power supply with high quality. The conventional DVR system consists of a three-phase three-leg voltage source converter (VSC), LC filters, and three single-phase isolation transformers. The DVR is connected in series with the load bus to protect sensitive loads against voltage disturbances.

To prevent line-line faults through the DC bus, the converter terminals of a conventional DVR are connected to the distribution feeder lines through isolation transformers. The transformer-less DVR (TDVR) topology has been studied to reduce system size

[47, 139], but it is only suitable for a single-phase system and not for a three-phase system with a common DC source. A modified conventional DVR topology has been proposed to include a fault current limiting function without compromising the DVR's functionalities [140, 141]. The DVR has also been utilized to meet fault ride-through requirements in wind farms [142, 143].

In the conventional DVR system, the secondary windings of the three isolation transformers are connected to the respective phases of the feeder, with the primaries connected in either a delta or star configuration. The delta configuration allows the flow of zero-sequence current but does not facilitate the injection of zero-sequence voltage, limiting the DVR's compensation capability during unbalanced voltage sag/swell with a zero-sequence component. On the other hand, the star configuration enables the injection of zero-sequence voltage but lacks the flow of zero-sequence current, impacting the DVR's ability to regulate load voltage for unbalanced loads, regardless of the type of voltage disturbance. A full control over the zero-sequence current and voltage can be achieved using a four-leg voltage source converter (FL-VSC) or a three-leg split capacitor-based converter. The FL-VSC is chosen in this chapter due to its lower DC-link voltage requirement, smaller DC-link capacitor, and absence of voltage balancing control circuitry [144–147].

Various methods for generating reference voltages and controllers for DVRs have been proposed in the literature. The generation of reference voltage methods such as pre-sag, in-phase, energy-optimized compensations, and dual instantaneous active-reactive power theory [30–33] have been used. In-phase compensation is a method that requires a lower DC-link voltage and can be implemented in the natural reference frame. Implementing a suitable controller in the same reference frame would reduce the computational burden and signal transformation errors. Controllers such as Pseudo-derivative feedback control [148] and PI controllers [149] have been used, with the former providing faster response than the latter for three-leg DVRs. However, the PI

controller can only achieve zero steady-state tracking error for DC signals. To process fundamental balanced AC signals, the PI controller is implemented in the synchronous reference (dq) frame, where the dq components of balanced AC signals appear as DC. In the presence of unbalanced and/or harmonic signals, sequence components of each frequency signal are processed individually using PI controllers in dq frame [34, 35] or using proportional-resonant (PR) controllers either in $\alpha\beta$ frame or abc frame [36]. While PR controllers can accurately process signals with frequencies corresponding to the controller resonant frequency, they require multiple PR controllers for systems dealing with harmonics, increasing design complexity.

Non-linear controllers such as hysteresis, model predictive, and sliding mode controllers are more suitable for DVRs due to their non-linear nature. Non-linear controllers accurately process any frequency signals, provided that the sampling time of the processor is low. Therefore, they can be implemented in the natural reference frame. The principle of the hysteresis controller [41] is the same as the conventional sliding mode controller (SMC). The sliding mode controller is robust against model inaccuracies and involves lower computational burden on digital processors compared to the model predictive controller [42].

Existing SMC schemes in the literature, presented in the natural frame, mainly focus on single-phase DVRs [48, 50]. The design of SMC with conventional sliding surfaces is straightforward and applicable to single-phase DVRs, which lack the presence of converter NPV. However, for three-phase systems, configurations with three single-phase half-bridge [47] or full-bridge [49] DVRs have been used, resulting in higher DC-link voltage requirements or increased number of switches. Both configurations lack converter NPV. In a four-leg converter-based DVR system, the presence of converter NPV introduces coupling in the voltage dynamics, making it challenging to assign appropriate values to control input variables using SMC with a conventional sliding surface. To address this, a new sliding surface is proposed in this chapter for the four-

Table 5.1: A comparison between the proposed method and the existing techniques

Comparison category	[47]	[48]	[50]	[49]	[147]	Proposed SMC
VSC topology	1- ϕ HB	1- ϕ FB	1- ϕ FB	1- ϕ FB	Four-leg	Four-leg
No. of semiconductor switches	6	12	12	12	8	8
No. of DC buses	3	1	1	1	1	1
Required DC bus voltage	$2v_{dc}$	v_{dc}	v_{dc}	v_{dc}	v_{dc}	v_{dc}
Control strategy	SMC	SMC	SMC	SMC	SMC	SMC
Frame of Control study	Natural	Natural	Natural	Natural	$\alpha\beta$	Natural
VSC control type (Application)	Voltage (DVR)	Voltage (DVR)	Voltage (DVR)	Voltage (DVR)	Voltage (UPS)	Voltage (DVR)
Ability of independent control	Yes	Yes	Yes	Yes	Yes	Yes
Ability of NPV control	No	No	No	No	No	Yes

leg converter-based DVR system.

Table 5.1 provides a comparison of the proposed scheme with other methods, highlighting the advantages of the four-leg converter with the proposed scheme, including a minimum number of switches and DC buses, lower DC voltage requirement, elimination of signal transformations, ability to control the neutral-point voltage, and per-phase system analysis. The design approach of SMC with the proposed sliding surface can also be applied to a three-wire DVR system.

5.2 MODELING OF FOUR-LEG DVR

Fig. 5.1 illustrates the schematic of a four-leg VSC-based DVR connected to a three-phase four-wire distribution system. For the purpose of this study, the dynamics of the DC-link voltage are neglected, assuming a stiff DC bus. In this section, the mathematical model of the four-leg DVR and the conventional SMC design in the natural reference frame are reviewed to elucidate the challenge associated with assigning suitable values to the control input variables.

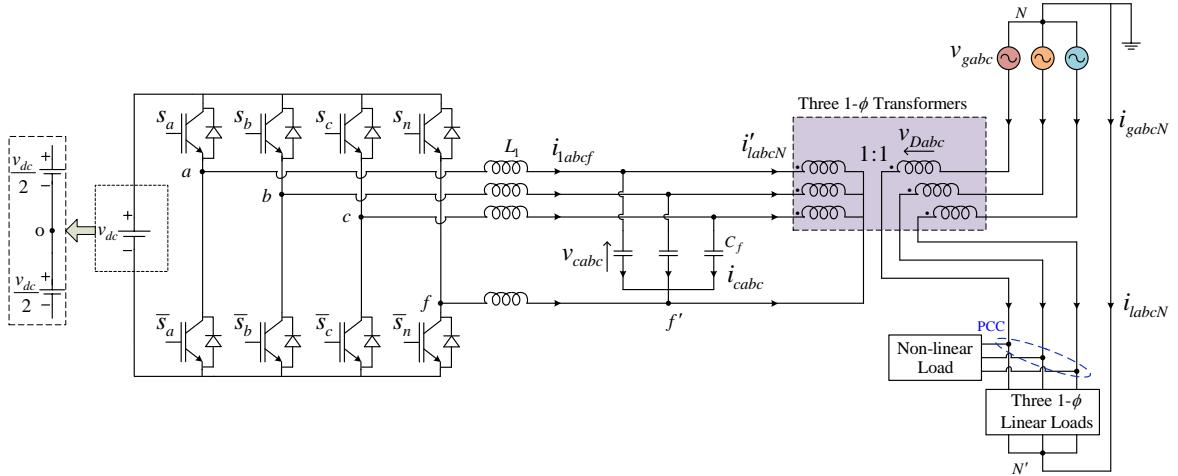


Figure 5.1: Schematic diagram of four-leg voltage source converter based DVR

5.2.1 System Modeling

To better comprehend the system dynamic equations, the diagram in Fig. 5.1 illustrates the extended split-source-based DC bus. The following equations describe the system

dynamics:

$$\begin{aligned} v_{io} &= L_1 \frac{di_{1i}}{dt} + v_{ci} + v_{f'o}, \\ C_f \frac{dv_{ci}}{dt} &= i_{1i} - i'_{li}, \end{aligned} \quad (5.1)$$

$$\begin{aligned} v_{fo} &= L_1 \frac{di_{1f}}{dt} + v_{f'o}, \\ -C_f \frac{d}{dt} \sum_i v_{ci} &= i_{1f} - i'_{lN}, \end{aligned} \quad (5.2)$$

where $i \in \{a, b, c\}$, $j \in \{i, f\}$, v_{jo} represent pole voltages of four-leg converter, v_{ci} represent filter-capacitor voltages, i_{1j} and L_1 represent inverter side currents and filter inductance, respectively. The currents, i'_{li} , i'_{lN} represent primary (inverter) side currents of injection transformers. In the case of unity turn's ratio transformers, these currents are equivalent to the load currents. The converter neutral-point voltage (NPV), $v_{f'o}$ refers to the voltage between the common point 'f' of the filter-capacitor's and the mid point 'o' of the DC-link. The expression for converter NPV given below is obtained by summing up all pole voltages of (5.1) and (5.2).

$$v_{f'o} = \frac{1}{4} \sum_{i=a,b,c} (v_{io} + v_{fo} - v_{ci}) \quad (5.3)$$

The pole voltages in the system always have values of either $+0.5$ times the DC bus voltage (v_{dc}) or -0.5 times the DC bus voltage. In other words, the voltage at the junction of each leg, denoted as v_{jo} , can be expressed as $u_j \cdot \frac{v_{dc}}{2}$. Here, u_j represents the control (manipulated) input variable for the j -th leg. When the top switch of the j -th leg (S_j) is turned ON and the bottom switch (\bar{S}_j) is turned OFF, u_j is assigned a value of $+1$. On the other hand, when the top switch is OFF and the bottom switch is ON, u_j is assigned a value of -1 . Taking this into account, (5.3) is modified as follows:

$$v_{f'o} = \frac{1}{4} \sum_{i=a,b,c} \left(\frac{v_{dc}}{2} \{u_i + u_f\} - v_{ci} \right). \quad (5.4)$$

5.2.2 Conventional SMC

To simplify the discussion, let's focus on the design of the conventional SMC for phase-*a* in the system. The state variables for phase-*a* can be defined as follows:

$$\begin{aligned} x_{a1} &= v_{ca} - v_{ca}^*, \\ x_{a2} &= \dot{x}_{a1} = \dot{v}_{ca} - \dot{v}_{ca}^*, \end{aligned} \quad (5.5)$$

where v_{ca}^* represents the DVR reference voltage for phase-*a*. It is important to note that, for any variable (say x), the terms \dot{x} , \ddot{x} and x^* refer to the first and second time derivatives, and the reference value of x , respectively. This notation is continuously followed throughout the thesis. The sliding variable, σ is commonly defined as [150],

$$\sigma = \left(\lambda + \frac{d}{dt} \right)^{n-1} x, \quad (5.6)$$

where x refers to the difference between actual and reference quantities, λ represents a sliding coefficient and n represents the order of system. Considering that the four-leg DVR system has an order of 2, the sliding variable for the phase-*a* leg can be expressed as follows:

$$\sigma_a = \left(\lambda_a + \frac{d}{dt} \right) x_{a1}. \quad (5.7)$$

In the control design process based on Lyapunov stability criteria, the objective is to ensure that the sliding variable σ_a reaches its surface $\sigma_a = 0$ within a finite time. According to Lyapunov stability criteria, the system is considered asymptotically stable if the Lyapunov function $V(\sigma_a)$ satisfies the following properties:

$$1. V(\sigma_a) = 0 \text{ if and only if } \sigma_a = 0$$

$$2. V(\sigma_a) > 0 \text{ if and only if } \sigma_a \neq 0$$

$$3. \dot{V}(\sigma_a) < 0 \quad \forall \sigma_a \neq 0.$$

To satisfy the first two properties of Lyapunov stability criteria, the Lyapunov function is chosen as follows:

$$V(\sigma_a) = \frac{1}{2}\sigma_a^2. \quad (5.8)$$

To verify the final property, the condition that needs to be satisfied is:

$$\sigma_a \dot{\sigma}_a < 0. \quad (5.9)$$

By differentiating (5.7) with respect to time, the following expression is obtained.

$$\dot{\sigma}_a = \left(\lambda_a + \frac{d}{dt} \right) \dot{x}_{a1} \quad (5.10)$$

Based on (5.5), the update for $\dot{\sigma}_a$ can be expressed as follows:

$$\dot{\sigma}_a = \lambda_a x_{a2} + \ddot{v}_{ca} - \ddot{v}_{ca}^*. \quad (5.11)$$

From (5.1), the updated expression for the above equation is as follows:

$$\begin{aligned} \dot{\sigma}_a &= \lambda_a x_{a2} + \frac{1}{C_f} \left(\dot{i}_{1a} - \dot{i}'_{la} \right) - \ddot{v}_{ca}^*, \\ &= \lambda_a x_{a2} + \frac{1}{L_1 C_f} \left(v_{ao} - v_{ca} - v_{f'o} - L_1 \dot{i}'_{la} \right) - \ddot{v}_{ca}^*. \end{aligned} \quad (5.12)$$

By adding and subtracting the term $\frac{1}{L_1 C_f} v_{ca}^*$ to (5.12), the following expression is obtained:

$$\dot{\sigma}_a = \lambda_a x_{a2} - \omega_0^2 x_{a1} + \omega_0^2 \left(v_{ao} - v_{ca}^* - v_{f'o} - L_1 \dot{i}'_{la} \right) - \ddot{v}_{ca}^*. \quad (5.13)$$

Where $\omega_0^2 = \frac{1}{L_1 C_f}$. Assuming the filter-capacitor voltages are balanced and by substituting (5.4) into (5.13) the following expression can be obtained.

$$\dot{\sigma}_a = \lambda_a x_{a2} - \omega_0^2 x_{a1} + \omega_0^2 \left(\frac{v_{dc}}{8} \{ 3u_a - u_b - u_c - u_f \} - v_{ca}^* - L_1 \dot{i}'_{la} \right) - \ddot{v}_{ca}^* \quad (5.14)$$

To satisfy the stability condition stated in (5.9), the control law/input is defined based on the polarity of σ . It can be expressed as follows [49]:

$$u_a = -\text{sgn}(\sigma_a). \quad (5.15)$$

Where $\text{sgn}(\cdot)$ is the signum function. However, this may not guarantee stability as the derivative of σ_a not only depends on u_a but also on the control inputs of other phases. To overcome this limitation and achieve decoupling of the control inputs, a new sliding variable is proposed in this chapter. The details of this new sliding variable will be explained in the upcoming section.

5.3 PROPOSED SLIDING MODE CONTROL SCHEME

The equivalent circuit of a four-leg DVR, based on (5.1) and (5.2) is illustrated in Fig. 5.2. It is important to note that the potential difference between grid neutral point ‘N’ or load neutral point ‘N’ and the capacitor neutral point ‘f’ is zero only when the capacitor voltages and the grid or load voltages are balanced. However, in Fig. 5.2, the dotted line representation from the grid or load neutral point to the capacitor neutral point indicates that the grid and load neutral currents are the negative sum of respective phase currents. The derived expressions for the DVR and capacitor voltages from Fig. 5.2 are given as follows:

$$v_{Di} = v_{li} - v_{gi}, \quad (5.16)$$

$$v_{ci} = v_{Di} + L_t \frac{di_{li}}{dt}, \quad (5.17)$$

where L_t is the equivalent transformer inductance, i_{li} are load currents and v_{Di} , v_{li} , v_{gi} are voltages of DVR, load and grid, respectively. From (5.16) and (5.17), the capacitor voltages are calculated using the sensed load currents, load and grid voltages.

From the Thevenin’s equivalent impedance seen at the converter NPV terminals, as

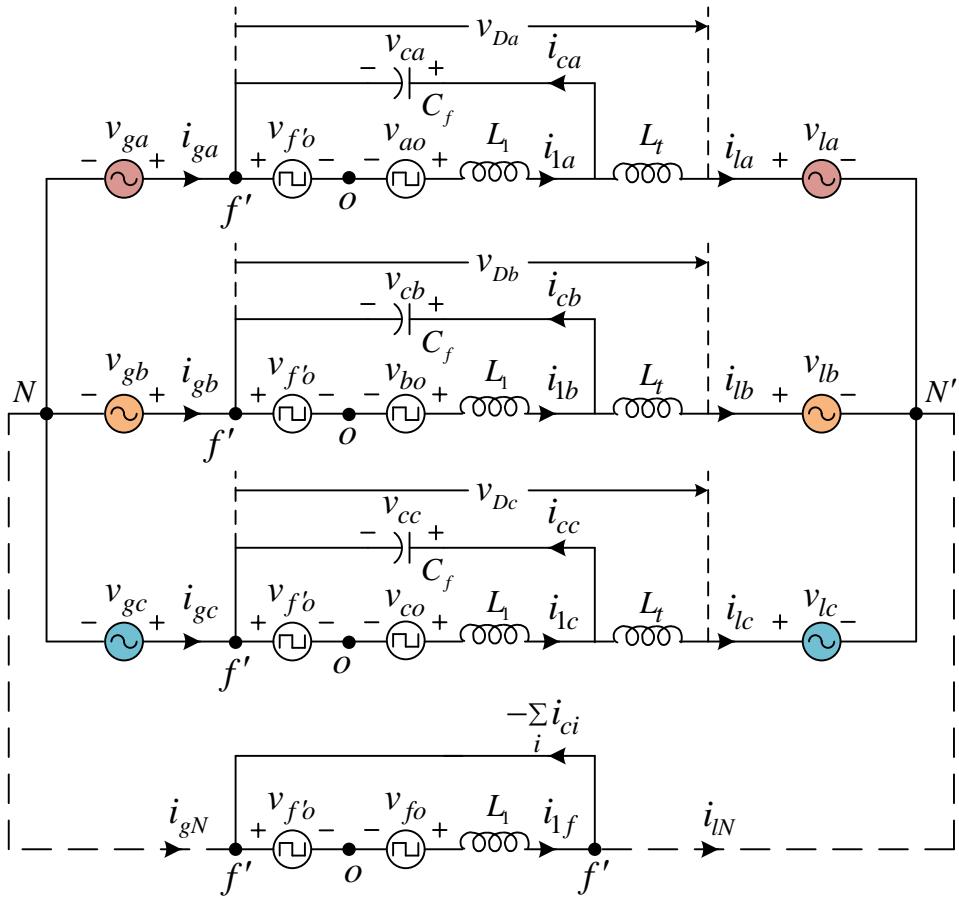


Figure 5.2: Equivalent circuit of four-leg DVR system

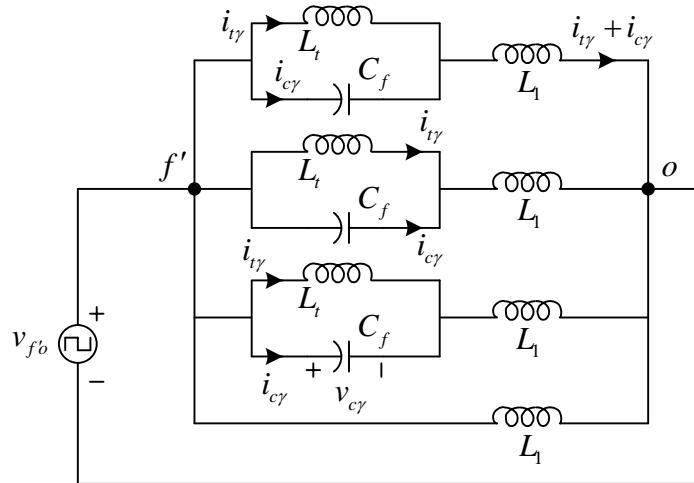


Figure 5.3: Thevenin's equivalent network seen by converter NPV terminals

shown in Fig. 5.3, the following expression can be obtained.

$$v_{f'o} = v_{c\gamma} + L_1 \frac{d}{dt}(i_{c\gamma} + i_{t\gamma}) \quad (5.18)$$

$$i_{c\gamma} = C_f \frac{dv_{c\gamma}}{dt}; \quad \frac{di_{t\gamma}}{dt} = \frac{v_{c\gamma}}{L_t} \quad (5.19)$$

By substituting (5.19) into (5.18), the following expression is obtained.

$$v_{f'o} = L_1 C_f \frac{d^2 v_{c\gamma}}{dt^2} + K v_{c\gamma} \quad (5.20)$$

Where $v_{c\gamma}$ is the voltage due to Thevenin's equivalent NPV of converter and $K = (1 + \frac{L_1}{L_t})$. The term $v_{c\gamma}$ is considered as a fourth controlled variable for the four-leg DVR.

Now, substituting (5.20) in (5.1) and (5.2), the following expression can be obtained.

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \\ v_{fo} \end{bmatrix} = L_1 C_f \begin{bmatrix} 1 & 0 & 0 & 1 \\ 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 \\ -1 & -1 & -1 & 1 \end{bmatrix} \begin{bmatrix} \ddot{v}_{ca} \\ \ddot{v}_{cb} \\ \ddot{v}_{cc} \\ \ddot{v}_{c\gamma} \end{bmatrix} + \begin{bmatrix} 1 & 0 & 0 & K \\ 0 & 1 & 0 & K \\ 0 & 0 & 1 & K \\ 0 & 0 & 0 & K \end{bmatrix} \begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \\ v_{c\gamma} \end{bmatrix} \\ + \begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_1 & 0 & 0 \\ 0 & 0 & L_1 & 0 \\ -L_1 & -L_1 & -L_1 & 0 \end{bmatrix} \begin{bmatrix} \dot{i}_{la} \\ \dot{i}_{lb} \\ \dot{i}_{lc} \\ 0 \end{bmatrix} \quad (5.21)$$

It is observed from (5.21) that the converter pole voltage of each phase-leg is influenced by the dynamics of corresponding phase capacitor voltage and $v_{c\gamma}$. Selecting sliding variable for each phase-leg as a combination of respective phase capacitor voltage and $v_{c\gamma}$ gives a decoupled feature with respect to the control inputs. Based on this, the selection of sliding surface is presented in the following subsection.

5.3.1 Selection of Sliding Surface

Let us define the state variables x_{p1} and x_{p2} of the DVR system as follows:

$$\begin{aligned} x_{p1} &= v_{cp} - v_{cp}^*, \\ x_{p2} &= \dot{x}_{p1} = \dot{v}_{cp} - \dot{v}_{cp}^*, \end{aligned} \quad (5.22)$$

where $p \in \{a, b, c, \gamma\}$. The generation of reference voltages (v_{cp}^*) is explained in the Section 5.3.3. To eliminate the cross-coupling effect in natural reference frame, the sliding surface is structured as follows:

$$\begin{aligned}\sigma_i &= \lambda_i x'_{i1} + x'_{i2} = 0, \\ \sigma_f &= \lambda_f x'_{f1} + x'_{f2} = 0,\end{aligned}\tag{5.23}$$

where λ_j are sliding coefficients, $x'_{i1} = x_{i1} + x_{\gamma 1}$, $x'_{i2} = x_{i2} + x_{\gamma 2}$, $x'_{f1} = x_{\gamma 1} - \sum_i x_{i1}$ and $x'_{f2} = x_{\gamma 2} - \sum_i x_{i2}$. Once the sliding surface is structured, the control law should be designed to ensure that the trajectory of states converges to their sliding surface, $\sigma_j = 0$ in a finite time and remains on the sliding surface. When the state trajectories on the sliding surface, the system dynamics are described by the following first-order equation.

$$\begin{aligned}\sigma_j &= \lambda_j x'_{j1} + x'_{j2} = 0 \\ \Rightarrow x'_{j2} &= \dot{x}'_{j1} = -\lambda_j x'_{j1}\end{aligned}\tag{5.24}$$

The solution of (5.24) is given by,

$$x'_{j1}(t) = x'_{j1}(0) e^{-\lambda_j t}.\tag{5.25}$$

From (5.25), it can be concluded that the time required to reach $x'_{j1} = 0$ is reduced with higher positive real values of λ_j . The selection of the sliding coefficients λ_j is an important aspect in designing the control law for the DVR system. The values of λ_j not only determine the convergence time of the sliding surface to zero but also affect the range of the sliding mode existence region. In [50], the sliding coefficient selection analysis is conducted in a two-dimensional space as the sliding surface is a function of two variables. However, the proposed sliding surface is a function of four variables, requiring the analysis to be carried out in a four-dimensional space. As a result, this chapter presents a selection procedure for λ_j that guarantees the maximum sliding mode existence region.

5.3.2 Selection of λ_j for Maximum Existence Region

To ensure the existence of sliding mode, the stability condition given in (5.9) should be satisfied, i.e.,

$$\sigma_j \dot{\sigma}_j < 0. \quad (5.26)$$

Therefore, the derivative of sliding variable (σ_j) is calculated from (5.1), (5.2), (5.20), (5.21), (5.22) and is given below.

$$\begin{aligned} \dot{\sigma}_i &= \lambda_i(x_{i2} + x_{\gamma 2}) - \omega_0^2(x_{i1} + Kx_{\gamma 1}) + \omega_0^2 \left(\frac{v_{dc}}{2} u_i - v_{io}^* \right) \\ \dot{\sigma}_f &= \lambda_f \left(x_{\gamma 2} - \sum_i x_{i2} \right) - \omega_0^2 K x_{\gamma 1} + \omega_0^2 \left(\frac{v_{dc}}{2} u_f - v_{fo}^* \right) \end{aligned} \quad (5.27)$$

Where,

$$\begin{aligned} v_{io}^* &= \frac{\ddot{v}_{ci}^*}{\omega_0^2} + v_{ci}^* + v_{f'o}^* + L_1 \dot{i}_{li}; \quad \omega_0^2 = \frac{1}{L_1 C_f} \\ v_{fo}^* &= -\frac{\sum_i \ddot{v}_{ci}^*}{\omega_0^2} + v_{f'o}^* + L_1 \dot{i}_{lN}; \quad i_{lN} = -\sum_i i_{li}. \end{aligned}$$

The decoupled feature of the sliding variable dynamics, as shown in (5.27), is a notable advantage compared to the conventional scheme described in (5.14). This decoupling property implies that the dynamics of the sliding variable associated with a specific phase-leg is completely independent of the control inputs of the other phase-legs. This decoupled behavior is beneficial for controller design, as it allows for the evaluation and design of each phase control input (u_j) independently, without interference from the other phase-legs.

For the control input $u_j = -sgn(\sigma_j)$, the condition (5.26) is derived as below.

Case I: $\sigma_j < 0$

This implies $u_j = 1$ and substituting it in (5.27) gives,

$$\begin{aligned} l_i &= \dot{\sigma}_i = \lambda_i(x_{i2} + x_{\gamma 2}) - \omega_0^2(x_{i1} + Kx_{\gamma 1}) + D_i > 0, \\ l_f &= \dot{\sigma}_f = \lambda_f \left(x_{\gamma 2} - \sum_i x_{i2} \right) - \omega_0^2 K x_{\gamma 1} + D_f > 0. \end{aligned} \quad (5.28)$$

Case II: $\sigma_j > 0$

This implies $u_j = -1$ and substituting it in (5.27) gives,

$$\begin{aligned} l'_i &= \dot{\sigma}_i = \lambda_i(x_{i2} + x_{\gamma 2}) - \omega_0^2(x_{i1} + Kx_{\gamma 1}) + D'_i < 0, \\ l'_f &= \dot{\sigma}_f = \lambda_f\left(x_{\gamma 2} - \sum_i x_{i2}\right) - \omega_0^2 K x_{\gamma 1} + D'_f < 0. \end{aligned} \quad (5.29)$$

Where,

$$\begin{aligned} D_j &= \omega_0^2\left(\frac{v_{dc}}{2} - v_{jo}^*\right), \\ D'_j &= \omega_0^2\left(\frac{-v_{dc}}{2} - v_{jo}^*\right). \end{aligned}$$

The two functions l_j and l'_j corresponding to each phase are defined in the same format of two parallel lines as in [50]. Using the Row Reduced Echelon form, the solution vectors of functions $\sigma_i = 0$ and $l_i = 0$; $\sigma_f = 0$ and $l_f = 0$ are S_{i1} and S_{f1} , respectively. These solution vectors can be expressed as the sum of a particular solution and a null solution.

$$S_{i1} = \begin{bmatrix} x_{i1} \\ x_{i2} \\ x_{\gamma 1} \\ x_{\gamma 2} \end{bmatrix} = \begin{bmatrix} \frac{D_i}{\lambda_i^2 + \omega_0^2} \\ -\frac{D_i \lambda_i}{\lambda_i^2 + \omega_0^2} \\ 0 \\ 0 \end{bmatrix} + x_{\gamma 1} \begin{bmatrix} -\frac{\lambda_i^2 + K \omega_0^2}{\lambda_i^2 + \omega_0^2} \\ -\frac{(1-K)\lambda_i \omega_0^2}{\lambda_i^2 + \omega_0^2} \\ 1 \\ 0 \end{bmatrix} + x_{\gamma 2} \begin{bmatrix} 0 \\ -1 \\ 0 \\ 1 \end{bmatrix} \quad (5.30)$$

$$S_{f1} = \begin{bmatrix} \sum_i x_{i1} \\ \sum_i x_{i2} \\ x_{\gamma 1} \\ x_{\gamma 2} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \frac{D_f}{\lambda_f^2 + K \omega_0^2} \\ -\frac{D_f \lambda_f}{\lambda_f^2 + K \omega_0^2} \end{bmatrix} + \sum_i x_{i1} \begin{bmatrix} 1 \\ 0 \\ \frac{\lambda_f^2}{\lambda_f^2 + K \omega_0^2} \\ \frac{\lambda_f K \omega_0^2}{\lambda_f^2 + K \omega_0^2} \end{bmatrix} + \sum_i x_{i2} \begin{bmatrix} 0 \\ 1 \\ 0 \\ 1 \end{bmatrix} \quad (5.31)$$

Similarly, the solution vectors of functions $\sigma_i = 0$ and $l'_i = 0$; $\sigma_f = 0$ and $l'_f = 0$ are S_{i2} and S_{f2} , respectively. These solution vectors can be expressed as the sum of a particular

solution and a null solution.

$$S_{i2} = \begin{bmatrix} x_{i1} \\ x_{i2} \\ x_{\gamma 1} \\ x_{\gamma 2} \end{bmatrix} = \begin{bmatrix} \frac{D'_i}{\lambda_i^2 + \omega_0^2} \\ -\frac{D'_i \lambda_i}{\lambda_i^2 + \omega_0^2} \\ 0 \\ 0 \end{bmatrix} + x_{\gamma 1} \begin{bmatrix} -\frac{\lambda_i^2 + K\omega_0^2}{\lambda_i^2 + \omega_0^2} \\ -\frac{(1-K)\lambda_i\omega_0^2}{\lambda_i^2 + \omega_0^2} \\ 1 \\ 0 \end{bmatrix} + x_{\gamma 2} \begin{bmatrix} 0 \\ -1 \\ 0 \\ 1 \end{bmatrix} \quad (5.32)$$

$$S_{f2} = \begin{bmatrix} \sum_i x_{i1} \\ \sum_i x_{i2} \\ x_{\gamma 1} \\ x_{\gamma 2} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \frac{D'_f}{\lambda_f^2 + K\omega_0^2} \\ -\frac{D'_f \lambda_f}{\lambda_f^2 + K\omega_0^2} \end{bmatrix} + \sum_i x_{i1} \begin{bmatrix} 1 \\ 0 \\ \frac{\lambda_f^2}{\lambda_f^2 + K\omega_0^2} \\ \frac{\lambda_f K\omega_0^2}{\lambda_f^2 + K\omega_0^2} \end{bmatrix} + \sum_i x_{i2} \begin{bmatrix} 0 \\ 1 \\ 0 \\ 1 \end{bmatrix} \quad (5.33)$$

From (5.30) and (5.32), it can be observed that the solution vectors S_{i1} and S_{i2} are parallel planes in the four-dimensional space defined by the variables x_{i1} , x_{i2} , $x_{\gamma 1}$, and $x_{\gamma 2}$. This parallelism arises from the fact that their null solutions are the same. Similarly, the solution vectors S_{f1} and S_{f2} are also parallel planes, but in the space defined by the variables $\sum_i x_{i1}$, $\sum_i x_{i2}$, $x_{\gamma 1}$, and $x_{\gamma 2}$. This parallelism is a result of their shared null solutions. The distances between S_{i1} and S_{i2} ; S_{f1} and S_{f2} are,

$$\begin{aligned} \overline{S_{i1} S_{i2}} &= \frac{v_{dc} \omega_0^2 \sqrt{\lambda_i^2 + 1}}{\lambda_i^2 + \omega_0^2}, \\ \overline{S_{f1} S_{f2}} &= \frac{v_{dc} \omega_0^2 \sqrt{\lambda_f^2 + 1}}{\lambda_f^2 + K\omega_0^2}. \end{aligned} \quad (5.34)$$

The values of λ_i and λ_f required for the maximum values of $\overline{S_{i1} S_{i2}}$ and $\overline{S_{f1} S_{f2}}$ respectively are,

$$\begin{aligned} \lambda_i &= \lambda_{im} = \sqrt{\omega_0^2 - 2}, \\ \lambda_f &= \lambda_{fm} = \sqrt{K\omega_0^2 - 2}. \end{aligned} \quad (5.35)$$

5.3.3 Reference Generation for DVR Compensation Voltages

The block diagram depicted in Fig. 5.4 illustrates the process of generating both the actual compensation voltages (v_{ci}) and the reference compensation voltages (v_{ci}^*). To generate the unit sine templates for the reference load voltages, the fundamental positive sequence components (FPSC) of the grid voltages (v_{gi1}^+) are extracted using a cascaded delayed signal cancellation (CDSC) operator, which was proposed in [116]. The reference load voltages (v_{li}^*) can then be determined using the following expression:

$$v_{li}^* = V_{lm}^+ \frac{v_{gi1}^+}{V_{g1m}^+}, \quad (5.36)$$

where V_{lm}^+ and V_{g1m}^+ are peak of desired load voltages and FPSC of grid voltages, respectively. The actual and reference compensation voltages are determined using (5.16), (5.17) and (5.36).

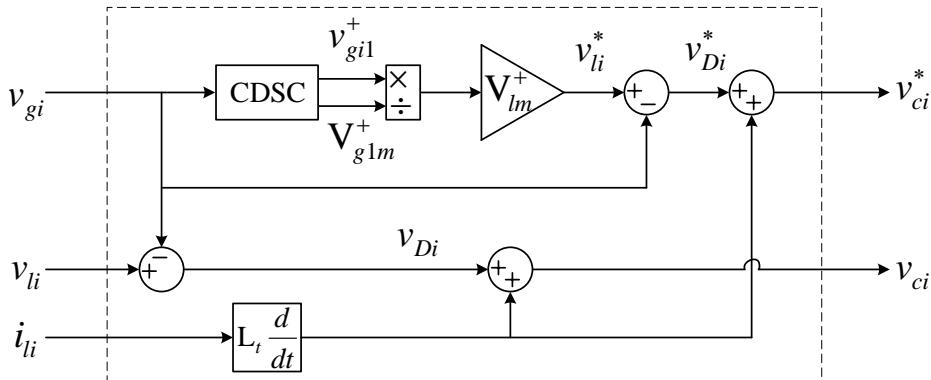


Figure 5.4: Block diagram for the generation of compensation voltages

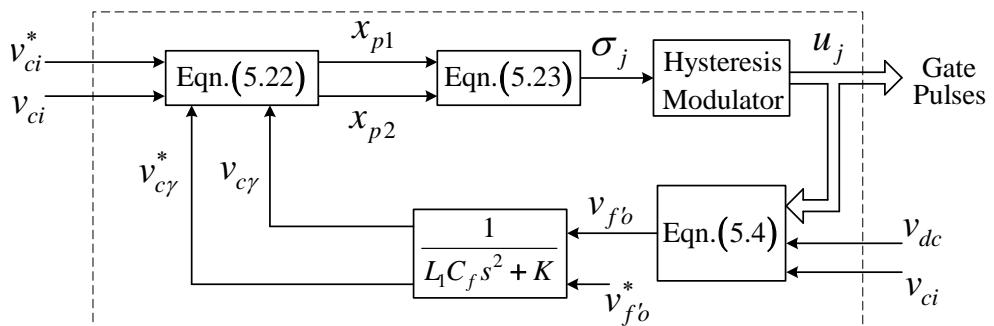


Figure 5.5: Block diagram of the proposed SMC control scheme for DVR

Table 5.2: System parameters for simulation and experimental studies

System parameters	Values
Rated supply phase voltage	50 V, 50 Hz
Filter parameters	$L_1 = 10 \text{ mH}$, $C_f = 75 \mu\text{F}$, $R_f = 3.5 \Omega$
DC-link voltage	$v_{dc} = 200 \text{ V}$
1- ϕ Transformer	1.4 kVA, 230/230 V, $L_t = 4 \text{ mH}$
Linear RL loads	$Z_a = 17 + j55.67 \Omega$ $Z_b = 50 + j58.72 \Omega$ $Z_c = 42 + j121.2 \Omega$
Resistive loads	$R_a = 48.5 \Omega$, $R_b = 32 \Omega$ $R_c = 54 \Omega$
Non-linear load	3- ϕ diode bridge rectifier with $R_{nl} = 92 \Omega$, $L_{nl} = 85.7 \text{ mH}$

The reference value for the fourth state variable, $v_{c\gamma}^*$, is generated by multiplying the user-defined value of $v_{f'o}^*$ with the transfer function $v_{c\gamma}(s)/v_{f'o}(s)$ obtained from (5.20).

This transfer function is obtained as follows:

$$v_{c\gamma}(s) = \frac{1}{L_1 C_f s^2 + K} v_{f'o}(s). \quad (5.37)$$

Fig. 5.5 illustrates the block diagram of the proposed control strategy, including the generation of the fourth state variable.

In sliding mode control (SMC), the control input (u_j) typically involves the use of the *signum* function, which is discontinuous and can lead to high switching frequencies. To mitigate this issue, various modifications to conventional SMC have been proposed in the literature, such as high-order SMC [151], robust integral of the sign of the error (RISE) control [152], and hysteresis modulators [49]. In this study, the hysteresis modulator presented below has been adopted to address this concern.

$$u_j = \begin{cases} 1 & \text{when } \sigma_j < -h \\ -1 & \text{when } \sigma_j > +h \end{cases} \quad (5.38)$$

Where h is a hysteresis band.

5.4 SIMULATION STUDIES

A simulation model of the sliding mode control based four-leg DVR has been developed using MATLAB-Simulink. The purpose of the simulation is to validate the effectiveness of the proposed control scheme in regulating the fundamental load voltage under various system conditions. The simulation is performed with a time step of $10\text{ }\mu\text{s}$ to capture the dynamics of the system accurately. The reference for the neutral-point voltage ($v_{f,o}^*$) is user-defined based on specific requirements. In this study, it is assigned an offset value of either 0 V or 50 V. The sliding variables, defined according to (5.23), are generated and used as inputs to the hysteresis modulator, which generates gate pulses for the power switches of the four-leg DVR. The system parameters, as listed in Table 5.2, are considered in the simulation model. The values of λ_i and λ_f are obtained from (5.35) as 1155 and 2160 respectively, using the given system parameters.

The simulation results provide information about various system parameters, including grid voltages (v_{gi}), load voltages (v_{li}), DVR injected voltages (v_{Di}), and load currents (i_{li}). In Fig. 5.6(a), the grid voltage anomalies are depicted. These include a fundamental balanced sag ($v_{gi} = 0.5\text{ pu}$), an unbalanced sag ($v_{ga} = 0.5\text{ pu}$), a balanced swell ($v_{gi} = 1.2\text{ pu}$), and an unbalanced swell ($v_{ga} = 1.2\text{ pu}$). These anomalies occur at different time instances, specifically at 0.5 s, 0.54 s, 0.58 s, and 0.62 s, respectively. Each voltage anomaly has a duration of 0.04 s. It is also noted that the resistive loads are not connected until $t = 0.86\text{ s}$.

Fig. 5.6(b) presents the DVR injected voltages during these grid voltage anomalies. The effectiveness of the proposed control algorithm in regulating the load voltages under fundamental grid voltage anomalies is demonstrated in Fig. 5.6(c). The four-leg DVR successfully regulates the load voltages even in the presence of unbalanced sag/swell with zero sequence components. Furthermore, Fig. 5.6(d) shows the unbalanced load currents. It can be observed that the proposed control algorithm effectively regulates the load voltages during both unbalanced sag/swell with zero sequence component and

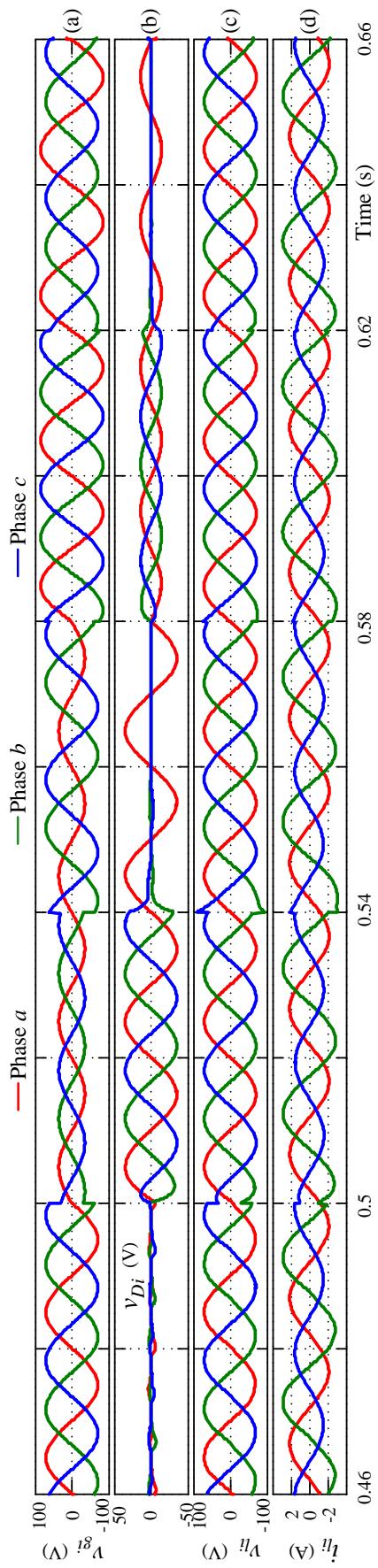


Figure 5.6: Simulation results of proposed SMC based four-leg DVR during voltage anomalies with fundamental component: (a) Grid voltages, (b) DVR injected voltages, (c) load voltages and (d) load currents

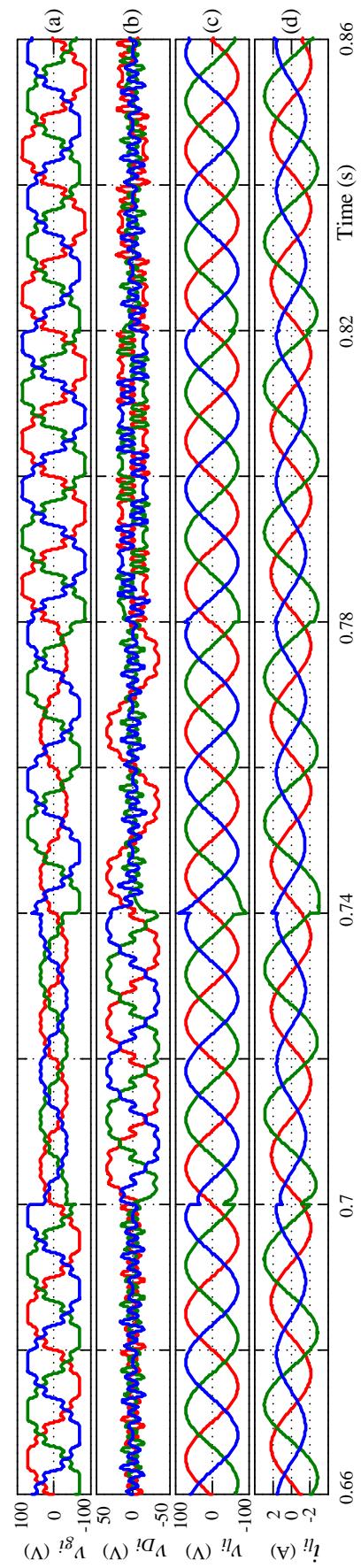


Figure 5.7: Simulation results of proposed SMC based four-leg DVR during voltage anomalies with harmonic components: (a) Grid voltages, (b) DVR injected voltages, (c) load voltages and (d) load currents

during unbalanced load currents.

In Fig. 5.7(a), various grid voltage anomalies are depicted, including harmonic distortion ($v_{gi} = 1 \text{ pu}$ and total harmonic distortion (THD) of 36.7 %), distorted balanced sag ($v_{gi} = 0.5 \text{ pu}$ and THD of 13.4 %), unbalanced sag ($v_{ga} = 0.5 \text{ pu}$ and THD of 13.4 %), balanced swell ($v_{gi} = 1.2 \text{ pu}$ and THD of 13.4 %), and unbalanced swell ($v_{ga} = 1.2 \text{ pu}$ and THD of 13.4 %). These anomalies occur at different time instances, specifically at 0.66 s, 0.7 s, 0.74 s, 0.78 s, and 0.82 s, respectively. Each voltage anomaly has a duration of 0.04 s.

Fig. 5.7(b) presents the DVR injected voltages during these grid voltage anomalies, while Fig. 5.7(c) shows the load voltages. The THDs of the load voltages during these voltage anomalies are also measured. Specifically, the THDs of load voltages are measured as 2.64 %, 0.83 %, 0.84 %, 1.41 %, and 1.45 % for the corresponding voltage anomalies mentioned above.

These simulation results provide evidence of the effectiveness of the proposed control algorithm for load voltage regulation under grid voltage anomalies with harmonic distortions. The four-leg DVR successfully mitigates the voltage distortions and maintains the desired load voltage quality, as indicated by the low THD values of the load voltages during these anomalies.

In Fig. 5.8, the effective load voltage regulation provided by the proposed SMC based four-leg DVR for a sudden load change and unbalanced sag at $t = 0.86 \text{ s}$ is demonstrated. The load voltage is regulated promptly and efficiently, maintaining the desired voltage quality despite the disturbances.

Fig. 5.9(a) shows the reference NPV, which is initially set at 50 V and then changed to 0 V at $t = 0.5 \text{ s}$. To obtain a stable NPV, the high-frequency pulsed waveform of the NPV ($v_{f'0}$) is passed through a low-pass filter (LPF) with a cutoff frequency of 15 Hz.

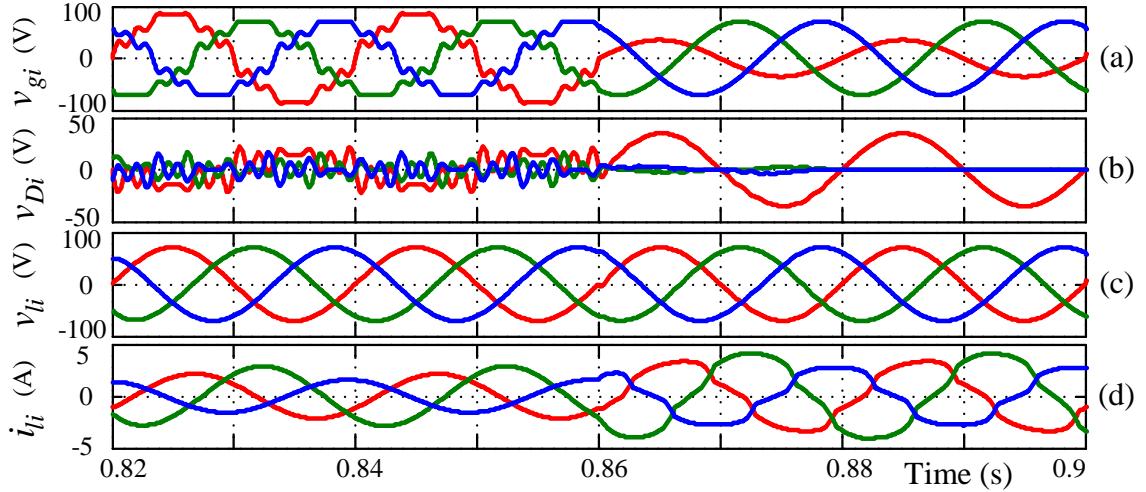


Figure 5.8: Simulation results of proposed SMC based four-leg DVR during sudden load change: (a) Grid voltages, (b) DVR injected voltages, (c) load voltages and (d) load currents

The resulting filtered voltage, referred to as the averaged NPV ($v_{f'_{o,flt}}$), is shown in Fig. 5.9(b). It can be observed that the averaged NPV tracks its reference NPV ($v_{f'_{o}}^*$) accurately.

Fig. 5.9(c)-(f) depict the state variables of the proposed control scheme. These state variables remain close to zero during all the discussed grid conditions, indicating the accurate tracking of DVR reference voltages and the reference NPV by the SMC. This demonstrates the effectiveness of the proposed control algorithm in accurately regulating both the DVR reference voltages and the NPV under various system conditions.

5.5 EXPERIMENTAL STUDIES

A prototype of a four-leg DVR system, as shown in Fig. 5.1, has been developed for experimental validation of the proposed sliding mode control (SMC) approach. The implementation of the system is depicted in Fig. 5.10. The parameters used in the experimental study are provided in Table 5.2. Based on these parameters, the values of λ_i and λ_f are determined using (5.35) as 1155 and 2160, respectively. The

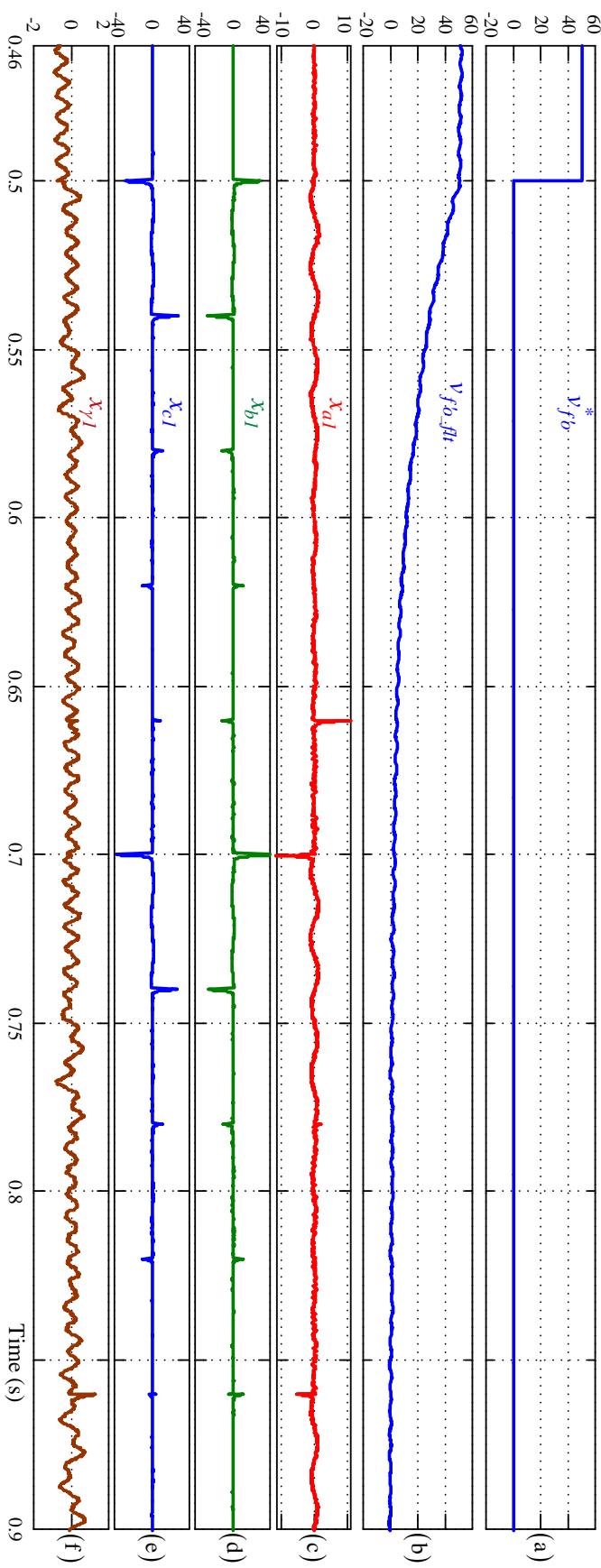


Figure 5.9: Simulation results of error state variables: (a) v_{fo}^* , (b) v_{fo_ftt} , (c) x_{a1} , (d) x_{b1} , (e) x_{c1} and (f) $x_{\gamma 1}$

four-leg voltage source converter (VSC) in the prototype system is from IGBT based SEMIKRON. Each leg of the converter is connected to an LC filter. Voltage and current signals required for control purposes are sensed using hall effect transducers and fed to a real-time controller Opal-RT OP4510 (main) and OP4520 (auxiliary) boards. The analog-to-digital converter (ADC) ports of the controller receive the sensed signals. The control algorithm is programmed with a step time of $15\ \mu\text{s}$ on the real-time controller using the RT-LAB software installed on the host PC. The real-time controller and the host PC are connected via an Ethernet cable, facilitating communication between them. This setup allows for the modification of the system parameter $v_{f'o}^*$ from the host PC during the execution of the program.

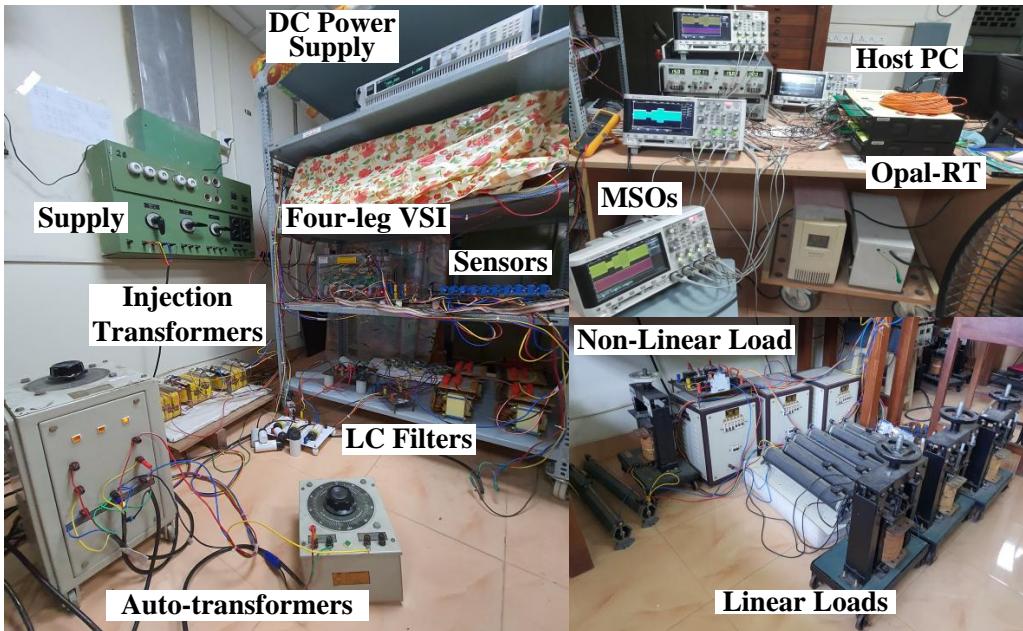


Figure 5.10: Experimental prototype of the four-leg DVR

In the experimental setup, the three-phase power supply is first stepped down to 50 V per phase using a three-phase autotransformer. To introduce various voltage anomalies, a combination of a three-phase and a single-phase autotransformer pair is employed. The results obtained for a balanced voltage sag of 0.5 pu on the grid voltage are presented in Fig. 5.11. The figure displays the grid voltages (v_{gabc}), DVR injected voltages (v_{Dabc}), load voltages (v_{labc}), and load currents (i_{labc}). Note that the load currents are not

shown for other voltage anomaly studies as they remain the same. During normal grid voltage conditions, it can be observed that the DVR injected voltages are almost zero. During the voltage sag period, the DVR injected voltages become non-zero to maintain the load voltages almost constant. This demonstrates the effectiveness of the proposed sliding mode control in mitigating voltage sags and maintaining load voltage quality. Furthermore, the total harmonic distortions (THDs) of the load voltages in phases a , b , and c are evaluated during normal grid conditions and the balanced sag condition. For normal grid conditions, the THDs of load voltages in phases a , b , and c are recorded as 2.58%, 3.36%, and 2.85%, respectively. During the balanced sag condition, the THDs of load voltages in phases a , b , and c are measured as 4.09%, 5.45%, and 4.11%, respectively. These THD values provide an indication of the load voltage distortion levels and show the effectiveness of the DVR in reducing voltage harmonics and maintaining load voltage quality even during voltage sag events.

Fig. 5.12 illustrates the behavior of the grid voltages (v_{gabc}), DVR injected voltages (v_{Dabc}), and load voltages (v_{labc}) during a balanced voltage swell event of 1.5 pu on the grid voltage. It can be observed that under normal grid voltage conditions, the DVR injected voltages are close to zero, indicating minimal compensation required. However, during the voltage swell period, the DVR injected voltages become non-zero and are phase-opposed to the grid voltages. This counteraction helps to maintain stable load voltages by compensating for the excessive grid voltage rise. Additionally, the THDs of the load voltages in phases a , b , and c are evaluated during the balanced swell condition. The THDs of load voltages in phases a , b , and c are recorded as 2.89%, 3.34%, and 2.22%, respectively. The relatively low THD values demonstrate the effectiveness of the DVR in mitigating voltage swell impacts and maintaining the quality of load voltages.

Fig. 5.13 depicts the behavior of the grid voltages (v_{gabc}), DVR injected voltages (v_{Dabc}), and load voltages (v_{labc}) during an unbalanced voltage sag event specifically on phase-

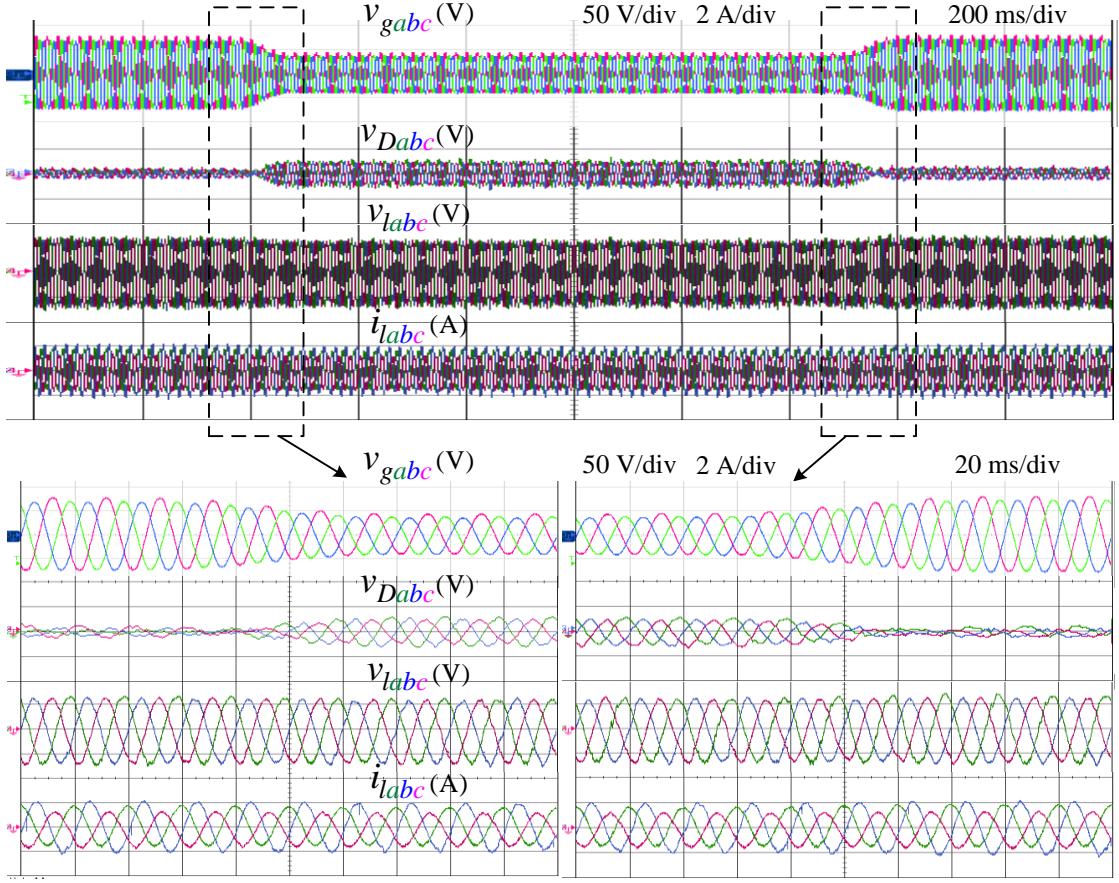


Figure 5.11: Proposed SMC based four-leg DVR during balanced sag

b grid voltage (i.e., $V_{gb} = 0.5 \text{ pu}$). From the figure, it is evident that the DVR injected voltages on phases- a and c remain close to zero throughout both normal grid voltage conditions and the unbalanced sag on grid voltages. This indicates that minimal compensation is required for phases- a and c as their grid voltages remain unaffected. However, the DVR voltage on phase- b is close to zero during normal grid voltage, but it becomes non-zero and compensates for the voltage sag on the respective phase grid voltage during the sag event. This active compensation helps in maintaining the load voltages at the desired levels, ensuring that they are not affected by the single-phase unbalanced grid voltage sag. During the unbalanced sag in phase- b grid voltage, the THDs of the load voltages in phases a , b , and c are recorded as 2.25%, 3.62%, and 2.48%, respectively. The relatively low THD values demonstrate the effectiveness of the DVR in mitigating voltage sag impacts and maintaining the quality of load voltages.

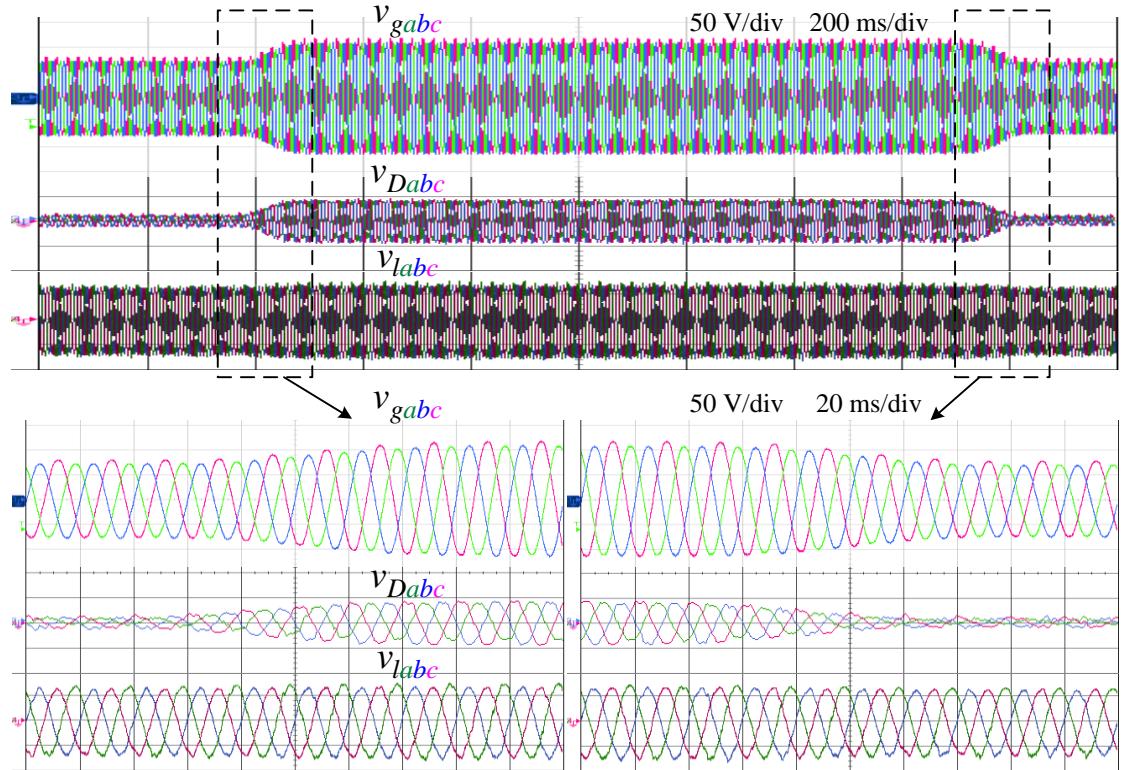


Figure 5.12: Proposed SMC based four-leg DVR during balanced swell

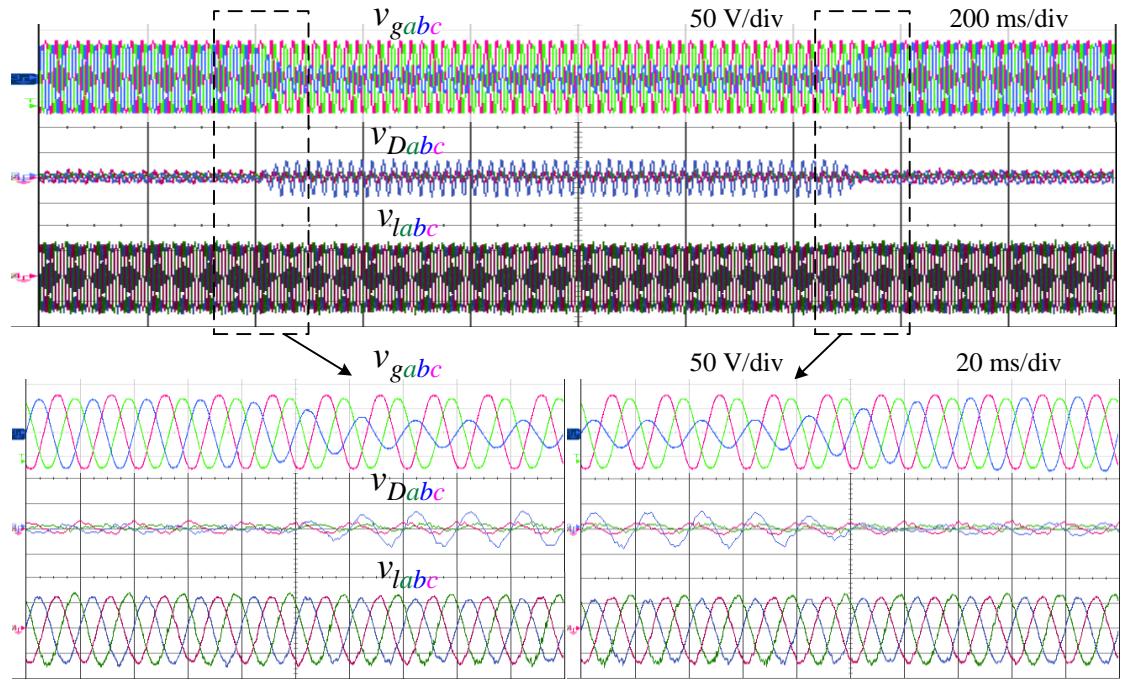


Figure 5.13: Proposed SMC based four-leg DVR during single-phase unbalanced sag

even in the presence of unbalanced grid conditions.

Fig. 5.14 displays the grid voltages (v_{gabc}), DVR injected voltages (v_{Dabc}), and load voltages (v_{labc}) during an unbalanced voltage swell event occurring on phase-*a* and phase-*c* grid voltages (i.e., $V_{ga} = V_{gc} = 1.5 \text{ pu}$). From the figure, it can be observed that the DVR injected voltage on phase-*b* remains relatively close to zero throughout both normal grid voltage conditions and the unbalanced swell on grid voltages. This indicates that minimal compensation is required for phase-*b* as its grid voltage remains unaffected by the swell event. On the other hand, the DVR voltages on phases-*a* and *c* are close to zero during normal grid voltage, but they become non-zero and actively compensate for the voltage swell on the respective phases. This active compensation ensures that the load terminal voltages are not impacted by the grid fluctuations and are maintained at the desired levels. During the unbalanced two-phase swell condition, the THDs of the load voltages in phases *a*, *b*, and *c* are recorded as 2.62%, 2.59%, and 1.81%, respectively. The relatively low THD values demonstrate the effectiveness of the DVR in mitigating voltage swell impacts and preserving the quality of load voltages even in the presence of unbalanced grid conditions.

Fig. 5.15 illustrates the behavior of various system variables and signals during different system conditions. The following time instances correspond to specific events:

1. At time t_1 , the grid experiences an unbalanced sag on phase-*b* grid voltage ($V_{gb} = 0.5 \text{ pu}$).
2. At time t_2 , the grid voltage recovers to normal mode.
3. At time t_3 , the grid encounters an unbalanced swell on phase-*b* grid voltage ($V_{gb} = 1.5 \text{ pu}$).
4. At time t_4 , the grid voltage returns to normal.
5. At time t_5 , an additional load is connected to the grid.
6. At time t_6 , the additional load is disconnected.
7. At time t_7 , the reference neutral-point voltage ($v_{f'0}^*$) is changed from 50 V to 0 V.
8. At time t_8 , the reference neutral-point voltage ($v_{f'0}^*$) is set back to 50 V.

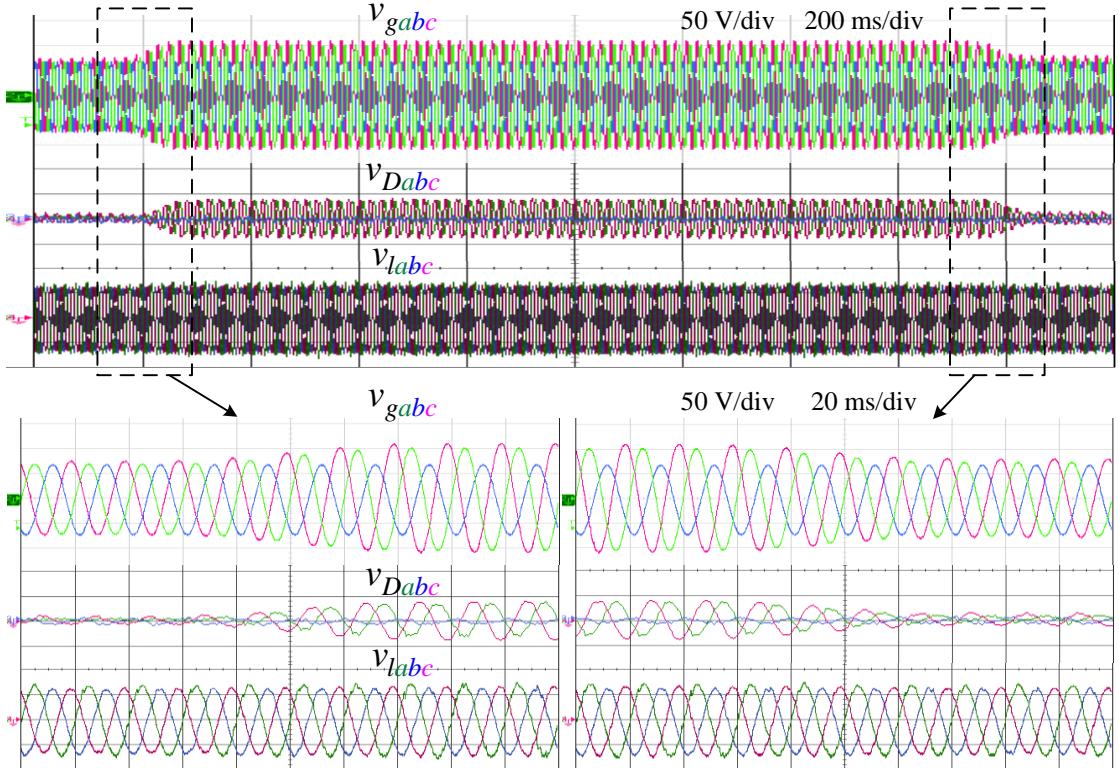


Figure 5.14: Proposed SMC based four-leg DVR during two-phase unbalanced swell

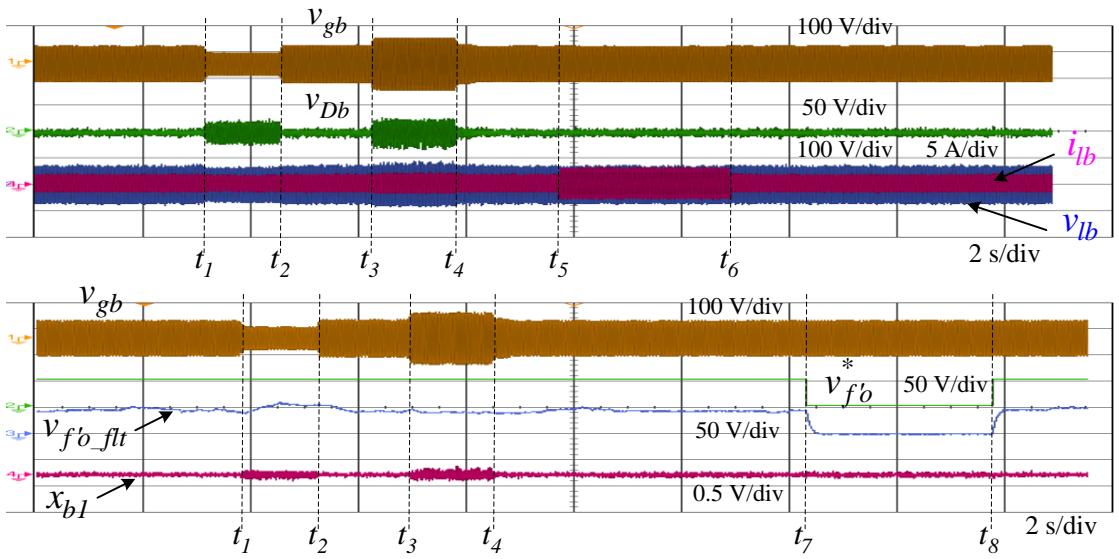


Figure 5.15: Proposed SMC based four-leg DVR during various modes of operations

Examining Fig. 5.15, it can be observed that the DVR injected voltage on phase-*b* remains close to zero during normal grid voltages, regardless of changes in load powers or the reference neutral-point voltage ($v_{f_o}^*$). However, during periods of voltage sag or swell on the phase-*b* grid voltage, the DVR voltage on phase-*b* becomes non-zero

to regulate the load voltage to the desired value. The neutral-point voltage ($v_{f'o}$) is a high-frequency pulsed waveform and is passed through a low-pass filter (LPF) with a cut-off frequency of 15 Hz. The filtered voltage, known as the averaged neutral-point voltage ($v_{f'o_flt}$), shown in Fig. 5.15, tracks its reference neutral-point voltage ($v_{f'o}^*$). The state variable x_{b1} remains close to zero for various conditions, indicating that the actual voltage v_{cb} accurately tracks its reference v_{cb}^* . Based on the observations from Fig. 5.15, it can be concluded that the proposed algorithm effectively tracks both the DVR reference voltages and the reference neutral-point voltage, ensuring proper regulation and control of the system under different operating conditions.

5.6 SUMMARY

This chapter introduces the design of sliding mode control (SMC) in the natural reference frame for a four-leg dynamic voltage restorer (DVR) using a voltage source converter. The conventional approach of assigning appropriate values to the control inputs based on sliding variables faces challenges, which are addressed by the proposed sliding variables. The proposed sliding variable for each leg of the converter is a combination of the respective filter-capacitor voltage and a fictitious voltage. The fictitious voltage is defined based on the converter's neutral-point voltage (NPV). This incorporation of the NPV control into the SMC scheme extends the control capabilities beyond just the compensation voltages of the DVR. Furthermore, the chapter presents the selection of optimum sliding coefficients to maximize the sliding existence region for the four-leg DVR. This ensures robust and effective control performance. To validate the performance of the DVR and the associated control scheme, detailed experimental studies are conducted under various operating conditions. The experimental results demonstrate the effectiveness of the proposed control approach in achieving accurate compensation performance.

Overall, the chapter provides insights into the design and implementation of SMC

for a four-leg DVR, highlighting the importance of the proposed sliding variables and the optimization of sliding coefficients for enhanced control performance. The experimental validation further strengthens the credibility of the proposed approach.

CHAPTER 6

A ROBUST CONTROL SCHEME FOR AN INTEGRATED DUAL-OUTPUT UNIFIED POWER QUALITY CONDITIONER

6.1 INTRODUCTION

In the preceding chapters, the limitations of the series converter in the unified power quality conditioner (UPQC) due to infrequent voltage-related issues in the distribution system (DG) have been explored. Consequently, the conventional back-to-back converter-based UPQC experiences reduced converter utilization. To address this issue and enhance converter utilization, a reduced switch count topology known as the dual-output converter (DOC) has been considered for UPQC application. The performance characteristics of the DOC and its control operation using linear controllers have been examined. In order to further improve performance of DOC based UPQC and ensure robustness against model inaccuracies and disturbances, a sliding mode controller (SMC) has been considered.

It has been emphasized that controlling the converter/load neutral-point voltage is essential for effectively controlling DOC-based systems. Additionally, implementing the complete control algorithm in the natural frame helps mitigate signal transformation errors and reduce computational burden to some extent. Taking all these factors into consideration, a new sliding surface-based SMC scheme has been proposed and independently evaluated on both the four-leg DSTATCOM and DVR. Since the UPQC integrates the functionalities of DSTATCOM and DVR, the proposed SMC scheme is applied to the DOC-based UPQC, and its performance is analyzed in this chapter under various grid conditions using MATLAB simulations.

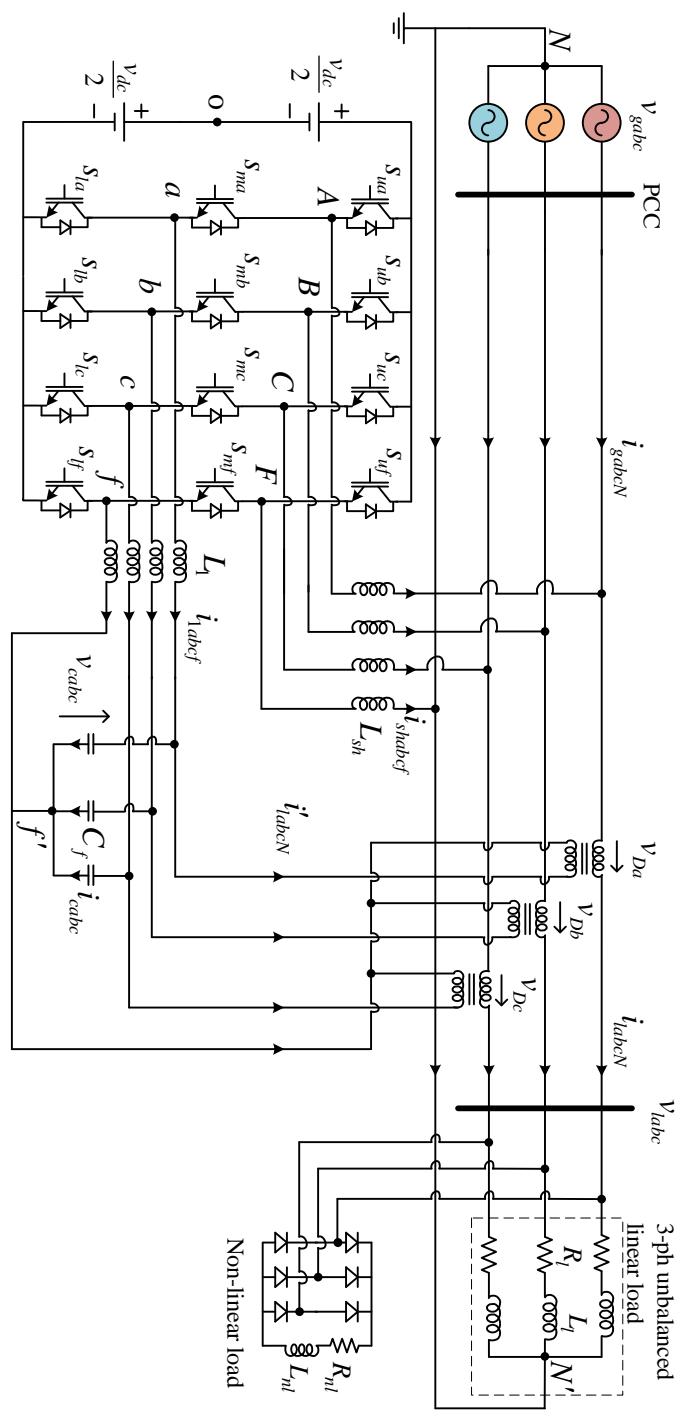


Figure 6.1: A dual output converter based UPQC-L

6.2 DESCRIPTION OF THE SYSTEM

Fig. 6.1 illustrates the schematic of a three-phase four-wire distribution system incorporating a four-leg dual-output converter-based UPQC. The control algorithm developed for the DSTATCOM is applied to the upper terminals of the dual-output converter, while the control algorithm developed for the DVR is applied to the lower terminals of the DOC.

The system consists of both a three-phase balanced linear RL load and a non-linear load comprising a diode bridge rectifier with an RL load. The shunt compensator current (i_{shabcf}) is regulated by employing a shunt filter inductor L_{sh} , and the series compensator voltage (v_{Dabc}) is regulated using an LC filter comprising inductor L_1 and capacitor C_f . The dual-output converter is connected to a stiff DC source, assuming that the DC-link voltage does not exhibit any dynamics.

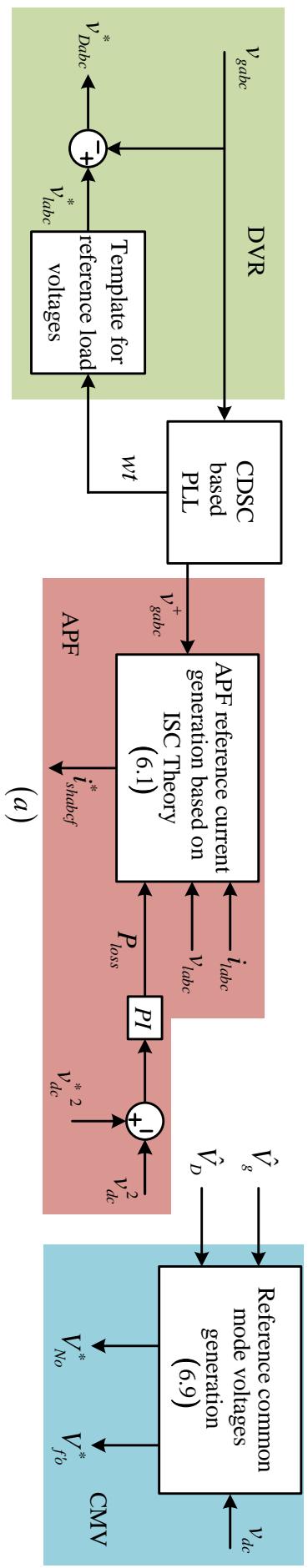
The notations and model equations introduced for the DSTATCOM in Chapter 4 are used for the upper ports of the dual-output converter, while the notations and model equations introduced for the DVR in Chapter 5 are used for the lower ports of the dual-output converter.

6.3 PROPOSED CONTROL SCHEME

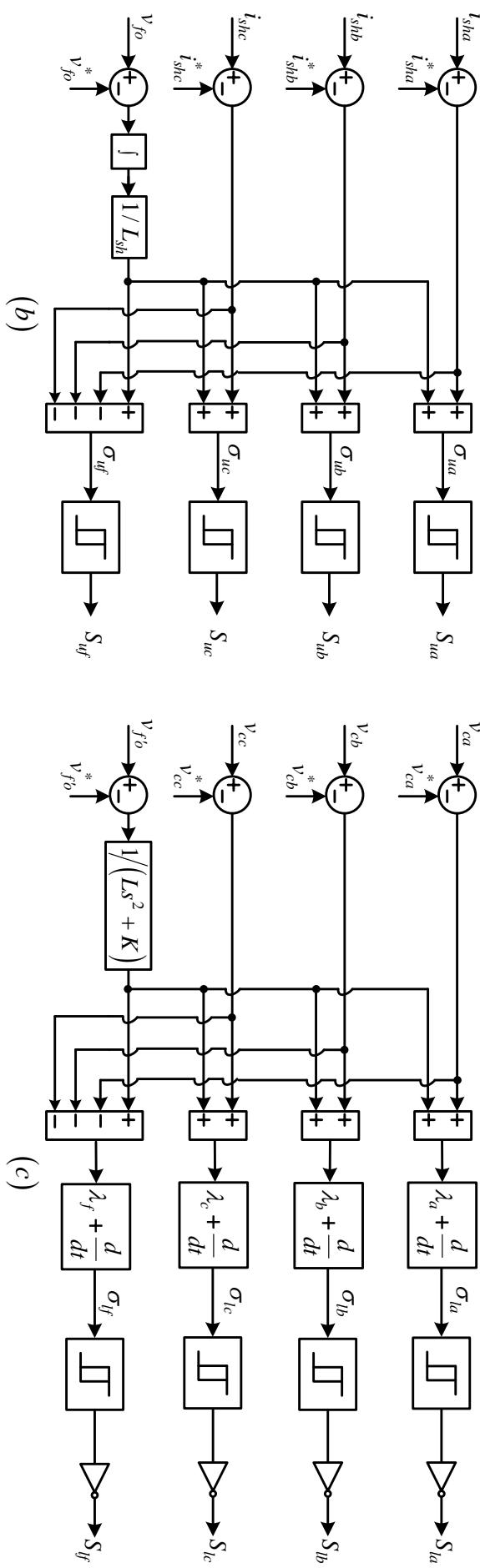
The control algorithm consists of two main components: the generation of reference quantities, such as compensator currents, compensator voltages, and neutral-point voltages, and the implementation of a sliding mode controller.

6.3.1 Generation of Reference Quantities

The complete block diagram of the required reference generations for sliding mode control are shown in Fig. 6.2(a). The reference currents for shunt APF are generated



(a)



(b)

(c)

Figure 6.2: Control schematics: (a) Reference generation, (b) Upper switches gating pulse generation, and (c) Lower switches gating pulse generation

using instantaneous symmetrical component theory (ISCT) discussed in Chapter 2. In order to achieve unity power factor operation at the grid, the variable γ^+ is substituted with zero in (2.45). The resultant expressions for the reference currents are as follows:

$$\begin{aligned} i_{shi}^* &= i_{li} - \frac{v_{gi}^+}{\sum_{k=a,b,c} (v_{gk}^+)^2} (P_{lavg} + P_{loss}) \quad \forall i \in \{a, b, c\}, \\ i_{shf}^* &= - \sum_{i=a,b,c} i_{shi}^*, \end{aligned} \quad (6.1)$$

where, P_{lavg} and P_{loss} are average load power and converter power losses respectively. The fundamental positive sequence components of grid voltages, v_{gj}^+ are extracted using CDSC operator. The converter power loss component is found from the mismatch in the DC-link voltage with its reference voltage using linear PI controller. The gains of controller are computed based on fast acting DC-link voltage controller, ensuring a rapid transient response [137]. It is worth noting that when a stiff DC source is utilized, the PI controller is not necessarily required. However, it is included in Fig. 6.2(a) for general understanding.

For the extraction of the grid voltage angle, a phase-locked loop (PLL) based on the CDSC operator, proposed in [123], is employed. This PLL offers superior performance compared to the commonly used second order generalized integrator (SOGI) based PLL, as discussed in Chapter 3. By utilizing the extracted phase angle, a reference template for load voltages is defined. The DVR reference voltages are then generated by subtracting the grid voltages from the defined load voltage template. The expression for DVR reference voltages based on the in-phase compensation scheme is defined as follows:

$$v_{Di}^* = v_{li}^* - v_{gi} \quad \forall i \in \{a, b, c\}. \quad (6.2)$$

In Chapter 2, it was discussed that offsets are added to both the modulating signals of the upper port and the lower port in order to avoid any intersection between the two

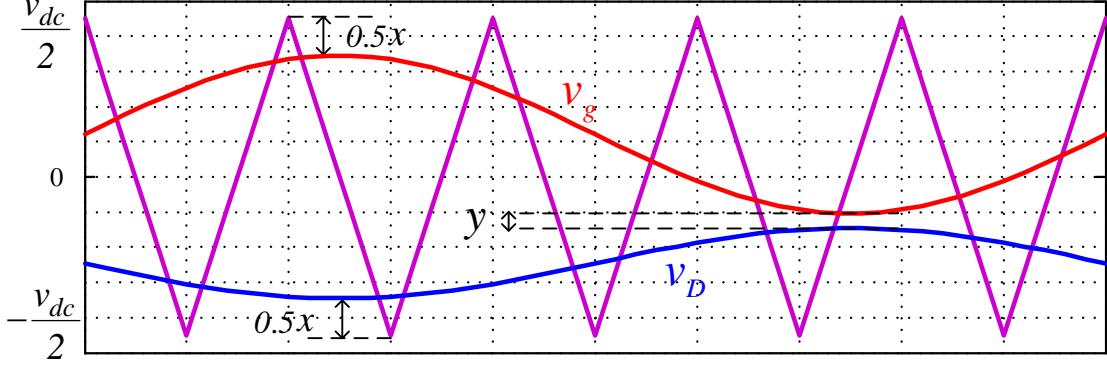


Figure 6.3: Illustration of PWM logic of DOC based UPQC-L for reference NPV calculations

modulating signals. Additionally, the offset ensures that the upper modulating signal is always higher than the lower modulating signal. These offsets contribute to the control of the respective neutral-point voltages (NPVs).

To gain a better understanding of this concept and to derive expressions for the reference quantities of the NPVs, the pulse width modulation (PWM) requirements for the DOC based UPQC-L are presented in Fig. 6.3. In the case of the UPQC-L, the upper port is utilized for DSTATCOM operation, and its voltage is approximately the same as the voltage at the point of common coupling (PCC). Hence, the modulating signal of the upper port is represented as v_g in Fig. 6.3. On the other hand, the lower port of the UPQC-L is employed for DVR operation, and its voltage is the difference between the desired load voltage (v_l^*) and the PCC voltage (v_g). Consequently, the modulating signal of the lower port is denoted as v_D in Fig. 6.3. The offsets or reference NPVs are added to these modulating signals to satisfy the following conditions, which ensure the generation of valid switching states for the DOC-based UPQC-L system.

1. Ensuring that the positive peak of the upper modulating signal is within the positive peak of the carrier signal, thus avoiding over modulation issues. This can be mathematically stated as follows:

$$\begin{aligned} V_{No}^* + \hat{V}_g &\leq \frac{v_{dc}}{2}, \\ \Rightarrow V_{No}^* &= \frac{v_{dc}}{2} - \hat{V}_g - \frac{x}{2}, \end{aligned} \tag{6.3}$$

where V_{No}^* represents the reference NPV for upper port, \hat{V}_g represents the positive peak of the grid/PCC voltage, and x represents the sum of free space available between the positive peak of upper modulating signal and positive peak of carrier signal, as well as the free space available between the negative peak of lower modulating signal and the negative peak of carrier signal. In Fig. 6.3, it is assumed that the free space at the positive peak of carrier is same as the free space at the negative peak of the carrier.

2. Ensuring that the negative peak of the lower modulating signal is within the negative peak of the carrier signal, thereby avoiding over modulation issues. This can be mathematically stated as follows:

$$\begin{aligned} V_{f'o}^* - \hat{V}_D &\geq -\frac{v_{dc}}{2}, \\ \Rightarrow V_{f'o}^* &= -\frac{v_{dc}}{2} + \hat{V}_D + \frac{x}{2}, \end{aligned} \quad (6.4)$$

where $V_{f'o}^*$ represents the reference NPV for lower port, and \hat{V}_D represents the absolute/positive peak of the DVR voltage reference.

3. Ensuring that the upper modulating signal is always higher than the lower modulating signal. This can be realized mathematically as given below:

$$\begin{aligned} V_{No}^* - \hat{V}_g &\geq V_{f'o}^* + \hat{V}_D, \\ \Rightarrow V_{No}^* &= V_{f'o}^* + \hat{V}_D + \hat{V}_g + y, \end{aligned} \quad (6.5)$$

where y represents the free space between the negative peak of upper modulating signal and the positive peak of the lower modulating signal. This space can be as low as possible compared to the space x . In this study, y is considered as 0.2 times the value of x , i.e.,

$$y = 0.2x. \quad (6.6)$$

By substituting (6.3) and (6.4) into (6.5), the total free space can be obtained as below:

$$x + y = v_{dc} - 2(\hat{V}_g + \hat{V}_D). \quad (6.7)$$

By substituting (6.6) into (6.7), the following is obtained:

$$x = \frac{v_{dc} - 2(\hat{V}_g + \hat{V}_D)}{1.2}. \quad (6.8)$$

Ensuring the positive values for free space is crucial. By substituting $\hat{V}_D = |\hat{V}_l^* - \hat{V}_g|$ into (6.8), the range of compensation voltage that maintains a positive free space can be determined. The notation \hat{V}_l^* represents the positive peak of the desired load voltage. The condition for achieving a positive free space is given as below.

$$v_{dc} > 2(\hat{V}_g + |\hat{V}_l^* - \hat{V}_g|) \quad (6.9)$$

During the voltage sag conditions, where $\hat{V}_l^* > \hat{V}_g$, the condition that needs to be satisfied is:

$$v_{dc} > 2\hat{V}_l^*. \quad (6.10)$$

Typically, the DC-link voltage is selected in a way that satisfies the above condition. This indicates that the DOC based UPQC can perform all of its functions satisfactorily during the voltage sag conditions. On the other hand, during the voltage swell conditions, where $\hat{V}_l^* < \hat{V}_g$, (6.9) is modified as below.

$$\begin{aligned} v_{dc} &> 2(\hat{V}_g + \hat{V}_g - \hat{V}_l^*) \\ \frac{v_{dc}}{2} &> 2\hat{V}_g - \hat{V}_l^* \\ \hat{V}_g &< \frac{0.5v_{dc} + \hat{V}_l^*}{2} \end{aligned} \quad (6.11)$$

Therefore, the maximum voltage swell that can be compensated by the DOC based UPQC is $\frac{0.5v_{dc} + \hat{V}_l^*}{2}$.

The reference NPVs of upper port and lower port can be obtained by substituting (6.8) into (6.3) and (6.4), respectively, as given below:

$$\begin{aligned} V_{No}^* &= \frac{1}{12} \left\{ v_{dc} - 2\hat{V}_g + 10\hat{V}_D \right\}, \\ V_{f'o}^* &= \frac{1}{12} \left\{ -v_{dc} - 10\hat{V}_g + 2\hat{V}_D \right\}. \end{aligned} \quad (6.12)$$

6.3.2 Implementation of Proposed SMC

The sliding variables proposed for DSTATCOM in Chapter 4 and the sliding variables proposed for DVR in Chapter 5 are redefined in this section. By substituting (4.10) into (4.12), the sliding variables for the upper port of DOC based UPQC-L are defined as follows:

$$\sigma_{uj} = (i_{shj} - i_{shj}^*) + \frac{1}{L_{sh}} \int (v_{No} - v_{No}^*) dt; \quad \forall j \in \{a, b, c, f\}. \quad (6.13)$$

For each leg of the DOC in the upper port, there are four sliding variables. For phase-*a* leg, the sliding variable, σ_{ua} is considered and it is passed to a hysteresis modulator to generate switching pulses for the upper switch of DOC. When σ_{ua} crosses the upper hysteresis band, the top switch S_{ua} is turned OFF. Conversely, when σ_{ua} crosses the lower hysteresis band, the top switch is turned ON. If σ_{ua} is within the hysteresis band, the state of the switch remains unchanged. The same principle applies to the other legs of DOC. The complete implementation of SMC for the upper port of DOC based UPQC-L is shown in Fig. 6.3(b).

Similarly, by substituting (5.22) into (5.23), the sliding variables for the lower port of DOC based UPQC-L can be defined as follows:

$$\sigma_{lj} = \left(\lambda_j + \frac{d}{dt} \right) \left\{ (v_{cj} - v_{cj}^*) + (v_{c\gamma} - v_{c\gamma}^*) \right\}; \quad \forall j \in \{a, b, c, f\}, \quad (6.14)$$

where $v_{cf} = -\sum_{k=a,b,c} v_{ck}$, and $v_{cf}^* = -\sum_{k=a,b,c} v_{ck}^*$. The fictitious voltages $(v_{c\gamma}, v_{c\gamma}^*)$ are obtained from (5.37), which is given as below.

$$V_{c\gamma}(s) = \frac{1}{Ls^2 + K} V_{f'o}(s) \quad (6.15)$$

Where $L = L_1 C_f$, and $K = (1 + \frac{L_1}{L_t})$.

For each leg of the DOC in the lower port, there are four sliding variables. For phase-*a* leg, the sliding variable, σ_{la} is considered and it is passed to a hysteresis modulator to generate switching pulses for the lower switch of DOC. When σ_{la} crosses the upper hysteresis band, the bottom switch S_{la} is turned ON. Conversely, when σ_{la} crosses the lower hysteresis band, the bottom switch is turned OFF. If σ_{la} is within the hysteresis band, the state of the switch remains unchanged. The same principle applies to the other legs of DOC. The complete implementation of SMC for lower port of DOC based UPQC-L is shown in Fig. 6.3(c).

The switching state for the middle switches (S_{mj}) is obtained by performing NAND operation on the switching state of upper switches (S_{uj}) and lower switches (S_{lj}). This can be realized mathematically as follows:

$$S_{mj} = \overline{S_{uj} \cdot S_{lj}} \quad \forall j \in \{a, b, c, f\}. \quad (6.16)$$

6.4 SIMULATION STUDIES

The MATLAB/Simulink tool is used to model the four-leg dual output converter based UPQC shown in Fig. 6.1, along with the proposed sliding mode control. The simulation considers the system parameters listed in Table 6.1. Based on these parameters and (6.11), the maximum voltage swell that can be compensated by the DOC-based UPQC is 387.5 V (peak) or 1.1923 pu. To validate the proposed control method, a simulation study is conducted for various grid voltage disturbances. Each event is considered for

Table 6.1: System parameters

System parameters	Simulation values
Rated supply phase voltage	230 V, 50 Hz
Filter parameters	$L_{sh} = 20 \text{ mH}$, $L_t = 3 \text{ mH}$ $L_1 = 5 \text{ mH}$, $C_f = 30 \mu\text{F}$
DC-link voltage	$v_{dc} = 900 \text{ V}$
Sliding surface coefficients	$\lambda_i = 2582$, $\lambda_f = 4145$
Linear load	$Z_a = 200 + j60 \Omega$, $Z_b = 60 + j55 \Omega$, $Z_c = 30 + j25 \Omega$
Nonlinear load	3- ϕ diode bridge rectifier with $R_{nl} = 40 \Omega$; $L_{nl} = 0.5 \text{ H}$
Injection transformer	230 V, 33 kVA, turns ratio 1:1

a duration of 0.06 s to ensure visual clarity and accommodate all voltage-related events in a plot.

In Fig. 6.4, the occurrence of a balanced voltage sag ($V_g = 0.5 \text{ pu}$), an unbalanced voltage sag in phase- a ($V_{ga} = 0.5 \text{ pu}$), and a balanced voltage swell ($V_g = 1.1 \text{ pu}$) are considered at 0.5 s, 0.56 s, and 0.62 s, respectively. In Fig. 6.5, the occurrence of an unbalanced voltage swell in phase- a ($V_{ga} = 1.1 \text{ pu}$), a balanced voltage swell ($V_g = 1.2 \text{ pu}$), and an unbalanced voltage swell in phase- a ($V_{ga} = 1.2 \text{ pu}$) are considered at the time instants of 0.68 s, 0.74 s and 0.8 s, respectively. All these voltage anomalies have a fundamental frequency component. A distorted grid is considered at time 0.86 s as shown in Fig. 6.5.

Figs. 6.6-6.8 display various system signals for voltage anomalies with harmonic components. In Fig. 6.6, a balanced voltage sag ($V_g = 0.5 \text{ pu}$), an unbalanced voltage sag in phase- a ($V_{ga} = 0.5 \text{ pu}$), a balanced voltage swell ($V_g = 1.1 \text{ pu}$), and an unbalanced voltage swell in phase- a ($V_{ga} = 1.1 \text{ pu}$) are considered at 0.92 s, 0.98 s, 1.04 s and 1.1 s, respectively. In Fig. 6.8, a balanced voltage swell ($V_g = 1.2 \text{ pu}$) and an unbalanced voltage swell in phase- a ($V_{ga} = 1.2 \text{ pu}$) are considered at the time instants of 1.16 s, and 1.22 s, respectively.

The simulation results demonstrate that the proposed control scheme exhibits fast

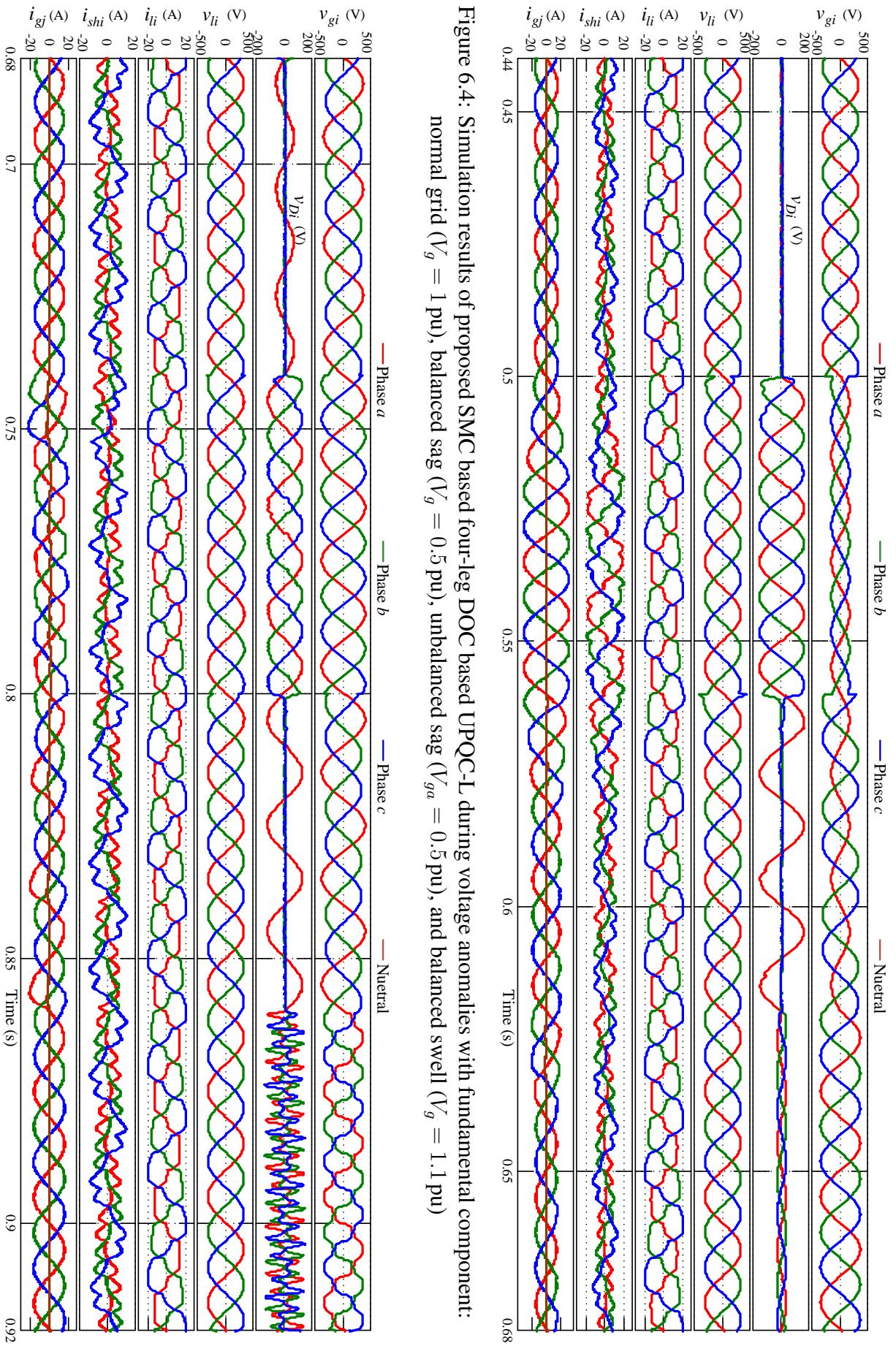


Figure 6.4: Simulation results of proposed SMC based four-leg DOC based UPQC-L during voltage anomalies with fundamental component: normal grid ($V_g = 1$ pu), balanced sag ($V_g = 0.5$ pu), unbalanced sag ($V_{ga} = 0.5$ pu), and balanced swell ($V_g = 1.1$ pu)

Figure 6.5: Simulation results of proposed SMC based four-leg DOC based UPQC-L during voltage anomalies with fundamental component: unbalanced swell ($V_{ga} = 1.1$ pu), balanced swell ($V_g = 1.2$ pu), unbalanced swell ($V_{ga} = 1.2$ pu) and distorted grid

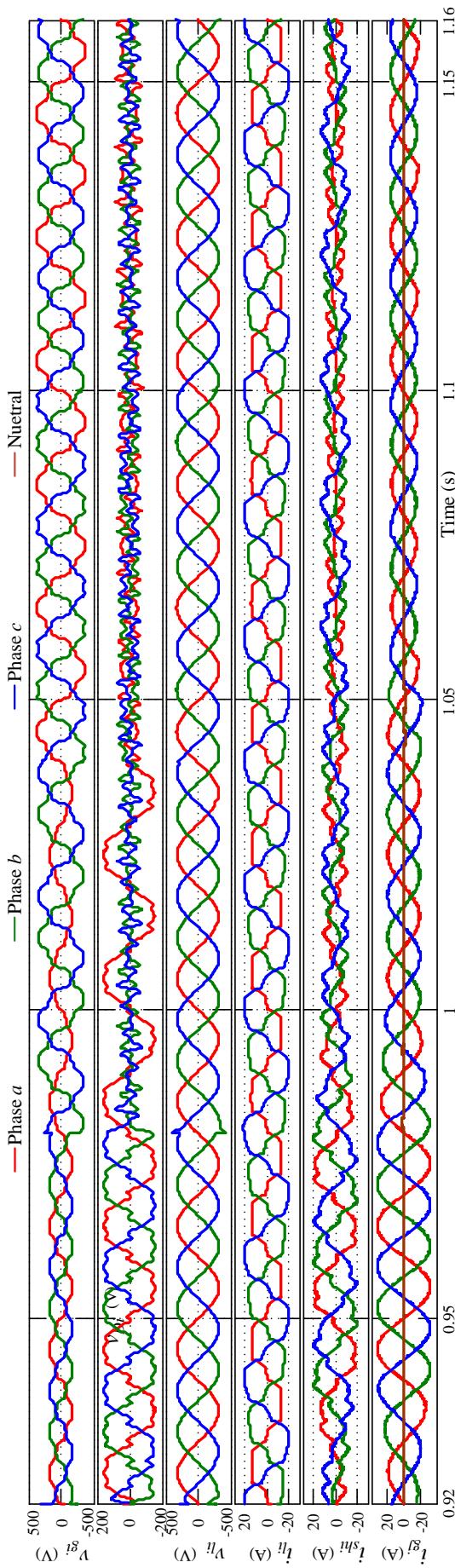


Figure 6.6: Simulation results of proposed SMC based four-leg DOC based UPQC-L during voltage anomalies with harmonic components: balanced sag ($V_g = 0.5 \text{ pu}$), unbalanced sag ($V_g = 0.5 \text{ pu}$), and unbalanced swell ($V_g = 1.1 \text{ pu}$)

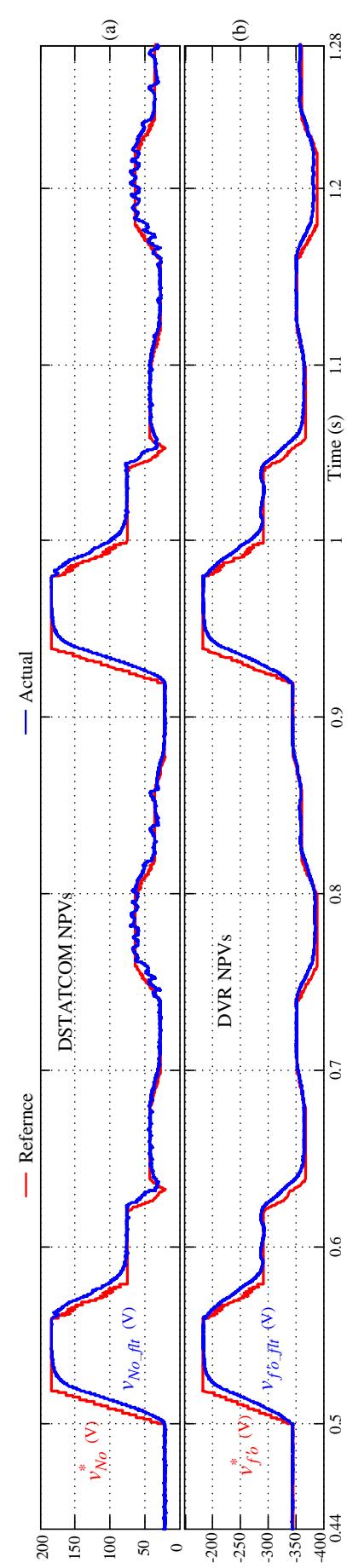


Figure 6.7: Simulation results of proposed SMC based four-leg DOC based UPQC-L during various voltage anomalies: reference and averaged NPVs of (a) DSTATCOM, and (b) DVR

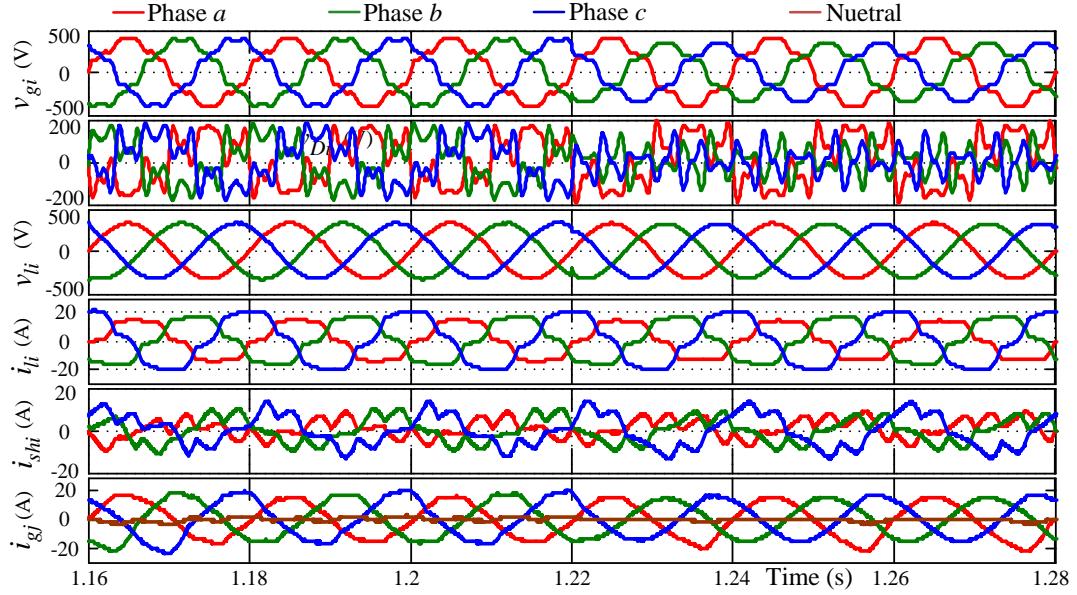


Figure 6.8: Simulation results of proposed SMC based four-leg DOC based UPQC-L during voltage anomalies with harmonic components: balanced swell ($V_g = 1.2 \text{ pu}$), and unbalanced swell ($V_{ga} = 1.2 \text{ pu}$)

response and effectively regulates the converter to fulfill the functionalities of both the DSTATCOM and DVR, namely ensuring load voltage regulation and load balancing. The current through the grid neutral (i_{gN}) is observed to be zero, indicating that the shunt terminals of the UPQC system supply the load neutral current. However, during a voltage swell of 1.2 pu, regardless of whether it is balanced or unbalanced, the compensator currents do not meet the required accuracy. This discrepancy arises due to the violation of the condition stated in (6.11).

Additionally, the tracking performance of averaged neutral-point voltages (NPVs) with their reference values can be observed from Fig. 6.7. This demonstrates that the proposed scheme effectively controls both the NPVs, and the compensator voltages and currents.

6.5 SUMMARY

The sliding mode control (SMC) scheme, previously introduced in the earlier chapters, is implemented in a dual-output converter-based UPQC-L system. Analytical expressions are derived for the reference neutral-point voltages (NPVs) of both the shunt and series terminals of the DOC-based UPQC-L system. Additionally, an expression is derived to determine the maximum value of voltage swell that the UPQC system can compensate. This limitation defines the range of voltage swell that can be effectively mitigated by the DOC-based UPQC-L system. To expand the compensation range for voltage swells, the DC-link voltage needs to be increased.

To assess and verify the effectiveness of the proposed SMC scheme, a comprehensive simulation study is conducted. This study evaluates the performance of the control scheme under various scenarios, including both balanced and unbalanced upstream fault conditions. The simulation results provide insights into the behavior of the DOC based UPQC-L system and demonstrate the efficiency of the proposed SMC scheme in addressing power quality issues.

CHAPTER 7

CONCLUSIONS AND FUTURE SCOPES

In this chapter, concise descriptions of the important contributions made in this thesis, along with conclusions and possibilities for future work, are presented.

7.1 SUMMARY

The interconnection of renewable energy sources and the increased utilization of non-linear loads, powered by semiconductor switching devices, has led to a decline in power quality (PQ) in distribution networks. Various factors such as symmetrical and asymmetrical faults, lightning, and environmental conditions further decrease the reliability of distributed generation (DG) systems, causing voltage variations such as sag, swell, and interruptions. Moreover, the non-linear loads draw distorted currents from the grid through the feeder impedance, leading to voltage distortions at the point of common coupling (PCC). This distortion can be harmful to sensitive loads connected at that point, potentially causing damage. To address these challenges, custom power devices (CPD), specifically the unified power quality conditioner (UPQC), have been introduced.

The conventional back-to-back (BTB) topology of the UPQC has been effective in addressing both current and voltage-related PQ issues. However, a drawback of the BTB configuration is that the series converter is idle for a significant portion of the time, as voltage-related problems occur less frequently. This leads to poor utilization of the converter. To enhance the converter utilization factor without compromising the UPQC's ability to generate the required voltages and currents, recent research has focused on developing a new configuration called the dual-output converter (DOC) based UPQC. In this topology, the traditional back-to-back arrangement is replaced by a reduced switch count converter topology, such as dual-output converter.

The control of custom power devices such as the UPQC requires a suitable controller capable of handling both fundamental and harmonic signals. Linear proportional-integral (PI) controllers are commonly used for tracking DC signals accurately. However, they are not sufficient for UPQC control as UPQC deals with fundamental and multiple harmonic signals. While proportional-resonant (PR) controllers can accurately track specific frequency signals for which the PR gains are tuned, they are limited to a single frequency. To process the wide range of frequencies encountered in UPQC applications, multiple PR controllers are often paralleled with a PI controller. This parallel arrangement increases design complexity. Alternatively, non-linear controllers are capable of handling signals at any frequency, provided the processor's sampling rate is sufficiently low. Therefore, non-linear controllers can be developed in any reference frame. Additionally, since UPQC contains non-linear components like power semiconductor switches, non-linear controllers are well-suited for UPQC control. Among the available non-linear controllers, sliding mode controller (SMC) is often considered due to its robustness against parameter variations and model mismatches.

These considerations have motivated the development of a complete control algorithm in the natural frame itself for the DOC based UPQC system. The unique topological characteristics of the DOC necessitate not only the control of compensator currents and voltages but also the control of neutral-point voltages (NPV). To achieve NPV control within the sliding mode controller framework, a novel sliding surface has been proposed for both the four-leg distribution static compensator (DSTATCOM) and the four-leg dynamic voltage restorer (DVR). To assess the performance of the proposed control scheme, extensive simulation and experimental studies have been conducted under various grid conditions for both the four-leg DSTATCOM and the four-leg DVR. These studies validate the effectiveness of the control scheme in regulating the compensator currents, voltages, and NPV, demonstrating its robustness and ability to enhance power quality.

Furthermore, the proposed control scheme has been extended to the DOC based UPQC-L configuration, where the shunt compensator is positioned on the left side (grid side) of the UPQC. A novel reference generation approach has been proposed for the neutral-point voltages in the UPQC-L application. Through simulation studies, the performance of the proposed control scheme for the four-leg DOC based UPQC-L has been evaluated, verifying its effectiveness and suitability for maintaining power quality and mitigating grid disturbances.

The DOC-based UPQC-L configuration offers the advantage of compensating voltage sags with reduced switch counts compared to the back-to-back (BTB) configuration. However, it has a limitation in its voltage swell compensation capability when using the same DC-link voltage as the BTB configuration. To enhance the voltage swell compensation capability of the DOC-based UPQC-L system, the DC-link voltage needs to be increased.

On the other hand, the BTB configuration provides a full range of voltage swell compensation capability but at the cost of additional switches. This means that the BTB configuration can effectively handle a wide range of voltage swells without limitations. However, this advantage comes with the drawback of requiring a higher number of switches, which increases the complexity and cost of the system.

Therefore, the choice between the DOC-based UPQC-L configuration and the BTB configuration depends on the specific requirements of the application. If the voltage swell compensation range is a critical factor and cost is not a major concern, the BTB configuration may be preferred. On the other hand, if reducing switch counts and cost are important considerations, the DOC-based UPQC-L configuration can be a suitable option, even though it has limitations in voltage swell compensation.

The major outcomes of the thesis are listed below:

1. The phase angle of the grid voltages is determined using the traditional synchronous reference frame phase locked loop (SRF-PLL). However, it accurately computes angles only for fundamental balanced voltages. When dealing with disturbed voltages, the incorporation of a low-bandwidth controller is necessary, but this tends to result in a sluggish response from PLL. To overcome this challenge, various pre-filters such as second order generalized integrator (SOGI), cascaded delayed signal cancellation (CDSC) and multiple delayed signal cancellation (MDSC) have been reviewed and compared. Through the comparative analysis, it has been observed that CDSC is the preferred choice due to its requirement of fewer delay operations, lower computational intensity and accurate performance in handling various voltage disturbances.
2. While developing a conventional sliding mode control scheme for four-leg VSI based systems in the natural reference frame, it has been analytically demonstrated that the conventional scheme encounters a challenges in generating switching pulses. This difficulty arises due to the coupling of dynamics in the sliding variable on each phase through all phase pole voltages.
3. In order to tackle the inherent coupling issue among the phases, a novel sliding surface has been proposed. This surface is defined as the sum of DSTATCOM current and current resulting from the neutral point voltage (NPV) for current compensation. Additionally, for voltage compensation, the sliding surface is the sum of DVR voltage and voltage due to NPV. The effectiveness of the proposed control scheme has been validated through simulation and experimental studies on a four-leg DSTATCOM and DVR. Since the UPQC is a combination of DSTATCOM and DVR, the proposed control scheme is also applicable to conventional back-to-back (BTB) converter based UPQC.
4. The series converter in BTB configuration remains inactive for a significant duration since voltage-related problems are less frequent. This results in

suboptimal utilization of the converter. In order to improve the converter utilization factor without compromising the UPQC's ability to generate the required voltages and currents, an analysis is conducted using a dual output converter (DOC) based UPQC-L with the proposed control scheme through simulation studies. However, it's worth noting that the DOC based UPQC-L exhibits a limitation in its ability to compensate for voltage swells when employing the same DC-link voltage as the BTB configuration. To enhance the voltage swell compensation capability, it becomes necessary to increase the DC-link voltage.

7.2 SCOPE FOR FUTURE RESEARCH

The application of dual-out converter to power system applications can be further explored and enhanced in the following ways:

- **Fault-Tolerant Feature:** Incorporating fault-tolerant features into the dual-output converter (DOC) topology is crucial for ensuring reliable operation of the UPQC or any other application based on the DOC. This can involve the development of fault detection, isolation, and recovery mechanisms to maintain system performance and stability in the presence of faults. Research efforts can focus on improving the fault-handling capabilities of the DOC-based UPQC to enhance the reliability of the system.
- **Integration of PV and/or Battery Storage Units:** The configuration of a DOC-based UPQC-L system can be extended to include the integration of photovoltaic (PV) and/or battery storage units. This investigation involves studying the performance of the proposed control scheme in a multi-functional UPQC that combines load voltage regulation, load balancing, and renewable energy integration. The objective is to optimize the utilization of PV and battery storage systems in conjunction with the DOC-based UPQC-L to enhance power

quality, mitigate voltage fluctuations, and maximize the utilization of renewable energy sources.

APPENDIX A

SIMPLIFIED EXPLANATION OF THE PROPOSED CONTROL SCHEME

In a current controlled inverter or DSTATCOM, the inverter/compensator current is regulated based on the voltage of its filter inductor. Referring to Fig. 4.1, the voltage across filter inductor in phase-*a* is given as below.

$$v_{Lsha} = L_{sh} \frac{di_{sha}}{dt} = (v_{ao} - v_{No}) - v_{ga} \quad (\text{A.1})$$

This clearly indicates that in order to achieve a positive slope of the compensator current, the inductor voltage should be positive, and vice versa. It can also be concluded that the sign of inductor voltage is changed by controlling the term $(v_{ao} - v_{No})$. From (4.2), it can be stated that the voltage v_{No} depends on all the pole voltages v_{ao} , v_{bo} , v_{co} , and v_{fo} . The pole voltages have a value of $+\frac{v_{dc}}{2}$ when the corresponding top switch of the leg is turned ON, and $-\frac{v_{dc}}{2}$ when the top switch is turned OFF. Therefore, it is not possible to control the switches on the phase-*a* leg alone to change the sign of the inductor voltage, since $(v_{ao} - v_{No})$ depends on all switch states. This is due to the presence of v_{No} . By transforming the above equation to the *dq* frame, the *dq* equivalent of v_{No} does not exist, and thus the sign of the inductor voltage in the *dq* frame is controlled by the *dq* equivalent of v_{ao} . Hence, it becomes straightforward to generate switching pulses for the switches in phase-*a* leg and similarly in other legs.

However, if the circuit diagram of DSTATCOM system is redrawn while preserving its dynamics, as shown in Fig. A.1, the selection of switching pulses would become simpler. In this figure, the neutral-point voltage (NPV), v_{No} is represented based on the expression given in (4.10), i.e., $v_{No} = L_{sh} \frac{0.25i_{sh}\gamma}{dt}$. From the Fig. A.1, the voltage across

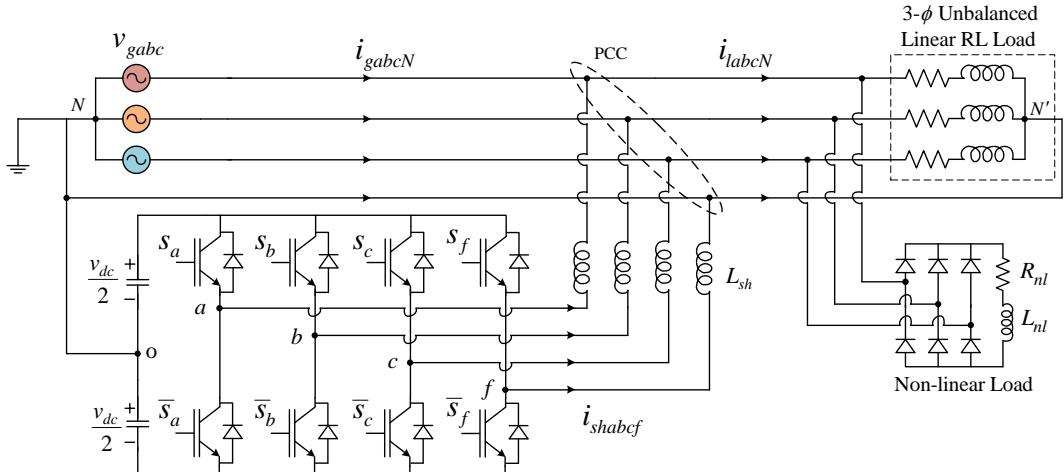


Figure A.1: Equivalent schematic diagram of a four-leg voltage source converter based DSTATCOM

filter inductor in phase- a is given as below.

$$v'_{Lsha} = L_{sh} \frac{d}{dt} \left\{ i_{sha} + 0.25i_{sh\gamma} \right\} = v_{ao} - v_{ga} \quad (\text{A.2})$$

This clearly indicates that the sign of inductor voltage is changed by controlling v_{ao} alone. Therefore, to achieve a positive sign of inductor voltage, the top switch of the respective leg, in this case the phase- a leg, should be turned ON. This action sets the pole voltage v_{ao} to $+\frac{v_{dc}}{2}$. Similarly, to obtain a negative sign of inductor voltage, the top switch should be turned OFF. In summary, by controlling $(i_{sha} + 0.25i_{sh\gamma})$ instead of i_{sha} alone, the selection of switching pulses becomes easier. Thus, the sliding surface is proposed as $\sigma_a = (i_{sha} + 0.25i_{sh\gamma}) - (i_{sha}^* + 0.25i_{sh\gamma}^*)$ for the DSTATCOM system.

The similar analysis is carried out for the DVR system shown in Fig. 5.1. In a voltage controlled inverter or DVR, the inverter/compensator voltage is controlled by the voltage across its filter capacitor. The capacitor voltage is controlled by its current, which is determined by the voltage across the filter inductor. The inductor voltage is, in turn, controlled by the state of switches. Referring to Fig. 5.1, the voltage across the

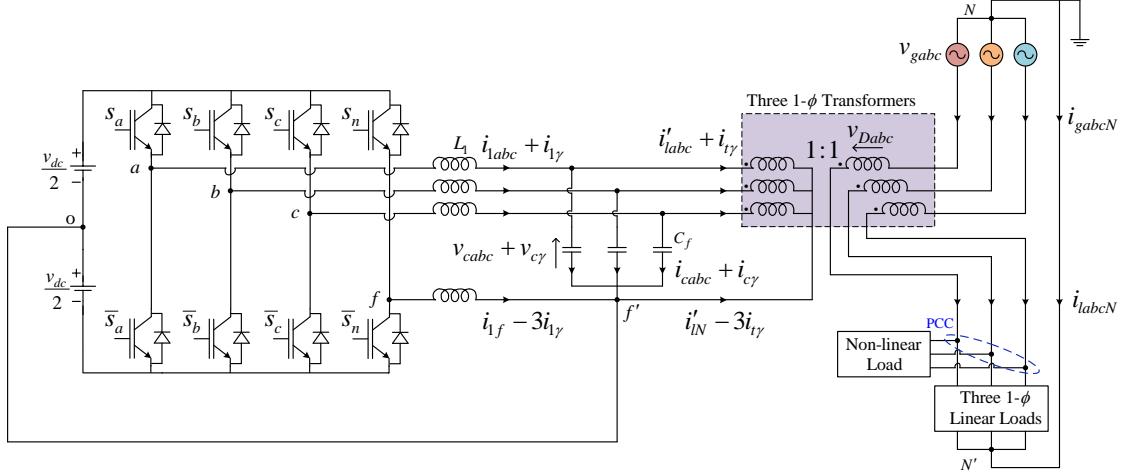


Figure A.2: Equivalent schematic diagram of a four-leg voltage source converter based DVR

filter inductor in phase-*a* is given as below.

$$\begin{aligned}
 v_{L1a} &= L_1 \frac{di_{1a}}{dt} = (v_{ao} - v_{f'o}) - v_{ca} \\
 &= L_1 \frac{d}{dt} \left\{ i_{ca} + i_{l'a} \right\} = (v_{ao} - v_{f'o}) - v_{ca} \\
 &= L_1 \frac{di_{ca}}{dt} = (v_{ao} - v_{f'o}) - v_{ca} - \frac{L_1}{L_t} \left\{ v_{ca} + v_{Da} \right\} \\
 &= L_1 C_f \frac{d^2 v_{ca}}{dt^2} = (v_{ao} - v_{f'o}) - \left\{ 1 + \frac{L_1}{L_t} \right\} v_{ca} - \frac{L_1}{L_t} v_{Da}
 \end{aligned} \tag{A.3}$$

This equation indicates that to have a positive slope of inductor current, the inductor voltage should be positive and vice versa. It also implies that the sign of the inductor voltage can be changed by controlling $(v_{ao} - v_{f'o})$ while keeping v_{ca} and v_{Da} known. From (5.3), it can be stated that the voltage $v_{f'o}$ depends on all the pole voltages v_{ao} , v_{bo} , v_{co} , and v_{fo} . The pole voltages have a value of $+\frac{v_{dc}}{2}$ when the corresponding top switch of the leg is turned ON and $-\frac{v_{dc}}{2}$ when the top switch is turned OFF. Therefore, controlling the switches on the phase-*a* leg alone cannot change the sign of the inductor voltage since $(v_{ao} - v_{f'o})$ depends on all the states of switches.

If the circuit diagram of DVR system is redrawn while preserving its dynamics as shown in Fig. A.2, the selection of switching pulses would become simpler. In this modified figure, the neutral-point voltage (NPV), $v_{f'o}$ is represented based on the expression

given in (5.20). From the Fig. A.2, the voltage across filter inductor in phase-*a* is given as below.

$$\begin{aligned}
v'_{L1a} &= L_1 \frac{d}{dt} \left\{ i_{1a} + i_{1\gamma} \right\} = v_{ao} - (v_{ca} + v_{c\gamma}) \\
&= L_1 \frac{d}{dt} \left\{ i_{ca} + i_{c\gamma} + i_{l'a} + i_{t\gamma} \right\} = v_{ao} - (v_{ca} + v_{c\gamma}) \\
&= L_1 \frac{d}{dt} \left\{ i_{ca} + i_{c\gamma} \right\} = v_{ao} - (v_{ca} + v_{c\gamma}) - \frac{L_1}{L_t} \left\{ v_{ca} + v_{c\gamma} + v_{Da} \right\} \\
&= L_1 C_f \frac{d^2}{dt^2} \left\{ v_{ca} + v_{c\gamma} \right\} = v_{ao} - \left\{ 1 + \frac{L_1}{L_t} \right\} (v_{ca} + v_{c\gamma}) - \frac{L_1}{L_t} v_{Da}
\end{aligned} \tag{A.4}$$

This equation reveals that the sign of inductor voltage or the sign of the slope of $v_{ca} + v_{c\gamma}$ can be changed by controlling v_{ao} alone. Therefore, to obtain a positive sign of inductor voltage or a positive slope of $v_{ca} + v_{c\gamma}$, the top switch of respective leg (in this case, phase-*a* leg) should be turned ON. This action sets the pole voltage v_{ao} to $+\frac{v_{dc}}{2}$. Similarly, to achieve a negative sign of inductor voltage or negative slope of $v_{ca} + v_{c\gamma}$, the top switch should be turned OFF. In summary, by controlling $(v_{ca} + v_{c\gamma})$ instead of v_{ca} alone, the selection of switching pulses becomes easier. Therefore, the proposed sliding surface for the DVR system is $\sigma_a = \left(\lambda_a + \frac{d}{dt} \right) x_a$, where $x_a = (v_{ca} + v_{c\gamma}) - (v_{ca}^* + v_{c\gamma}^*)$.

APPENDIX B

LIMITATIONS OF A THREE-WIRE DVR IN DISTRIBUTION SYSTEM

In previous chapters, it is discussed that the dynamic voltage restorer (DVR) is connected to the distribution feeder through the single-phase injection transformers. The primaries of the transformers can be connected in three configurations such as delta, star with isolated neutral and star with neutral connected to filter capacitors neutral point, as shown in Fig. B.1. This appendix focuses on evaluating the performance of a three-wire DVR using these three transformer configurations.

The delta configuration is widely recognized for enabling the flow of zero sequence current but does not facilitate zero sequence voltage injection. Consequently, this configuration adversely affects the DVR's ability to compensate and regulate load voltage during unbalanced voltage sag/swell situations that involve zero sequence voltage components. On the other hand, the two star configurations allow for zero sequence voltage injection. However, the star configuration with an isolated neutral does not provide a path for zero sequence current flow. As a result, the DVR fails to regulate load voltage for unbalanced loads, regardless of the type of voltage disturbance.

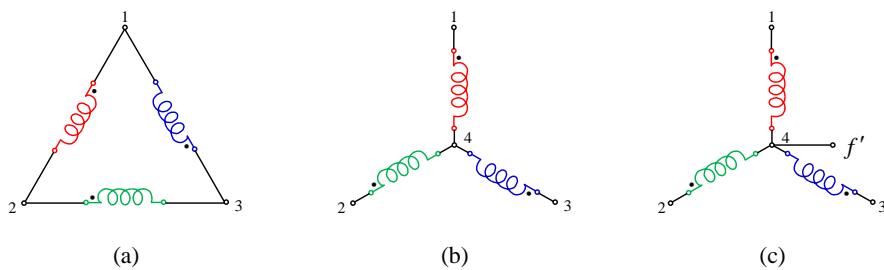


Figure B.1: Transformer primary winding configurations: (a) Delta, (b) Star with isolated neutral and (c) Star with neutral connected to filter capacitors neutral

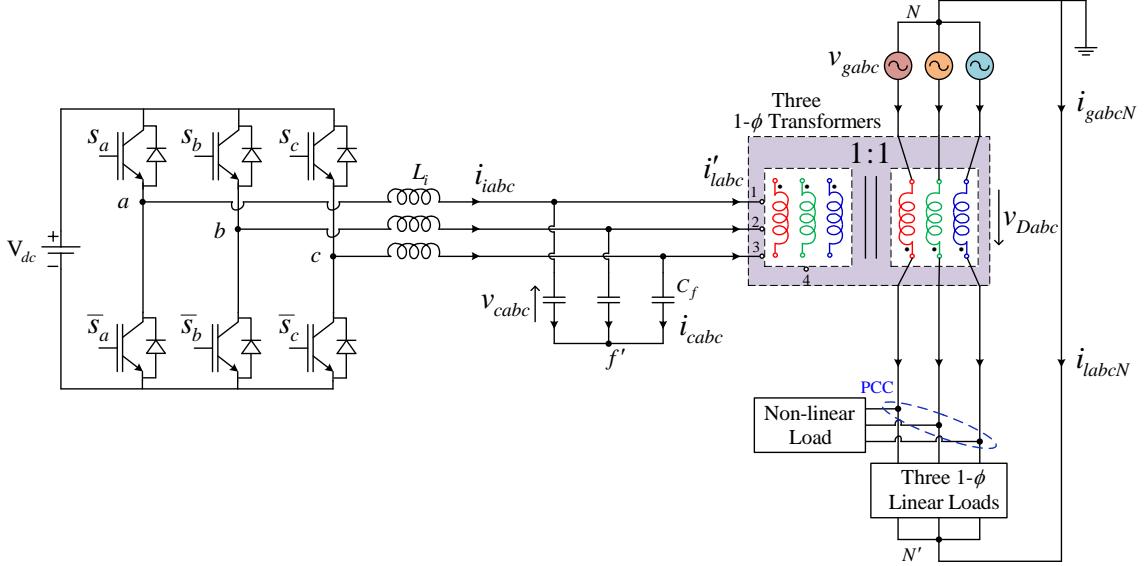


Figure B.2: Schematic diagram of three-leg voltage source converter based DVR

Table B.1: System parameters for simulation study

System parameters	Values
Rated supply phase voltage	230 V, 50 Hz
Filter parameters	$L_f = 5 \text{ mH}$, $C_f = 30 \mu\text{F}$
DC link voltage	$V_{dc} = 900 \text{ V}$
1 – ϕ Transformer	50 kVA, 230/230 V, $L_t = 1.5 \text{ mH}$
Unbalanced linear load	$Z_a = 1.7 + j5.567 \Omega$, $Z_b = 50 + j58.72 \Omega$, $Z_c = 5.25 + j15.15 \Omega$
Balanced linear load	$Z_a = Z_b = Z_c = 17 + j55.67 \Omega$

In the case of the other star configuration, although it allows for the flow of zero sequence current, the presence of filter capacitors prevents this current flow due to their low impedance specifically designed for switching frequency components. This causes the DVR to also fail in regulating load voltage for unbalanced loads with this particular configuration. To verify these conclusive statements, simulation results obtained from MATLAB-Simulink are utilized.

The proposed control scheme in Chapter 5 is extended to the three-wire DVR connected in a distribution system as shown in Fig. B.2. The system parameters considered for the simulation study are listed in Table B.1.

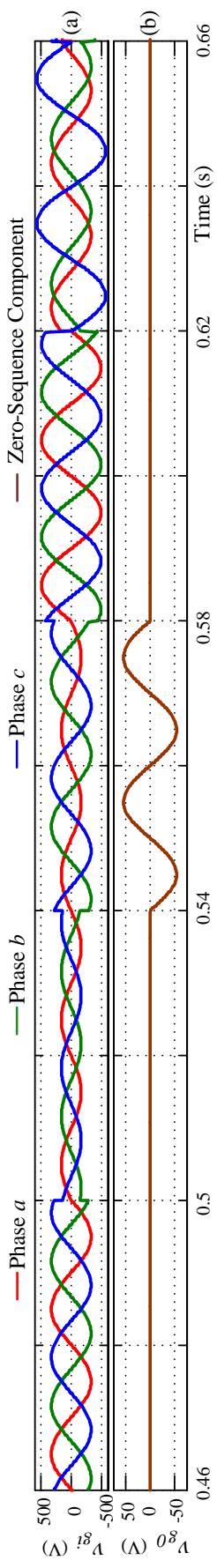


Figure B.3: Simulation results: (a) Grid voltages and (b) Zero sequence component of grid voltages

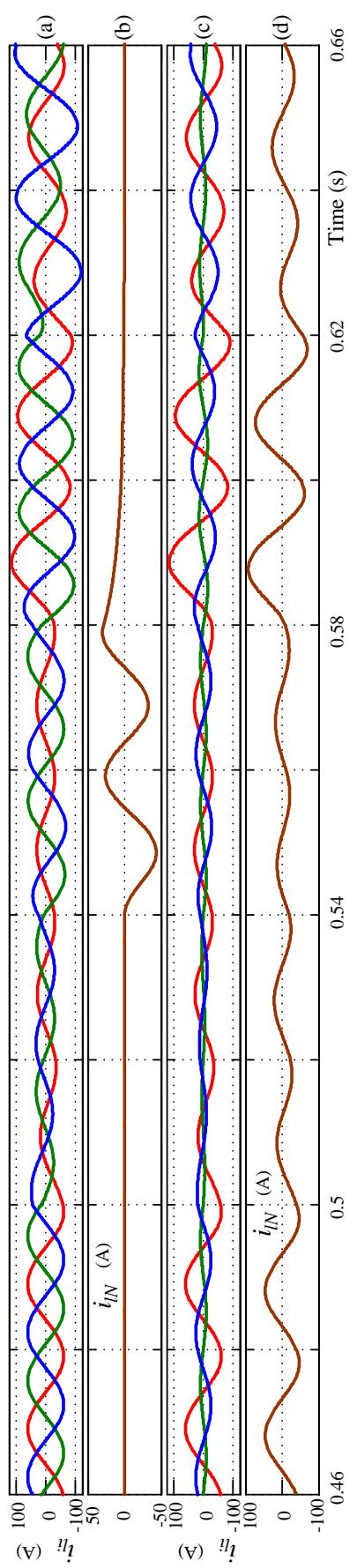


Figure B.4: Simulation results in the absence of DVR; The load currents (i_{hi}) and its neutral current (i_{IN}): (a) & (b) Balanced load, and (c) & (d) Unbalanced load

The simulation results include several system parameters, namely grid voltages (v_{gi}), load voltages (v_{li}), DVR injected voltages (v_{Di}), load currents (i_{li}), transformer primary currents (i'_{li}), and zero sequence components of grid voltages (v_{g0}) and load currents (i_{LN}). In Fig. B.3(a), the grid voltage anomalies are presented, including fundamental balanced sag ($v_{gi} = 0.5$ pu), unbalanced sag ($v_{ga} = 0.5$ pu), balanced swell ($v_{gi} = 1.5$ pu), and unbalanced swell with no zero sequence component ($v_{ga} = 1\angle 30^\circ$ pu, $v_{gb} = 1\angle -30^\circ$ pu, $v_{gc} = \sqrt{3}\angle 180^\circ$ pu). These anomalies occur at specific time instances: 0.5 s, 0.54 s, 0.58 s, and 0.62 s, respectively. Each voltage anomaly lasts for a duration of 0.04 s. It is important to note that the same grid voltage profile is utilized for studying the DVR with each transformer configuration. Additionally, Fig. B.3(b) indicates that the zero sequence component exists in the grid voltage only during the period of unbalanced sag. Furthermore, Fig. B.4 displays the load currents for both balanced and unbalanced loads in the absence of the DVR.

Fig. B.5 illustrates the DVR injected voltages and load voltages for both balanced and unbalanced loads in the case of the delta configuration. It can be observed that, regardless of load unbalance, the DVR effectively regulates the load voltage for all voltage anomalies except during the period of unbalanced sag. This observation provides clear evidence that the DVR with the delta configuration is unable to mitigate unbalanced voltage disturbances with zero sequence components.

Fig. B.6(a)-(c) depict the DVR injected voltages, load voltages, and transformer primary currents for a balanced load in the case of star with isolated neutral configuration. Similarly, Fig. B.6(d)-(f) represent the same parameters for an unbalanced load. Likewise, in the case of the star configuration with the neutral connected to the filter capacitors, Fig. B.7(a)-(c) showcase the DVR injected voltages, load voltages, and transformer primary currents for a balanced load, while Fig. B.7(d)-(f) depict the same for an unbalanced load.

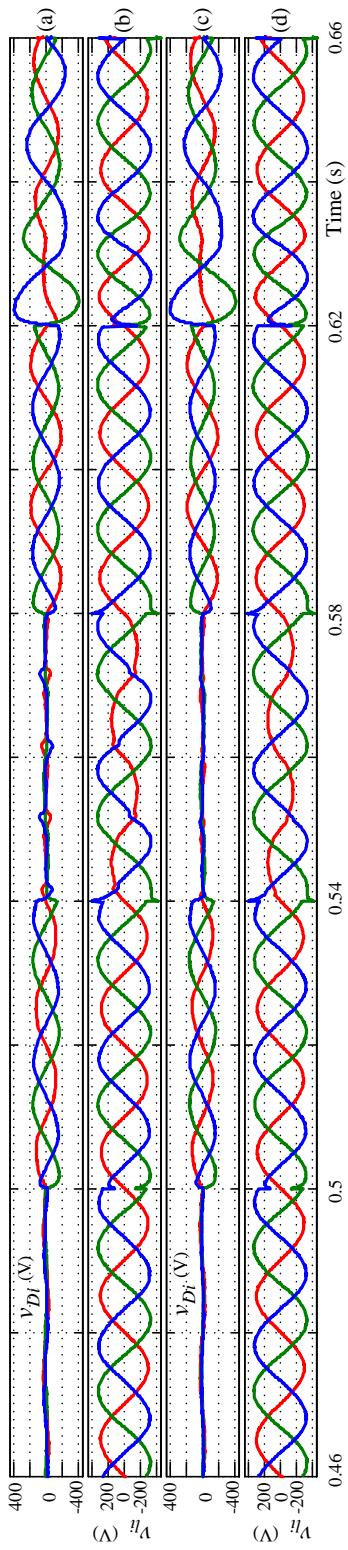


Figure B.5: Simulation results for a delta configuration; The DVR voltages (v_{Di}) and load voltages (v_{li}): (a) & (b) Balanced load, and (c) & (d) Unbalanced load

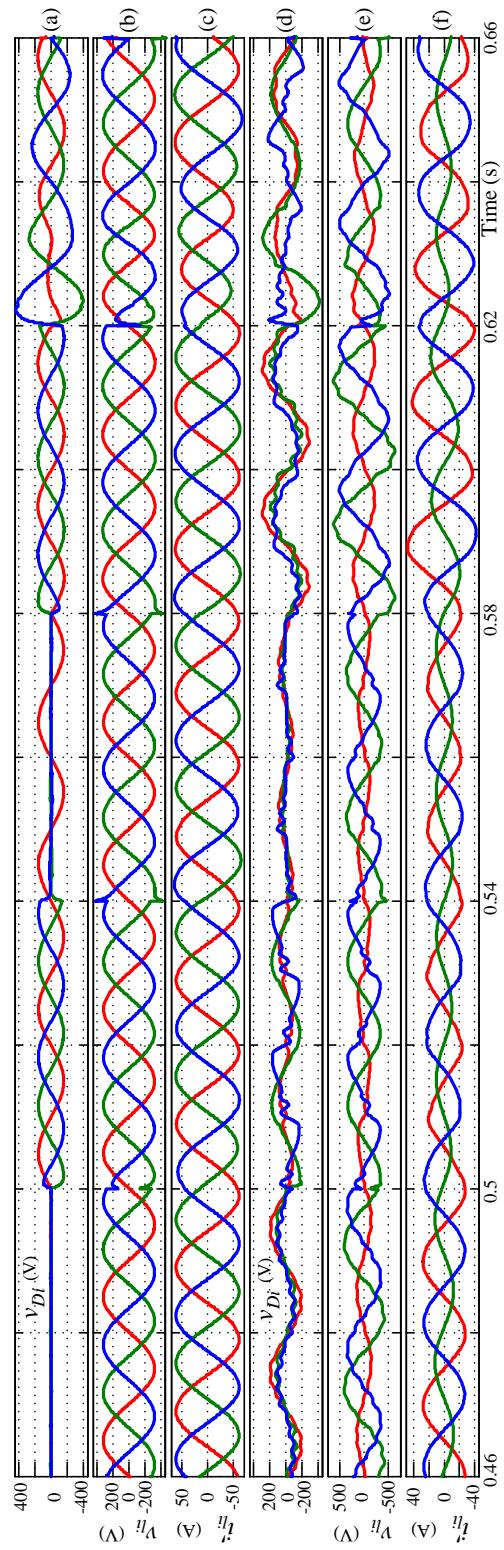


Figure B.6: Simulation results for a star with isolated neutral configuration; The DVR voltages (v_{Di}), load voltages (v_{li}) and transformer primary currents (i'_{li}): (a), (b) & (c) Balanced load, and (d), (e) & (f) Unbalanced load

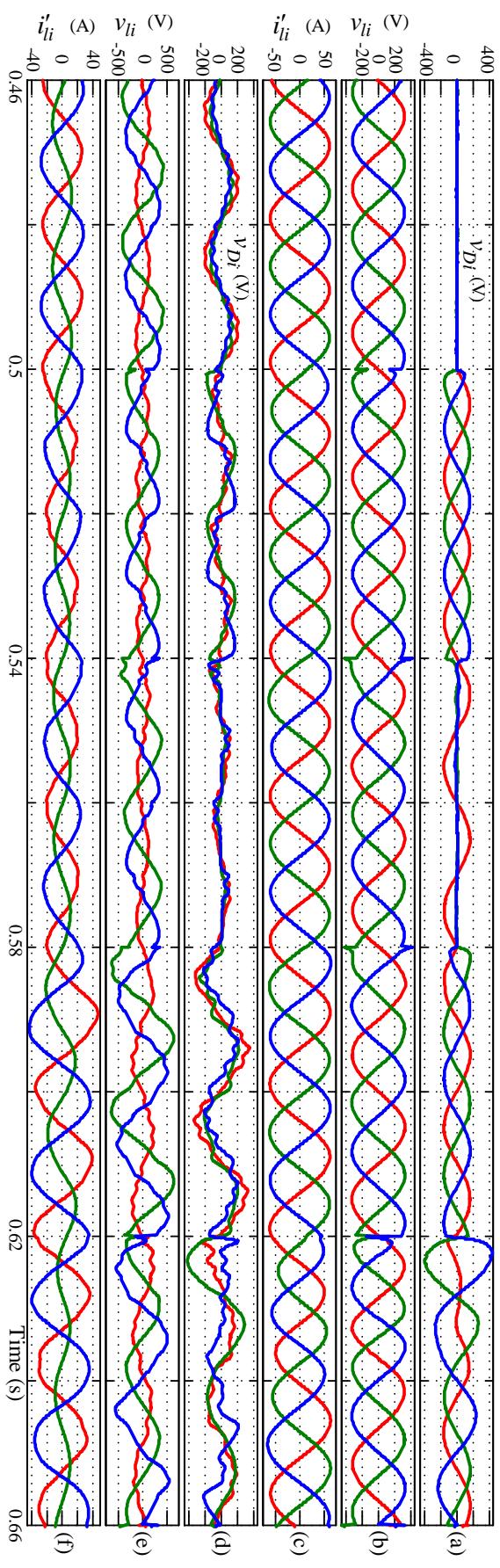


Figure B.7: Simulation results for a star with neutral connected to filter capacitors neutral configuration; The DVR voltages (v_{D_i}), load voltages (v_{li}) and transformer primary currents (i'_{li}): (a), (b) & (c) Balanced load, and (d), (e) & (f) Unbalanced load

Observing Figs. B.6 and B.7, it is evident that the star-configured three-leg DVR effectively mitigates all voltage disturbances for balanced loads. However, for unbalanced loads, voltage disturbances remain unresolved due to the absence of a path for zero sequence currents at the transformer primary side. Notably, the successful regulation of load voltage for unbalanced sag indicates the capability of the three-leg DVR to generate zero-sequence voltage. Consequently, a star-configured transformer and converter that facilitate the flow of zero sequence current emerge as the feasible solution for DVR implementation in the secondary distribution system.

The comprehensive analysis of this study is summarized in Table B.2. The table presents the performance of the DVR in different transformer configurations and system scenarios, indicating whether the DVR successfully maintains load voltages at the desired value ("Yes") or fails to regulate load voltages ("No"). The table offers a clear overview of the DVR's effectiveness under various conditions, enabling easy evaluation.

It has been verified that the three-wire DVR, regardless of the transformer configuration, is unable to regulate load voltages for all possible grid conditions. Consequently, alternative DVR converter topologies need to be explored to achieve load voltage regulation under all grid conditions. The split-capacitor-based three-leg converter and four-leg converter are potential solutions that can provide both zero-sequence voltage injection and current flow, thereby addressing this limitation.

Table B.2: The compensation capability of three-leg DVR with three transformer configurations under various grid conditions

Load →		Balanced load						Unbalanced load					
Grid voltage →		Balanced	Unbalanced	Unbalanced		Balanced	Unbalanced	Unbalanced					
		Normal	sag/swell	sag/swell	sag/swell	Normal	sag/swell	sag/swell	sag/swell	with $v_{g0} \neq 0$	with $v_{g0} = 0$	with $v_{g0} \neq 0$	with $v_{g0} = 0$
1. Delta	Yes	Yes	No	Yes	Yes	Yes	Yes	No	Yes	Yes	No	Yes	
2. Star with isolated neutral	Yes	Yes	Yes	Yes	Yes	No	No	No	No	No	No	No	
3. Star with neutral connected to filter capacitors neutral	Yes	Yes	Yes	Yes	Yes	No	No	No	No	No	No	No	

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