# Terminal Output - Team Friday: Genus CPU Synthesis

```
[vlsiuser21@vlsicadclient07 ~]$ cd
/home/vlsiuser21/Desktop/aditya_Friday/files_rtl3gds/Cadence_design_da
tabase_45nm/Cadence_design_database_45nm/s
simulation/ synthesis/
[vlsiuser21@vlsicadclient07 ~]$ cd
/home/vlsiuser21/Desktop/aditya_Friday/files_rtl3gds/Cadence_design_da
tabase_45nm/Cadence_design_database_45nm/synthesis/
[vlsiuser21@vlsicadclient07 synthesis]$ c

[vlsiuser21@vlsicadclient07 synthesis]$ genus --legacy_ui
genus: WARNING: 32bit executable version of "genus" not found... the
64bit version will  be used instead.
Option with '--' (--legacy_ui) is not valid.
Abnormal exit.
[vlsiuser21@vlsicadclient07 synthesis]$ genus --legacy-ui
genus: WARNING: 32bit executable version of "genus" not found... the
64bit version will  be used instead.
Option with '--' (--legacy-ui) is not valid.
Abnormal exit.
[vlsiuser21@vlsicadclient07 synthesis]$ genus -legacy_ui
genus: WARNING: 32bit executable version of "genus" not found... the
64bit version will  be used instead.
TMPDIR is being set to
/tmp/genus_temp_14100_vlsicadclient07_vlsiuser21_UxlErS
Cadence Genus(TM) Synthesis Solution.
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of Cadence Design Systems, Inc. in the United States and other
countries.

Version: 21.10-p002_1, built Thu Aug 19 21:43:13 PDT 2021
Options: -legacy_ui
Date:    Thu Jan 23 19:34:16 2025
```

```
Host:    vlsicadclient07 (x86_64 w/Linux 3.10.0-957.el7.x86_64)
(6cores*12cpus*1physical cpu*Intel(R) Core(TM) i7-8700 CPU @ 3.20GHz
12288KB) (36699188KB)
PID:     14100
OS:      Red Hat Enterprise Linux Workstation release 7.6 (Maipo)

Checkout succeeded: Genus_Synthesis/AF9962AAA7C3F38A370F
License file: 5280@172.16.201.225
License Server: 5280@172.16.201.225
Checking out license: Genus_Synthesis


**************************************************************************
************************************
**************************************************************************
************************************



Loading tool scripts...
Finished loading tool scripts (7 seconds elapsed).

WARNING: This version of the tool is 1252 days old.
legacy_genus:/> clear









legacy_genus:/> source ../../../genus_scripts.tcl
Sourcing '../../../genus_scripts.tcl' (Thu Jan 23 19:34:37 IST
2025)...
  Setting attribute of root '/': 'init_lib_search_path' = ../lib/
```

```
Warning : This attribute will be obsolete in a next major release.
[TUI-32]
        : attribute: 'hdl_search_path', object type: 'root'
        : Attribute 'hdl_search_path' is going to be obsoleted, use
the new attribute 'init_hdl_search_path'.
  Setting attribute of root '/': 'hdl_search_path' = ../rtl/

Threads Configured:3

  Message Summary for Library slow_vdd1v0_basicCells.lib:
  *******************************************************
  Missing a function attribute in the output pin definition.
[LBR-518]: 1
  *******************************************************

Info    : Created nominal operating condition. [LBR-412]
        : Operating condition '_nominal_' was created for the PVT
values (1.000000, 0.900000, 125.000000) in library
'slow_vdd1v0_basicCells.lib'.
        : The nominal operating condition is represented, either by
the nominal PVT values specified in the library source (via
nom_process,nom_voltage and nom_temperature respectively), or by the
default PVT values (1.0,1.0,1.0).
Warning : Library cell has no output pins defined. [LBR-9]
        : Library cell 'ANTENNA' must have an output pin.
        : Add the missing output pin(s), then reload the library. Else
the library cell will be marked as timing model i.e. unusable.
Timing_model means that the cell does not have any defined function.
If there is no output pin, Genus will mark library cell as unusable
i.e. the attribute 'usable' will be marked to 'false' on the libcell.
Therefore, the cell is not used for mapping and it will not be picked
up from the library for synthesis. If you query the attribute
'unusable_reason' on the libcell; result will be: 'Library cell has no
output pins.'Note: The message LBR-9 is only for the logical pins and
not for the power_ground pins. Genus will depend upon the output
function defined in the pin group (output pin) of the cell, to use it
for mapping. The pg_pin will not have any function defined.
Warning : Library cell has no output pins defined. [LBR-9]
```

```
        : Library cell 'ANTENNA' must have an output pin.
  Setting attribute of root '/': 'library' =
slow_vdd1v0_basicCells.lib
  Library has 324 usable logic and 128 usable sequential lib-cells.
Info    : Elaborating Design. [ELAB-1]
        : Elaborating top-level block 't1c_riscv_cpu' from file
'../rtl/t1c_riscv_cpu.v'.
Warning : In legacy_ui mode, Genus creates a blackbox as description
for a module is not found. Black boxes represent unresolved references
in the design and are usually not expected. Another possible reason
is, some libraries are not read and the tool could not get the content
for some macros or lib_cells. [CDFG-428]
        : A blackbox was created for instance 'rvcpu' in file
'../rtl/t1c_riscv_cpu.v' on line 18.
        : Check the kind of module a black box is. If it is a lib_cell
or a macro, check why the corresponding .lib was not read in. This
could be either due to a missing or faulty file or due to an
incomplete init_lib_search_path attribute value making restricting
access to the missing file. If it is a module of your design, verify
whether the path to this module is a part of the files you read or
else check that the init_hdl_search_path attribute is not missing some
paths.
Warning : In legacy_ui mode, Genus creates a blackbox as description
for a module is not found. Black boxes represent unresolved references
in the design and are usually not expected. Another possible reason
is, some libraries are not read and the tool could not get the content
for some macros or lib_cells. [CDFG-428]
        : A blackbox was created for instance 'instrmem' in file
'../rtl/t1c_riscv_cpu.v' on line 21.
Warning : In legacy_ui mode, Genus creates a blackbox as description
for a module is not found. Black boxes represent unresolved references
in the design and are usually not expected. Another possible reason
is, some libraries are not read and the tool could not get the content
for some macros or lib_cells. [CDFG-428]
        : A blackbox was created for instance 'datamem' in file
'../rtl/t1c_riscv_cpu.v' on line 22.
Info    : Done Elaborating Design. [ELAB-3]
        : Done elaborating 't1c_riscv_cpu'.
```

```
Warning : Black-boxes are represented as unresolved references in the
design. [TUI-273]
        : Cannot resolve reference to 'riscv_cpu'.
        : Run check_design to get all unresolved instance. To resolve
the reference, either load a technology library containing the cell by
appending to the 'library' attribute, or read in the hdl file
containing the module before performing elaboration. As the design is
incomplete, synthesis results may not correspond to the entire design.
Warning : Black-boxes are represented as unresolved references in the
design. [TUI-273]
        : Cannot resolve reference to 'instr_mem'.
Warning : Black-boxes are represented as unresolved references in the
design. [TUI-273]
        : Cannot resolve reference to 'data_mem'.
Checking for analog nets...
Check completed for analog nets.
Checking for source RTL...
Check completed for source RTL.
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks
-----------------------------------------------------------
| Trick             | Accepts | Rejects | Runtime (ms) |
-----------------------------------------------------------
| ume_constant_bmux |       0 |       0 |         1.00 |
-----------------------------------------------------------
Starting clip mux common data inputs [v1.0] (stage: post_elab,
startdef: t1c_riscv_cpu, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0,
runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: post_elab,
startdef: t1c_riscv_cpu, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0,
runtime: 0.000s)
Warning : Could not find requested search value. [SDC-208] [get_ports]
        : The 'get_ports' command on line '5' of the SDC file
'../constraints/constraints_top.sdc'  cannot find any ports named
'rst'
```

```
        : Use get_* commands to find the objects along with a wild
card entry in the name of the object to check if the object is
existing with different naming style.
Error   : Invalid SDC command option combination. [SDC-204]
[set_io_delay]
        : The set_io_delay command does not accept empty ports lists
        : This option is not valid for the indicated SDC command.
Check the SDC command and contact Cadence customer support if you
believe this option combination should be supported.
Error   : Could not interpret SDC command. [SDC-202] [read_sdc]
        : The 'read_sdc' command encountered an error while processing
this command on line '5' of the SDC file
'../constraints/constraints_top.sdc': set_input_delay -max 1.0
[get_ports 'rst'] -clock [get_clocks 'clk'].
        : The 'read_sdc' command encountered a problem while trying to
evaluate an SDC command. This SDC command will be added to the Tcl
variable $::dc::sdc_failed_commands.
Warning : Could not find requested search value. [SDC-208] [get_ports]
        : The 'get_ports' command on line '6' of the SDC file
'../constraints/constraints_top.sdc'  cannot find any ports named
'count'
Error   : Could not interpret SDC command. [SDC-202] [read_sdc]
        : The 'read_sdc' command encountered an error while processing
this command on line '6' of the SDC file
'../constraints/constraints_top.sdc': set_output_delay -max 1.0
[get_ports 'count'] -clock [get_clocks 'clk'].
Statistics for commands executed by read_sdc:
 "create_clock"             - successful      1 , failed      0
(runtime  0.00)
 "get_clocks"               - successful      4 , failed      0
(runtime  0.00)
 "get_ports"                - successful      2 , failed      2
(runtime  0.00)
 "set_clock_transition"     - successful      2 , failed      0
(runtime  0.00)
 "set_clock_uncertainty"    - successful      1 , failed      0
(runtime  0.00)
```

```
 "set_input_delay"          - successful      0 , failed      1
(runtime  0.00)
 "set_output_delay"         - successful      0 , failed      1
(runtime  0.00)
Warning : Total failed commands during read_sdc are 4
Warning : One or more commands failed when these constraints were
applied. [SDC-209]
        : The 'read_sdc' command encountered a problem while
processing commands.
        : You can examine the failed commands or save them to a file
by querying the Tcl variable $::dc::sdc_failed_commands.
read_sdc completed in 00:00:00 (hh:mm:ss)
  Setting attribute of root '/': 'syn_generic_effort' = high
##Generic Timing Info for library domain: _default_ typical gate
delay: 127.6 ps std_slew: 17.9 ps std_load: 1.0 fF
Starting mux data reorder optimization [v1.0] (stage:
pre_to_gen_setup, startdef: t1c_riscv_cpu, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0,
runtime: 0.000s)
Info    : Synthesizing. [SYNTH-1]
        : Synthesizing 't1c_riscv_cpu' to generic gates using 'high'
effort.
PBS_Generic-Start - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_Generic-Start' being created for table 'pbs_debug'

  Total Time (Wall) |  Stage Time (Wall)  |   % (Wall)   |    Date -
Time     |  Memory   | Stage
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:18) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:38
(Jan23) |  251.6 MB | PBS_Generic-Start
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
Number of threads: 8 * 1   (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
TNS Restructuring config: no_value at stage: generic applied.
```

```
Info    : Partition Based Synthesis execution skipped. [PHYS-752]
        : Design size is less than the partition size '100000' for
distributed generic optimization to kick in.
Starting mux data reorder optimization [v1.0] (stage:
pre_to_gen_setup, startdef: t1c_riscv_cpu, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0,
runtime: 0.001s)
Starting mux data reorder optimization [v1.0] (stage:
post_to_gen_setup, startdef: t1c_riscv_cpu, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0,
runtime: 0.000s)
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks
-------------------------------------------
| Trick | Accepts | Rejects | Runtime (ms) |
-------------------------------------------
-------------------------------------------
Starting datapath recasting [v1.0] (stage: pre_rtlopt, startdef:
t1c_riscv_cpu, recur: true)
Completed datapath recasting (accepts: 0, rejects: 0, runtime: 0.000s)
Starting infer macro optimization [v1.0] (stage: pre_rtlopt, startdef:
t1c_riscv_cpu, recur: true)
Completed infer macro optimization (accepts: 0, rejects: 0, runtime:
0.001s)
Starting decode mux sandwich optimization [v2.0] (stage: pre_rtlopt,
startdef: t1c_riscv_cpu, recur: true)
Completed decode mux sandwich optimization (accepts: 0, rejects: 0,
runtime: 0.000s)
Starting decode mux optimization [v1.0] (stage: pre_rtlopt, startdef:
t1c_riscv_cpu, recur: true)
Completed decode mux optimization (accepts: 0, rejects: 0, runtime:
0.000s)
Starting chop wide muxes [v1.0] (stage: pre_rtlopt, startdef:
t1c_riscv_cpu, recur: true)
Completed chop wide muxes (accepts: 0, rejects: 0, runtime: 0.000s)
Starting common data mux cascade opt [v1.0] (stage: pre_rtlopt,
startdef: t1c_riscv_cpu, recur: true)
```

```
Completed common data mux cascade opt (accepts: 0, rejects: 0,
runtime: 0.000s)
Starting mux input consolidation [v1.0] (stage: pre_rtlopt, startdef:
t1c_riscv_cpu, recur: true)
Completed mux input consolidation (accepts: 0, rejects: 0, runtime:
0.000s)
Starting priority mux optimization [v1.0] (stage: pre_rtlopt,
startdef: t1c_riscv_cpu, recur: true)
Completed priority mux optimization (accepts: 0, rejects: 0, runtime:
0.012s)
Starting constant-data mux optimization [v1.0] (stage: pre_rtlopt,
startdef: t1c_riscv_cpu, recur: true)
Completed constant-data mux optimization (accepts: 0, rejects: 0,
runtime: 0.000s)
Starting chain-to-tree inequality transform [v2.0] (stage: pre_rtlopt,
startdef: t1c_riscv_cpu, recur: true)
Completed chain-to-tree inequality transform (accepts: 0, rejects: 0,
runtime: 0.000s)
Starting reconvergence optimization [v1.0] (stage: pre_rtlopt,
startdef: t1c_riscv_cpu, recur: true)
Completed reconvergence optimization (accepts: 0, rejects: 0, runtime:
0.000s)
Starting logic restructure optimization [v1.0] (stage: pre_rtlopt,
startdef: t1c_riscv_cpu, recur: true)
Completed logic restructure optimization (accepts: 0, rejects: 0,
runtime: 0.000s)
Starting common select mux optimization [v1.0] (stage: pre_rtlopt,
startdef: t1c_riscv_cpu, recur: true)
Completed common select mux optimization (accepts: 0, rejects: 0,
runtime: 0.000s)
Starting identity transform [v3.0] (stage: pre_rtlopt, startdef:
t1c_riscv_cpu, recur: true)
Completed identity transform (accepts: 0, rejects: 0, runtime: 0.000s)
Starting reduce operator chain [v1.0] (stage: pre_rtlopt, startdef:
t1c_riscv_cpu, recur: true)
Completed reduce operator chain (accepts: 0, rejects: 0, runtime:
0.000s)
```

```
Starting common data mux cascade opt [v1.0] (stage: pre_rtlopt,
startdef: t1c_riscv_cpu, recur: true)
Completed common data mux cascade opt (accepts: 0, rejects: 0,
runtime: 0.000s)
Starting mux input consolidation [v1.0] (stage: pre_rtlopt, startdef:
t1c_riscv_cpu, recur: true)
Completed mux input consolidation (accepts: 0, rejects: 0, runtime:
0.000s)
Starting optimize datapath elements [v1.0] (stage: pre_rtlopt,
startdef: t1c_riscv_cpu, recur: true)
Completed optimize datapath elements (accepts: 0, rejects: 0, runtime:
0.000s)
Starting clip mux common data inputs [v1.0] (stage: pre_rtlopt,
startdef: t1c_riscv_cpu, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0,
runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: pre_rtlopt,
startdef: t1c_riscv_cpu, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0,
runtime: 0.000s)
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks
-------------------------------------------------
| Trick       | Accepts | Rejects | Runtime (ms) |
-------------------------------------------------
| ume_runtime |       0 |       0 |         0.00 |
-------------------------------------------------
Number of big hc bmuxes before = 0
Info    : Pre-processed datapath logic. [DPOPT-6]
        : No pre-processing optimizations applied to datapath logic in
't1c_riscv_cpu'.
Info    : Skipping datapath optimization. [DPOPT-5]
        : There is no datapath logic in 't1c_riscv_cpu'.
Number of big hc bmuxes after = 0
Starting logic reduction [v1.0] (stage: post_rtlopt, startdef:
t1c_riscv_cpu, recur: true)
Completed logic reduction (accepts: 0, rejects: 0, runtime: 0.000s)
```

```
Starting mux data reorder optimization [v1.0] (stage: post_rtlopt,
startdef: t1c_riscv_cpu, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0,
runtime: 0.000s)
Starting mux speculation [v1.0] (stage: post_muxopt, startdef:
t1c_riscv_cpu, recur: true)
Starting speculation optimization
Completed speculation optimization (accepts:0)
Completed mux speculation (accepts: 0, rejects: 0, runtime: 0.008s)
==================================
Stage : to_generic
==================================
  =================
   Message Summary
  =================
------------------------------------------------------------------------
------------------------------------------------------------------------
-------------------------------------------------
|    Id    |  Sev   |Count |
Message Text
|
------------------------------------------------------------------------
------------------------------------------------------------------------
-------------------------------------------------
| CDFG-372 |Info    |    1 |Bitwidth mismatch in assignment.
|
|          |        |      |Review and make sure the mismatch is
unintentional. Genus can possibly issue bitwidth mismatch warning for
explicit assignments present in RTL as-well-as for    |
|          |        |      | implicit assignments inferred by the
tool. For example, in case of enum declaration without value, the tool
will implicitly assign value to the enum variables. |
|          |        |      | It also issues the warning for any
bitwidth mismatch that appears in this implicit assignment.
|
| CDFG-428 |Warning |    3 |In legacy_ui mode, Genus creates a
blackbox as description for a module is not found. Black boxes
represent unresolved references in the design and are usually  |
```

|  |  |  | not expected. Another possible reason is, some libraries are not read and the tool could not get the content for some macros or lib_cells.  |
|  |  |  |Check the kind of module a black box is. If it is a lib_cell or a macro, check why the corresponding .lib was not read in. This could be either due to a missing |
|  |  |  | or faulty file or due to an incomplete init_lib_search_path attribute value making restricting access to the missing file. If it is a module of your design,  |
|  |  |  | verify whether the path to this module is a part of the files you read or else check that the init_hdl_search_path attribute is not missing some paths.  |
| DPOPT-5 |Info |  1 |Skipping datapath optimization.
|
| DPOPT-6 |Info |  1 |Pre-processed datapath logic.
|
| ELAB-1 |Info |  1 |Elaborating Design.
|
| ELAB-3 |Info |  1 |Done Elaborating Design.
|
| LBR-9 |Warning |  2 |Library cell has no output pins defined.
|
|  |  |  |Add the missing output pin(s)
|
|  |  |  | , then reload the library. Else the library cell will be marked as timing model i.e. unusable. Timing_model means that the cell does not have any defined  |
|  |  |  | function. If there is no output pin, Genus will mark library cell as unusable i.e. the attribute 'usable' will be marked to 'false' on the libcell. Therefore,  |
|  |  |  | the cell is not used for mapping and it will not be picked up from the library for synthesis. If you query the attribute 'unusable_reason' on the libcell;  |
|  |  |  | result will be: 'Library cell has no output pins.'Note: The message LBR-9 is only for the logical pins and not for the power_ground pins. Genus will depend  |

|          |        |      | upon the output function defined in the pin group (output pin) of the cell, to use it for mapping. The pg_pin will not have any function defined.               |
| LBR-41   |Info    |    1 |An output library pin lacks a function attribute.
|
|          |        |      |If the remainder of this library cell's semantic checks are successful, it will be considered as a timing-model                                                 |
|          |        |      | (because one of its outputs does not have a valid function.
|
| LBR-155  |Info    |  264 |Mismatch in unateness between 'timing_sense' attribute and the function.
|
|          |        |      |The 'timing_sense' attribute will be respected.
|
| LBR-161  |Info    |    1 |Setting the maximum print count of this message to 10 if information_level is less than 9.
|
| LBR-162  |Info    |  124 |Both 'pos_unate' and 'neg_unate' timing_sense arcs have been processed.
|
|          |        |      |Setting the 'timing_sense' to non_unate.
|
| LBR-412  |Info    |    1 |Created nominal operating condition.
|
|          |        |      |The nominal operating condition is represented, either by the nominal PVT values specified in the library source                                                |
|          |        |      | (via nom_process,nom_voltage and nom_temperature respectively), or by the default PVT values (1.0,1.0,1.0).                                                    |
| LBR-518  |Info    |    1 |Missing a function attribute in the output pin definition.
|

| PHYS-752 |Info    |    1 |Partition Based Synthesis execution skipped.
|
| SDC-202  |Error   |    2 |Could not interpret SDC command.
|
|          |        |      |The 'read_sdc' command encountered a problem while trying to evaluate an SDC command. This SDC command will be added to the Tcl variable                          |
|          |        |      | $::dc::sdc_failed_commands.
|
| SDC-204  |Error   |    1 |Invalid SDC command option combination.
|
|          |        |      |This option is not valid for the indicated SDC command. Check the SDC command and contact Cadence customer support if you believe this option combination should |
|          |        |      | be supported.
|
| SDC-208  |Warning |    2 |Could not find requested search value.
|
|          |        |      |Use get_* commands to find the objects along with a wild card entry in the name of the object to check if the object is existing with different naming style.    |
| SDC-209  |Warning |    1 |One or more commands failed when these constraints were applied.
|
|          |        |      |You can examine the failed commands or save them to a file by querying the Tcl variable $::dc::sdc_failed_commands.
|
| SYNTH-1  |Info    |    1 |Synthesizing.
|
| TUI-32   |Warning |    1 |This attribute will be obsolete in a next major release.
|
| TUI-273  |Warning |    3 |Black-boxes are represented as unresolved references in the design.
|

```
|          |        |      |Run check_design to get all unresolved
instance. To resolve the reference, either load a technology library
containing the cell by appending to the 'library'    |
|          |        |      | attribute, or read in the hdl file
containing the module before performing elaboration. As the design is
incomplete, synthesis results may not correspond to    |
|          |        |      | the entire design.
|
------------------------------------------------------------------------
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-------------------------------------------------
Mapper: Libraries have:
domain _default_: 324 combo usable cells and 128 sequential usable
cells
Multi-threaded constant propagation [1|0] ...
Multi-threaded Virtual Mapping    (8 threads, 8 of 12 CPUs usable)

Global mapping target info
==========================
Cost Group 'default' target slack: Unconstrained

PBS_Generic_Opt-Post - Elapsed_Time 1, CPU_Time 0.9058790000000005
stamp 'PBS_Generic_Opt-Post' being created for table 'pbs_debug'

  Total Time (Wall) |  Stage Time (Wall)  |   % (Wall)   |    Date -
Time     |  Memory   | Stage
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:18) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:38
(Jan23) |  251.6 MB | PBS_Generic-Start
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:01) | 100.0(100.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic_Opt-Post
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
Number of threads: 8 * 1   (id: pbs_debug, time_info v1.57)
```

```
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
PBS_Generic-Postgen HBO Optimizations - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_Generic-Postgen HBO Optimizations' being created for table
'pbs_debug'

  Total Time (Wall) |  Stage Time (Wall)  |   % (Wall)   |    Date -
Time     |  Memory   | Stage
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:18) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:38
(Jan23) |  251.6 MB | PBS_Generic-Start
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:01) | 100.0(100.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic_Opt-Post
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 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic-Postgen HBO Optimizations
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--------+-----------+----------------------
Number of threads: 8 * 1   (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
##>=================== Cadence Confidential (Generic-Logical)
===================
##>=================== Cadence Confidential (Generic-Logical)
===================
##>Main Thread Summary:
##>-----------------------------------------------------------------------
---------------------
##>STEP                            Elapsed       WNS       TNS
Insts      Area    Memory
##>-----------------------------------------------------------------------
---------------------
```

```
##>G:Initial                              0         -         -
67       352       251
##>G:Setup                                0         -         -
-         -         -
##>G:Launch ST                            0         -         -
-         -         -
##>G:Design Partition                     0         -         -
-         -         -
##>G:Create Partition Netlists            0         -         -
-         -         -
##>G:Init Power                           0         -         -
-         -         -
##>G:Budgeting                            0         -         -
-         -         -
##>G:Derenv-DB                            0         -         -
-         -         -
##>G:Debug Outputs                        0         -         -
-         -         -
##>G:ST loading                           0         -         -
-         -         -
##>G:Distributed                          0         -         -
-         -         -
##>G:Timer                                0         -         -
-         -         -
##>G:Assembly                             0         -         -
-         -         -
##>G:DFT                                  0         -         -
-         -         -
##>G:Const Prop                           0         -         -
194       517       251
##>G:Misc                                 1
##>-------------------------------------------------------------------
---------------------
##>Total Elapsed                          1
##>===================================================================
=====================
Info    : Done synthesizing. [SYNTH-2]
        : Done synthesizing 't1c_riscv_cpu' to generic gates.
```

```
##Generic Timing Info for library domain: _default_ typical gate
delay: 127.6 ps std_slew: 17.9 ps std_load: 1.0 fF
Info    : Mapping. [SYNTH-4]
        : Mapping 't1c_riscv_cpu' using 'high' effort.
Mapper: Libraries have:
domain _default_: 324 combo usable cells and 128 sequential usable
cells
Configuring mapper costing (none)
TNS Restructuring config: no_value at stage: map applied.
PBS_TechMap-Start - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_TechMap-Start' being created for table 'pbs_debug'

  Total Time (Wall) |  Stage Time (Wall)  |   % (Wall)   |    Date -
Time     |  Memory   | Stage
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:18) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:38
(Jan23) |  251.6 MB | PBS_Generic-Start
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:01) | 100.0(100.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic_Opt-Post
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic-Postgen HBO Optimizations
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_TechMap-Start
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
Number of threads: 8 * 1   (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
PBS_TechMap-Premap HBO Optimizations - Elapsed_Time 0, CPU_Time 0.0
```

```
stamp 'PBS_TechMap-Premap HBO Optimizations' being created for table
'pbs_debug'

  Total Time (Wall) |  Stage Time (Wall)  |   % (Wall)   |    Date -
Time     |  Memory   | Stage
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:18) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:38
(Jan23) |  251.6 MB | PBS_Generic-Start
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:01) | 100.0(100.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic_Opt-Post
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic-Postgen HBO Optimizations
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_TechMap-Start
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--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_TechMap-Premap HBO Optimizations
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
Number of threads: 8 * 1   (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
Info    : Partition Based Synthesis execution skipped. [PHYS-752]
        : Design size is less than the partition size '100000' for
distributed mapping optimization to kick in.
Mapper: Libraries have:
domain _default_: 324 combo usable cells and 128 sequential usable
cells
Multi-threaded Virtual Mapping    (8 threads, 8 of 12 CPUs usable)
```

```
Global mapping target info
==========================
Cost Group 'default' target slack: Unconstrained

Multi-threaded Technology Mapping (8 threads, 8 of 12 CPUs usable)

Global mapping status
=====================
                                   Group
                                  Tot Wrst
                           Total  Weighted
Operation                   Area   Slacks
 global_map                  158        0

    Cost Group            Target    Slack    Diff.  Constr.
-------------------------------------------------------------
       default          unconst. unconst.              N.A.


Global incremental target info
==============================
Cost Group 'default' target slack: Unconstrained

==================================
Stage : global_incr_map
==================================
  =================
   Message Summary
  =================
-------------------------------------------------------------------------
---
|    Id    |Sev  |Count |                 Message Text
|
-------------------------------------------------------------------------
---
| PA-7     |Info |    2 |Resetting power analysis results.
|
```

```
|          |     |      |All computed switching activities are
removed. |
| PHYS-752 |Info |    1 |Partition Based Synthesis execution skipped.
|
| SYNTH-2  |Info |    1 |Done synthesizing.
|
| SYNTH-4  |Info |    1 |Mapping.
|
------------------------------------------------------------------------
---

Global incremental optimization status
======================================
                                  Group
                                 Tot Wrst
                           Total  Weighted
Operation                   Area   Slacks
 global_incr                 158        0

    Cost Group            Target    Slack    Diff.  Constr.
-------------------------------------------------------------
       default          unconst. unconst.              N.A.

INFO: skipping constant propagation
PBS_Techmap-Global Mapping - Elapsed_Time 1, CPU_Time
0.7948399999999989
stamp 'PBS_Techmap-Global Mapping' being created for table 'pbs_debug'

  Total Time (Wall) |  Stage Time (Wall)  |   % (Wall)   |    Date -
Time     |  Memory   | Stage
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:18) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:38
(Jan23) |  251.6 MB | PBS_Generic-Start
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:01) |  53.3( 50.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic_Opt-Post
```

```
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--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic-Postgen HBO Optimizations
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_TechMap-Start
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--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_TechMap-Premap HBO Optimizations
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:01) |  46.7( 50.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_Techmap-Global Mapping
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
Number of threads: 8 * 1   (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
Warning : Command 'commit_power_intent' cannot proceed as there is no
power intent loaded. [CPI-506]
        : Command 'commit_power_intent' requires a valid power_intent
to be loaded.
Info    : Wrote formal verification information. [CFM-5]
        : Wrote 'fv/t1c_riscv_cpu/fv_map.fv.json' for netlist
'fv/t1c_riscv_cpu/fv_map.v.gz'.
Info    : Wrote dofile. [CFM-1]
        : Dofile is 'fv/t1c_riscv_cpu/rtl_to_fv_map.do'.
        : Alias mapping flow is enabled.
PBS_TechMap-Datapath Postmap Operations - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_TechMap-Datapath Postmap Operations' being created for
table 'pbs_debug'

  Total Time (Wall) |  Stage Time (Wall)  |   % (Wall)   |    Date -
Time     |  Memory   | Stage
```

```
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:08(00:00:18) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:38
(Jan23) |  251.6 MB | PBS_Generic-Start
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:01) |  53.3( 50.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic_Opt-Post
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic-Postgen HBO Optimizations
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 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_TechMap-Start
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--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_TechMap-Premap HBO Optimizations
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:01) |  46.7( 50.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_Techmap-Global Mapping
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_TechMap-Datapath Postmap Operations
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
Number of threads: 8 * 1   (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
PBS_TechMap-Postmap HBO Optimizations - Elapsed_Time 0, CPU_Time
-0.002285999999999788
stamp 'PBS_TechMap-Postmap HBO Optimizations' being created for table
'pbs_debug'
```

```
  Total Time (Wall) |  Stage Time (Wall)  |   % (Wall)   |    Date -
Time     |  Memory   | Stage
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:18) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:38
(Jan23) |  251.6 MB | PBS_Generic-Start
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:01) |  53.3( 50.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic_Opt-Post
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic-Postgen HBO Optimizations
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_TechMap-Start
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_TechMap-Premap HBO Optimizations
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:01) |  46.8( 50.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_Techmap-Global Mapping
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_TechMap-Datapath Postmap Operations
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:00) |  -0.1(  0.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_TechMap-Postmap HBO Optimizations
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
Number of threads: 8 * 1   (id: pbs_debug, time_info v1.57)
```

```
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
 Doing ConstProp on /designs/t1c_riscv_cpu ...

IOPT-REDREM: Performing redundancy removal: Detected 0 redundant
wires. CPU time 0.000 seconds.

PBS_TechMap-Postmap Clock Gating - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_TechMap-Postmap Clock Gating' being created for table
'pbs_debug'

  Total Time (Wall) |  Stage Time (Wall)  |   % (Wall)   |    Date -
Time     |  Memory   | Stage
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:18) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:38
(Jan23) |  251.6 MB | PBS_Generic-Start
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:01) |  53.3( 50.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic_Opt-Post
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic-Postgen HBO Optimizations
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--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_TechMap-Start
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_TechMap-Premap HBO Optimizations
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:01) |  46.8( 50.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_Techmap-Global Mapping
```

```
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_TechMap-Datapath Postmap Operations
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:00) |  -0.1(  0.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_TechMap-Postmap HBO Optimizations
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_TechMap-Postmap Clock Gating
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
Number of threads: 8 * 1   (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
-------------------------------------------------------------------------
---------
 hi_fo_buf                   158        0         0         0        0

           Trick     Calls     Accepts   Attempts    Time(secs)
-----------------------------------------------------------
       hi_fo_buf         0  (        0 /        0 )  0.00


Incremental optimization status
================================
                                    Group
                                   Tot Wrst     Total - - DRC Totals -
-
                           Total  Weighted      Neg      Max       Max
Operation                   Area   Slacks      Slack    Trans      Cap
 init_delay                  158        0         0         0        0

           Trick     Calls     Accepts   Attempts    Time(secs)
-----------------------------------------------------------
```

```
       crit_upsz         0  (        0 /        0 )  0.00
    plc_bal_star         0  (        0 /        0 )  0.00
     drc_buftimb         0  (        0 /        0 )  0.00
          plc_st         0  (        0 /        0 )  0.00
    plc_st_fence         0  (        0 /        0 )  0.00
        plc_star         0  (        0 /        0 )  0.00
      plc_laf_st         0  (        0 /        0 )  0.00
 plc_laf_st_fence         0  (        0 /        0 )  0.00
     drc_buftims         0  (        0 /        0 )  0.00
            fopt         0  (        0 /        0 )  0.00
   plc_laf_lo_st         0  (        0 /        0 )  0.00
       plc_lo_st         0  (        0 /        0 )  0.00
        mb_split         0  (        0 /        0 )  0.00


Local TNS optimization status
=============================
                                  Group
                                 Tot Wrst     Total - - DRC Totals -
-
                          Total  Weighted      Neg      Max       Max
Operation                  Area   Slacks      Slack    Trans      Cap
 init_tns                   158        0         0        0        0

           Trick     Calls     Accepts   Attempts    Time(secs)
-------------------------------------------------------------
    plc_bal_star         0  (        0 /        0 )  0.00
     drc_buftimb         0  (        0 /        0 )  0.00
     drc_buftims         0  (        0 /        0 )  0.00
       crit_upsz         0  (        0 /        0 )  0.00
   plc_laf_lo_st         0  (        0 /        0 )  0.00
       plc_lo_st         0  (        0 /        0 )  0.00
            fopt         0  (        0 /        0 )  0.00
       crit_dnsz         0  (        0 /        0 )  0.00
             dup         0  (        0 /        0 )  0.00
        setup_dn         0  (        0 /        0 )  0.00
        mb_split         0  (        0 /        0 )  0.00
```

```
PBS_TechMap-Postmap Cleanup - Elapsed_Time 0, CPU_Time
-0.0022469999999987778
stamp 'PBS_TechMap-Postmap Cleanup' being created for table
'pbs_debug'

  Total Time (Wall) |  Stage Time (Wall)  |   % (Wall)   |    Date -
Time     |  Memory   | Stage
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:18) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:38
(Jan23) |  251.6 MB | PBS_Generic-Start
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:01) |  53.4( 50.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic_Opt-Post
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic-Postgen HBO Optimizations
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_TechMap-Start
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_TechMap-Premap HBO Optimizations
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:01) |  46.9( 50.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_Techmap-Global Mapping
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_TechMap-Datapath Postmap Operations
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
```

```
 00:00:09(00:00:20) |  00:00:00(00:00:00) |  -0.1(  0.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_TechMap-Postmap HBO Optimizations
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_TechMap-Postmap Clock Gating
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:00) |  -0.1(  0.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_TechMap-Postmap Cleanup
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
Number of threads: 8 * 1   (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
PBS_Techmap-Post_MBCI - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_Techmap-Post_MBCI' being created for table 'pbs_debug'

  Total Time (Wall) |  Stage Time (Wall)  |   % (Wall)   |    Date -
Time     |  Memory   | Stage
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:18) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:38
(Jan23) |  251.6 MB | PBS_Generic-Start
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:01) |  53.4( 50.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic_Opt-Post
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_Generic-Postgen HBO Optimizations
--------------------+---------------------+--------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_TechMap-Start
```

```
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:08(00:00:19) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:39
(Jan23) |  251.6 MB | PBS_TechMap-Premap HBO Optimizations
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:01) |  46.9( 50.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_Techmap-Global Mapping
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_TechMap-Datapath Postmap Operations
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:00) |  -0.1(  0.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_TechMap-Postmap HBO Optimizations
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_TechMap-Postmap Clock Gating
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:00) |  -0.1(  0.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_TechMap-Postmap Cleanup
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
 00:00:09(00:00:20) |  00:00:00(00:00:00) |   0.0(  0.0) |   19:34:40
(Jan23) |  251.6 MB | PBS_Techmap-Post_MBCI
--------------------+---------------------+-------------+------------
--------+-----------+----------------------
Number of threads: 8 * 1   (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
##>=================== Cadence Confidential (Mapping-Logical)
===================
##>Main Thread Summary:
```

```
##>-----------------------------------------------------------------
---------------------
##>STEP                            Elapsed       WNS       TNS
Insts      Area    Memory
##>-----------------------------------------------------------------
---------------------
##>M:Initial                             0         -         -
194       517       251
##>M:Pre Cleanup                        0         -         -
194       517       251
##>M:Setup                               0         -         -
-         -         -
##>M:Launch ST                           0         -         -
-         -         -
##>M:Design Partition                    0         -         -
-         -         -
##>M:Create Partition Netlists           0         -         -
-         -         -
##>M:Init Power                          0         -         -
-         -         -
##>M:Budgeting                           0         -         -
-         -         -
##>M:Derenv-DB                           0         -         -
-         -         -
##>M:Debug Outputs                       0         -         -
-         -         -
##>M:ST loading                          0         -         -
-         -         -
##>M:Distributed                         0         -         -
-         -         -
##>M:Timer                               0         -         -
-         -         -
##>M:Assembly                            0         -         -
-         -         -
##>M:DFT                                 0         -         -
-         -         -
##>M:DP Operations                       0         -         -
68       157       251
```

```
##>M:Const Prop                          0         -         0
68       157       251
##>M:Cleanup                            0         -         0
68       157       251
##>M:MBCI                               0         -         -
68       157       251
##>M:Const Gate Removal                 0         -         -
-         -         -
##>M:Misc                               1
##>-------------------------------------------------------------------
--------------------
##>Total Elapsed                        1
##>=================================================================
====================
Info    : Done mapping. [SYNTH-5]
        : Done mapping 't1c_riscv_cpu'.
Info    : Joules engine is used. [RPT-16]
        : Joules engine is being used for the command report_power.
Info   : ACTP-0001 [ACTPInfo] Activity propagation started for stim#0
netlist
       : t1c_riscv_cpu
Info   : ACTP-0009 [ACTPInfo] Activity Propagation Progress Report :
100%
Info   : ACTP-0001 Activity propagation ended for stim#0
Info   : PWRA-0001 [PwrInfo] compute_power effective options
       : -mode : vectorless
       : -skip_propagation : 1
       : -frequency_scaling_factor : 1.0
       : -use_clock_freq : stim
       : -stim :/stim#0
       : -fromGenus : 1
Info   : ACTP-0001 Timing initialization started
Info   : ACTP-0001 Timing initialization ended
Info   : PWRA-0002 [PwrInfo] Skipping activity propagation due to
-skip_ap
       : option....
Warning: PWRA-0302 [PwrWarn] Frequency scaling is not applicable for
vectorless
```

```
       : flow. Ignoring frequency scaling.
Warning: PWRA-0304 [PwrWarn] -stim option is not applicable with
vectorless mode
       : of power analysis, ignored this option.
Info   : PWRA-0002 Started 'vectorless' power computation.
Info   : PWRA-0002 Finished power computation.
Info   : PWRA-0007 [PwrInfo] Completed successfully.
       : Info=6, Warn=2, Error=0, Fatal=0
Error: Directory './reports' not writable!
Instance: /t1c_riscv_cpu
Power Unit: W
PDB Frames: /stim#0/frame#0

-------------------------------------------------------------------------
---
    Category         Leakage     Internal    Switching        Total
Row%

-------------------------------------------------------------------------
---
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00
0.00%
    register     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00
0.00%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00
0.00%
       logic     2.81518e-09  6.87454e-07  4.85190e-08  7.38788e-07
100.00%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00
0.00%
       clock     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00
0.00%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00
0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00
0.00%
```

```
------------------------------------------------------------------------
---
    Subtotal     2.81518e-09  6.87454e-07  4.85190e-08  7.38788e-07
100.00%
  Percentage           0.38%       93.05%        6.57%      100.00%
100.00%

------------------------------------------------------------------------
---
================================================================
  Generated by:           Genus(TM) Synthesis Solution 21.10-p002_1
  Generated on:           Jan 23 2025  07:34:40 pm
  Module:                 t1c_riscv_cpu
  Technology library:     slow_vdd1v0 1.0
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
================================================================


  Gate    Instances   Area       Library
-----------------------------------------
INVX1             1    0.684    slow_vdd1v0
INVXL             1    0.684    slow_vdd1v0
MX2XL            64  153.216    slow_vdd1v0
NAND2BXL          1    1.368    slow_vdd1v0
OR2X2             1    1.710    slow_vdd1v0
-----------------------------------------
total            68  157.662


     Type      Instances   Area  Area %
----------------------------------------
inverter               2   1.368    0.9
unresolved             3   0.000    0.0
logic                 66 156.294   99.1
```

```
physical_cells         0   0.000    0.0
----------------------------------------
total                 71 157.662  100.0

  Setting attribute of root '/': 'syn_opt_effort' = high
Info    : Incrementally optimizing. [SYNTH-7]
        : Incrementally optimizing 't1c_riscv_cpu' using 'high'
effort.

Incremental optimization status
================================
                                    Group
                                   Tot Wrst     Total - - DRC Totals -
-
                           Total  Weighted      Neg      Max       Max
Operation                   Area   Slacks      Slack    Trans      Cap
 init_iopt                   158        0         0        0        0
IOPT-REDREM: Performing redundancy removal: Detected 0 redundant
wires. CPU time 0.000 seconds.

-------------------------------------------------------------------------
---------
 const_prop                  158        0         0        0        0
-------------------------------------------------------------------------
---------
 hi_fo_buf                   158        0         0        0        0

           Trick     Calls     Accepts   Attempts    Time(secs)
-----------------------------------------------------------
       hi_fo_buf         0  (        0 /        0 )  0.00


Incremental optimization status
================================
                                    Group
                                   Tot Wrst     Total - - DRC Totals -
-
                           Total  Weighted      Neg      Max       Max
```

```
Operation                  Area   Slacks      Slack    Trans      Cap
 init_delay                 158        0          0        0        0

           Trick     Calls     Accepts   Attempts    Time(secs)
-------------------------------------------------------------
        crit_msz         0  (        0 /        0 )  0.00
       crit_upsz         0  (        0 /        0 )  0.00
       crit_slew         0  (        0 /        0 )  0.00
        setup_dn         0  (        0 /        0 )  0.00
    plc_bal_star         0  (        0 /        0 )  0.00
     drc_buftimb         0  (        0 /        0 )  0.00
          plc_st         0  (        0 /        0 )  0.00
    plc_st_fence         0  (        0 /        0 )  0.00
        plc_star         0  (        0 /        0 )  0.00
      plc_laf_st         0  (        0 /        0 )  0.00
 plc_laf_st_fence         0  (        0 /        0 )  0.00
     drc_buftims         0  (        0 /        0 )  0.00
   plc_laf_lo_st         0  (        0 /        0 )  0.00
       plc_lo_st         0  (        0 /        0 )  0.00
            fopt         0  (        0 /        0 )  0.00
       crit_swap         0  (        0 /        0 )  0.00
       mux2_swap         0  (        0 /        0 )  0.00
       crit_dnsz         0  (        0 /        0 )  0.00
       load_swap         0  (        0 /        0 )  0.00
            fopt         0  (        0 /        0 )  0.00
        setup_dn         0  (        0 /        0 )  0.00
       load_isol         0  (        0 /        0 )  0.00
       load_isol         0  (        0 /        0 )  0.00
        move_for         0  (        0 /        0 )  0.00
        move_for         0  (        0 /        0 )  0.00
          rem_bi         0  (        0 /        0 )  0.00
         offload         0  (        0 /        0 )  0.00
          rem_bi         0  (        0 /        0 )  0.00
         offload         0  (        0 /        0 )  0.00
           phase         0  (        0 /        0 )  0.00
        in_phase         0  (        0 /        0 )  0.00
       merge_bit         0  (        0 /        0 )  0.00
     merge_idrvr         0  (        0 /        0 )  0.00
```

| | | | | | |
|---|---|---|---|---|---|
| merge_iload | 0 | ( | 0 / | 0 ) | 0.00 |
| merge_idload | 0 | ( | 0 / | 0 ) | 0.00 |
| merge_drvr | 0 | ( | 0 / | 0 ) | 0.00 |
| merge_load | 0 | ( | 0 / | 0 ) | 0.00 |
| decomp | 0 | ( | 0 / | 0 ) | 0.00 |
| p_decomp | 0 | ( | 0 / | 0 ) | 0.00 |
| levelize | 0 | ( | 0 / | 0 ) | 0.00 |
| mb_split | 0 | ( | 0 / | 0 ) | 0.00 |
| dup | 0 | ( | 0 / | 0 ) | 0.00 |
| mux_retime | 0 | ( | 0 / | 0 ) | 0.00 |
| buf2inv | 0 | ( | 0 / | 0 ) | 0.00 |
| exp | 0 | ( | 0 / | 0 ) | 0.00 |
| gate_deco | 0 | ( | 0 / | 0 ) | 0.00 |
| gcomp_tim | 0 | ( | 0 / | 0 ) | 0.00 |
| inv_pair_2_buf | 0 | ( | 0 / | 0 ) | 0.00 |

| Trick | Calls | | Accepts | Attempts | Time(secs) |
|---|---|---|---|---|---|
| crr_220 | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_glob | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_200 | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_glob | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_300 | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_glob | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_400 | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_glob | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_111 | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_glob | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_210 | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_glob | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_110 | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_glob | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_101 | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_glob | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_201 | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_glob | 0 | ( | 0 / | 0 ) | 0.00 |
| crr_211 | 0 | ( | 0 / | 0 ) | 0.00 |

```
       crr_glob         0  (        0 /        0 )  0.00
       crit_msz         0  (        0 /        0 )  0.00
      crit_upsz         0  (        0 /        0 )  0.00
      crit_slew         0  (        0 /        0 )  0.00
       setup_dn         0  (        0 /        0 )  0.00
   plc_bal_star         0  (        0 /        0 )  0.00
    drc_buftimb         0  (        0 /        0 )  0.00
         plc_st         0  (        0 /        0 )  0.00
   plc_st_fence         0  (        0 /        0 )  0.00
       plc_star         0  (        0 /        0 )  0.00
     plc_laf_st         0  (        0 /        0 )  0.00
plc_laf_st_fence         0  (        0 /        0 )  0.00
    drc_buftims         0  (        0 /        0 )  0.00
      plc_lo_st         0  (        0 /        0 )  0.00
           fopt         0  (        0 /        0 )  0.00
      crit_swap         0  (        0 /        0 )  0.00
      mux2_swap         0  (        0 /        0 )  0.00
      crit_dnsz         0  (        0 /        0 )  0.00
      load_swap         0  (        0 /        0 )  0.00
           fopt         0  (        0 /        0 )  0.00
       setup_dn         0  (        0 /        0 )  0.00
      load_isol         0  (        0 /        0 )  0.00
      load_isol         0  (        0 /        0 )  0.00
       move_for         0  (        0 /        0 )  0.00
       move_for         0  (        0 /        0 )  0.00
         rem_bi         0  (        0 /        0 )  0.00
        offload         0  (        0 /        0 )  0.00
         rem_bi         0  (        0 /        0 )  0.00
        offload         0  (        0 /        0 )  0.00
      merge_bit         0  (        0 /        0 )  0.00
    merge_idrvr         0  (        0 /        0 )  0.00
    merge_iload         0  (        0 /        0 )  0.00
   merge_idload         0  (        0 /        0 )  0.00
     merge_drvr         0  (        0 /        0 )  0.00
     merge_load         0  (        0 /        0 )  0.00
          phase         0  (        0 /        0 )  0.00
         decomp         0  (        0 /        0 )  0.00
       p_decomp         0  (        0 /        0 )  0.00
```

```
        levelize         0  (        0 /        0 )  0.00
        mb_split         0  (        0 /        0 )  0.00
        in_phase         0  (        0 /        0 )  0.00
             dup         0  (        0 /        0 )  0.00
      mux_retime         0  (        0 /        0 )  0.00
         buf2inv         0  (        0 /        0 )  0.00
             exp         0  (        0 /        0 )  0.00
       gate_deco         0  (        0 /        0 )  0.00
       gcomp_tim         0  (        0 /        0 )  0.00
  inv_pair_2_buf         0  (        0 /        0 )  0.00
 init_drc                    158        0          0         0        0

           Trick     Calls     Accepts   Attempts    Time(secs)
-------------------------------------------------------------
          plc_st         0  (        0 /        0 )  0.00
        plc_star         0  (        0 /        0 )  0.00
        drc_bufs         0  (        0 /        0 )  0.00
        drc_fopt         0  (        0 /        0 )  0.00
        drc_bufb         0  (        0 /        0 )  0.00
      simple_buf         0  (        0 /        0 )  0.00
             dup         0  (        0 /        0 )  0.00
       crit_dnsz         0  (        0 /        0 )  0.00
       crit_upsz         0  (        0 /        0 )  0.00
       crit_slew         0  (        0 /        0 )  0.00


           Trick     Calls     Accepts   Attempts    Time(secs)
-------------------------------------------------------------
          plc_st         0  (        0 /        0 )  0.00
        plc_star         0  (        0 /        0 )  0.00
      drc_buf_sp         0  (        0 /        0 )  0.00
        drc_bufs         0  (        0 /        0 )  0.00
        drc_fopt         0  (        0 /        0 )  0.00
        drc_bufb         0  (        0 /        0 )  0.00
      simple_buf         0  (        0 /        0 )  0.00
             dup         0  (        0 /        0 )  0.00
       crit_dnsz         0  (        0 /        0 )  0.00
       crit_upsz         0  (        0 /        0 )  0.00
```

```
           Trick     Calls     Accepts   Attempts    Time(secs)
-------------------------------------------------------------
          plc_st         0  (        0 /        0 )  0.00
        plc_star         0  (        0 /        0 )  0.00
      drc_buf_sp         0  (        0 /        0 )  0.00
        drc_bufs         0  (        0 /        0 )  0.00
        drc_fopt         0  (        0 /        0 )  0.00
        drc_bufb         0  (        0 /        0 )  0.00
             dup         0  (        0 /        0 )  0.00
       crit_dnsz         0  (        0 /        0 )  0.00
       crit_upsz         0  (        0 /        0 )  0.00

 init_tns                  158        0         0         0        0

           Trick     Calls     Accepts   Attempts    Time(secs)
-------------------------------------------------------------
            fopt         0  (        0 /        0 )  0.00
    plc_bal_star         0  (        0 /        0 )  0.00
     drc_buftimb         0  (        0 /        0 )  0.00
     drc_buftims         0  (        0 /        0 )  0.00
        crit_msz         0  (        0 /        0 )  0.00
       crit_upsz         0  (        0 /        0 )  0.00
   plc_laf_lo_st         0  (        0 /        0 )  0.00
       plc_lo_st         0  (        0 /        0 )  0.00
       crit_swap         0  (        0 /        0 )  0.00
       mux2_swap         0  (        0 /        0 )  0.00
       crit_dnsz         0  (        0 /        0 )  0.00
       load_swap         0  (        0 /        0 )  0.00
            fopt         0  (        0 /        0 )  0.00
        setup_dn         0  (        0 /        0 )  0.00
       load_isol         0  (        0 /        0 )  0.00
       load_isol         0  (        0 /        0 )  0.00
        move_for         0  (        0 /        0 )  0.00
        move_for         0  (        0 /        0 )  0.00
          rem_bi         0  (        0 /        0 )  0.00
         offload         0  (        0 /        0 )  0.00
```

```
          rem_bi         0  (        0 /        0 )  0.00
         offload         0  (        0 /        0 )  0.00
       merge_bit         0  (        0 /        0 )  0.00
     merge_idrvr         0  (        0 /        0 )  0.00
     merge_iload         0  (        0 /        0 )  0.00
    merge_idload         0  (        0 /        0 )  0.00
      merge_drvr         0  (        0 /        0 )  0.00
      merge_load         0  (        0 /        0 )  0.00
           phase         0  (        0 /        0 )  0.00
          decomp         0  (        0 /        0 )  0.00
        p_decomp         0  (        0 /        0 )  0.00
        levelize         0  (        0 /        0 )  0.00
        mb_split         0  (        0 /        0 )  0.00
             dup         0  (        0 /        0 )  0.00
      mux_retime         0  (        0 /        0 )  0.00
       crr_local         0  (        0 /        0 )  0.00
         buf2inv         0  (        0 /        0 )  0.00

 init_area                  158        0         0         0        0

           Trick     Calls     Accepts   Attempts    Time(secs)
-------------------------------------------------------------
           undup         0  (        0 /        0 )  0.00
         rem_buf         0  (        0 /        0 )  0.00
         rem_inv         0  (        0 /        0 )  0.00
        merge_bi         0  (        0 /        0 )  0.00
      rem_inv_qb         0  (        0 /        0 )  0.00
    seq_res_area         0  (        0 /        0 )  0.00
        io_phase         0  (        0 /        0 )  0.00
       gate_comp         0  (        0 /        0 )  0.00
       gcomp_mog         0  (        0 /        0 )  0.00
       glob_area         4  (        0 /        4 )  0.00
       area_down         1  (        0 /        0 )  0.01
      size_n_buf         0  (        0 /        0 )  0.00
  gate_deco_area         0  (        0 /        0 )  0.00
         rem_buf         0  (        0 /        0 )  0.00
         rem_inv         0  (        0 /        0 )  0.00
        merge_bi         0  (        0 /        0 )  0.00
```

```
      rem_inv_qb         0  (        0 /        0 )  0.00


Incremental optimization status
===============================
                                    Group
                                   Tot Wrst     Total - - DRC Totals -
-
                          Total  Weighted      Neg      Max       Max
Operation                  Area   Slacks      Slack    Trans      Cap
 init_delay                 158        0         0        0        0

           Trick     Calls     Accepts   Attempts    Time(secs)
-------------------------------------------------------------
        crit_msz         0  (        0 /        0 )  0.00
       crit_upsz         0  (        0 /        0 )  0.00
       crit_slew         0  (        0 /        0 )  0.00
        setup_dn         0  (        0 /        0 )  0.00
    plc_bal_star         0  (        0 /        0 )  0.00
     drc_buftimb         0  (        0 /        0 )  0.00
          plc_st         0  (        0 /        0 )  0.00
    plc_st_fence         0  (        0 /        0 )  0.00
        plc_star         0  (        0 /        0 )  0.00
      plc_laf_st         0  (        0 /        0 )  0.00
 plc_laf_st_fence         0  (        0 /        0 )  0.00
     drc_buftims         0  (        0 /        0 )  0.00
   plc_laf_lo_st         0  (        0 /        0 )  0.00
       plc_lo_st         0  (        0 /        0 )  0.00
            fopt         0  (        0 /        0 )  0.00
       crit_swap         0  (        0 /        0 )  0.00
       mux2_swap         0  (        0 /        0 )  0.00
       crit_dnsz         0  (        0 /        0 )  0.00
       load_swap         0  (        0 /        0 )  0.00
            fopt         0  (        0 /        0 )  0.00
        setup_dn         0  (        0 /        0 )  0.00
       load_isol         0  (        0 /        0 )  0.00
       load_isol         0  (        0 /        0 )  0.00
        move_for         0  (        0 /        0 )  0.00
```

```
       move_for          0  (        0 /        0 )  0.00
         rem_bi          0  (        0 /        0 )  0.00
        offload          0  (        0 /        0 )  0.00
         rem_bi          0  (        0 /        0 )  0.00
        offload          0  (        0 /        0 )  0.00
          phase          0  (        0 /        0 )  0.00
       in_phase          0  (        0 /        0 )  0.00
      merge_bit          0  (        0 /        0 )  0.00
    merge_idrvr          0  (        0 /        0 )  0.00
    merge_iload          0  (        0 /        0 )  0.00
   merge_idload          0  (        0 /        0 )  0.00
     merge_drvr          0  (        0 /        0 )  0.00
     merge_load          0  (        0 /        0 )  0.00
         decomp          0  (        0 /        0 )  0.00
       p_decomp          0  (        0 /        0 )  0.00
       levelize          0  (        0 /        0 )  0.00
       mb_split          0  (        0 /        0 )  0.00
            dup          0  (        0 /        0 )  0.00
     mux_retime          0  (        0 /        0 )  0.00
        buf2inv          0  (        0 /        0 )  0.00
            exp          0  (        0 /        0 )  0.00
      gate_deco          0  (        0 /        0 )  0.00
      gcomp_tim          0  (        0 /        0 )  0.00
  inv_pair_2_buf         0  (        0 /        0 )  0.00

 init_drc                   158        0         0         0        0

          Trick     Calls     Accepts   Attempts    Time(secs)
-------------------------------------------------------------
         plc_st          0  (        0 /        0 )  0.00
       plc_star          0  (        0 /        0 )  0.00
       drc_bufs          0  (        0 /        0 )  0.00
       drc_fopt          0  (        0 /        0 )  0.00
       drc_bufb          0  (        0 /        0 )  0.00
     simple_buf          0  (        0 /        0 )  0.00
            dup          0  (        0 /        0 )  0.00
      crit_dnsz          0  (        0 /        0 )  0.00
      crit_upsz          0  (        0 /        0 )  0.00
```

```
       crit_slew         0  (        0 /        0 )  0.00


           Trick     Calls     Accepts   Attempts    Time(secs)
-------------------------------------------------------------
          plc_st         0  (        0 /        0 )  0.00
        plc_star         0  (        0 /        0 )  0.00
        drc_bufs         0  (        0 /        0 )  0.00
        drc_fopt         0  (        0 /        0 )  0.00
        drc_bufb         0  (        0 /        0 )  0.00
      simple_buf         0  (        0 /        0 )  0.00
             dup         0  (        0 /        0 )  0.00
       crit_dnsz         0  (        0 /        0 )  0.00
       crit_upsz         0  (        0 /        0 )  0.00


           Trick     Calls     Accepts   Attempts    Time(secs)
-------------------------------------------------------------
          plc_st         0  (        0 /        0 )  0.00
        plc_star         0  (        0 /        0 )  0.00
        drc_bufs         0  (        0 /        0 )  0.00
        drc_fopt         0  (        0 /        0 )  0.00
        drc_bufb         0  (        0 /        0 )  0.00
             dup         0  (        0 /        0 )  0.00
       crit_dnsz         0  (        0 /        0 )  0.00
       crit_upsz         0  (        0 /        0 )  0.00

==================================
Stage : incr_opt
==================================
  =================
   Message Summary
  =================
-------------------------------------------------------------------------
---------------------------------------
|   Id    |  Sev   |Count |                                  Message
Text                                    |
```

```
--------------------------------------------------------------------------
--------------------------------------
| CFM-1   |Info    |    1 |Wrote dofile.
|
| CFM-5   |Info    |    1 |Wrote formal verification information.
|
| CPI-506 |Warning |    1 |Command 'commit_power_intent' cannot
proceed as there is no power intent loaded. |
| PA-7    |Info    |    4 |Resetting power analysis results.
|
|         |        |      |All computed switching activities are
removed.                                    |
| RPT-16  |Info    |    1 |Joules engine is used.
|
| SYNTH-5 |Info    |    1 |Done mapping.
|
| SYNTH-7 |Info    |    1 |Incrementally optimizing.
|
--------------------------------------------------------------------------
--------------------------------------
Info    : Done incrementally optimizing. [SYNTH-8]
        : Done incrementally optimizing 't1c_riscv_cpu'.
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.10-p002_1
  Generated on:           Jan 23 2025  07:34:40 pm
  Module:                 t1c_riscv_cpu
  Technology library:     slow_vdd1v0 1.0
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


  Gate    Instances   Area       Library
-----------------------------------------
INVX1             1    0.684    slow_vdd1v0
INVXL             1    0.684    slow_vdd1v0
MX2XL            64  153.216    slow_vdd1v0
```

```
NAND2BXL           1    1.368    slow_vdd1v0
OR2X2              1    1.710    slow_vdd1v0
-------------------------------------------
total             68  157.662


     Type      Instances   Area  Area %
-----------------------------------------
inverter               2   1.368    0.9
unresolved             3   0.000    0.0
logic                 66 156.294   99.1
physical_cells         0   0.000    0.0
-----------------------------------------
total                 71 157.662  100.0


 No LEF file read in.
Finished SDC export (command execution time mm:ss (real) = 00:01).
Info    : Joules engine is used. [RPT-16]
        : Joules engine is being used for the command report_power.
Output file: ./reports/power.txt
legacy_genus:/> elaborate
legacy_genus:/> gui_show
legacy_genus:/>
```