Mentor

1 point

Course outline

Prerequisite: Week 0

based VLSI Design

Week2: C-Based VLSI

Week3: C-Based VLSI

Week 4: C-Based VLSI

Lec1: Forced Directed

Lecture Note for Lec1

Lec2: Forced Directed MLRC

Lec3: Path Based Scheduling

Lec4: Path Based Scheduling

Quiz: Week 4: Assignment 4

and MRLC Scheduling

Lecture Note for Lec2

Lecture Note for Lec3

Lecture Note for Lec4

Week 4: Feedback form

Solution: Assignment 4

Week 5: C-Based VLSI Design: Allocation and

Week 6: C-Based VLSI

Week 7: C-Based VLSI

Week 8: C-Based VLSI

Week 9: C-Based VLSI

level Synthesis

Design: Allocation, Binding,

Design: Efficient Synthesis of

Design: Hardware Efficient C

Design: Impact of Compiler

Optimizations in Hardware

Week 11: Securing Design

with High-level Synthesis

Week 12: Introduction to EDA

and Recent Advances in C-

Based VLSI Design

Download

Live Sessions

Week 10: Verification of High-

Data-path and Controller

Binding

Generation

C Code

Coding

Design: Advanced

Scheduling

Algorithm

Design: List Based

Scheduling

Scheduling

Design: Basic Scheduling

Week1: Introduction to C-

course work?

How does an NPTEL online

Week 4: Assignment 4

The due date for submitting this assignment has passed.

Due on 2021-09-01, 23:59 IST. As per our records you have not submitted this assignment.

Consider the Sequence Graph shown in the figure below. Each MUL (performs multiplication operation) and ALU (performs rest operations) operation takes one unit of time (i.e., single cycle). The latency bound $\lambda = 5$. Please note that the dummy operations 0 and n do not take any time step. Operations 1 to 11 will be scheduled during time steps 1 to 5. Answer the following questions from 1 to 9 for

repeat {

Compute the time-frames;

Compute the operation and type probabilities;

Compute the self-forces, predecessor/successor forces and total forces;

Schedule the operation with least force and update its time-frame;
}

until (all operations are scheduled);

return (t);
}

1) What is the ASAP and ALAP times of operation 6?

minimizing resources under latency constrained (MRLC) Force-Directed scheduling.

1) What is the ASAP and ALAP times of operation 6?

1, 3

3, 1

1, 2

2, 1

No, the answer is incorrect. Score: 0

Accepted Answers: 1, 3

○3 ○2 ○1

Accepted Answers:
3

3) Select the correct ALAP time of operations 3 and 11?

2) What is the mobility of operation 8?

No. the answer is incorrect.

Score: 0

2,2

3, 1

0[1,3]

Score: 0

[1, 4]

No, the answer is incorrect.

No, the answer is incorrect.

Accepted Answers:

Accepted Answers:

3, 2
2, 5
3, 5

No, the answer is incorrect.
Score: 0

3, 54) How many number of MUL and ALU required for this MRLC Schedule

○ 2, 2 ○ 1, 1 ○ 2, 1

Score: 0
Accepted Answers: 2, 1

5) What is the time frame of operation 10?

○ [1, 4] ○ [1, 5] ○ [2, 5]

6) The probability of operations 1 and 10 at time step 1 are

0.5, 0.25

0.33, 0.25

0.5, 0.33

No, the answer is incorrect.
Score: 0

Accepted Answers:
0.5, 0.25

7) The value of the MUL resource type distribution at time step 1 is

1.83

0.25

1.58

O 2.83

No, the answer is incorrect.
Score: 0

Accepted Answers:
1.58

○ 0.415 ○ 0.25 ○ -0.25

O -0.415

No, the answer is incorrect.
Score: 0

Accepted Answers:
-0.415

9) The assignment of operation 2 to time step 2 implies that the assignment of operation 3 to time step 3. Therefore, the force of 1 point

○ 0.415 ○ 0.25

○ -0.25
○ -0.415

No, the answer is incorrect.
Score: 0
Accepted Answers:

for(__)

10) Consider the following code. How many longest paths are there in the behavior?

8) When operation 2 is assigned to time step 1, what is the self-force for operation 2:

1. ppc = pc

2. popc = oldpc

3. pbus = ibus + 4

4. if(branch==1)

5. pc = branchpc;

6. endif

5. pc = branchpc;
6. endif
7. while(irel=1); //Busy Wait//
8. oldpc = pc
9. pc = pc + 4
10. Endop
}

operation 3 related to time step 3 is:

-0.25

No, the answer is incorrect.
Score: 0
Accepted Answers:

04