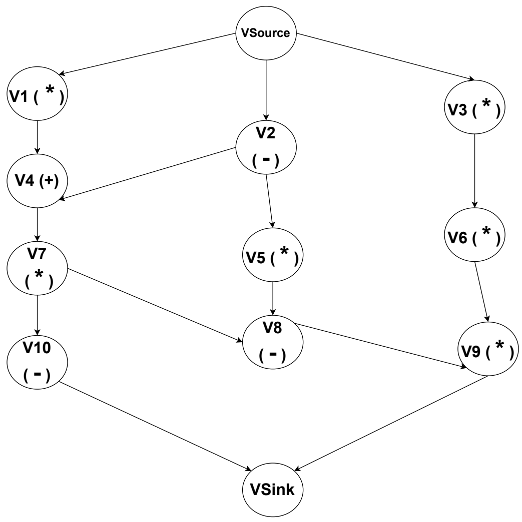
C-Based VLSI (CS 577) Mid Sem Examination (Part B)

Total Marks: 30

Name:

Roll No:

1. Given 2 resources of type Mult $(*)$ and 2 resources of type ALU $(+, -, <)$ and each operation of the unit cycle, answer the following questions on ILP formulation of the following sequence graph. Write your answers based on the Boolean variable x_{il}, where i represents the node v_i and l is the time step. Consider the ASAP and ALAP bound for x_{il}. To compute ALAP, consider the latency obtained by ASAP scheduling. (2+2+4+3+4 =15)



   (a) Write the objective function of ML-RC scheduling.

   (b) Write the objective fn. of MR-LC scheduling assuming the cost of MULT and ALU as 10 and 2, respectively.

   (c) Determine the correct inequality representing the data dependency constraint (i) between operations V3 and V6 and (ii) between operations V5 and V8.

   (d) Write down the inequality representing the unique start time of operations V3 and V9.

   (e) Determine the resource constraints in the time step 3.

2. Consider the following code snippet: $a = b + c$; $d = d + b$; $x = a - d$; The questions are interdependent. Use the solution of the previous question to answer the next: (2 + 3 + 3 + 4 + 3 == 15)

   (a) Schedule the behavior considering only one ALU $(+, -)$ and each operation is a single cycle.

   (b) Identify the lifetime of the variables (draw only a diagram to show lifetime).

   (c) Find the variable to register mapping where at most two variables can be mapped to one register.

   (d) Draw the datapath of the design. The datapath must use minimum-size multiplexers (some code modification may need to achieve that).

   (e) Find the control signal value in each state and draw the final controller FSM.

Variable	a	b	c	d	x
Register					

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(Supplementary Answer Sheet)

Name of Student :		Roll No.	
Course No.		Signature of the student :	

Q 1 Subjective

ASAP

1)	V_1	V_3	V_2	
2)	V_6	V_5	V_4	
3)	V_7			
4)			V_{10}	V_8
5)	V_9			

ALAP

1	V_1	V_2
2		V_4
3	V_7 V_5 V_3	
4	V_6	V_8
5	V_9	V_{10}

a) MLRC obj. fun = $C^T . t$ $\{ C = [0 \ 0 \ 0 \cdots 1]$.

b) Obj. fun. MRLC = $C^T a$

$$= [10 \ \ 2] \begin{bmatrix} a_{MUL} \\ a_{ALU} \end{bmatrix}$$

$$= 10 . a_{MUL} + 2 a_{ALU}$$

c) Data dependency

i) $(V_3 \to V_6)$

$$2 x_{6,2} + 3 x_{6,3} + 4 x_{6,4} \geq x_{3,1} + 2 x_{3,2} + 3 x_{3,3} + 1$$

ii) $(V_5 \to V_8)$

$$4 x_{8,4} \geq 2 x_{5,2} + 3 x_{5,3} + 1$$

d) Unique Start time

$V_3 = x_{3,1} + \cancel{2} x_{3,2} + \cancel{3} x_{3,3} = 1$

$V_9 = \cancel{5} x_{9,5} = 1$

e) Resource constraint at t.s 3

MUL = $x_{3,3} + x_{7,3} + x_{5,3} + x_{6,3} \leq 2$

or $x_{3,3} + x_{5,3} + x_{6,3} \leq 1$

ALU = No op.

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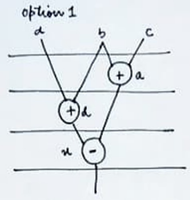
Q2 Part B

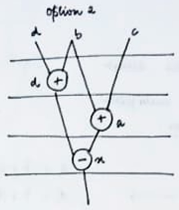
$a = b + c;$
$d = d + b;$
$x = a - d;$

(a) Considering only one ALU Schedule: (both option will be considered correct).

option 1

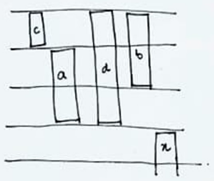


option 2

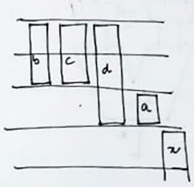


(b) lifetime of the variables

option1



option 2.



(c) Variable to register mapping

option1.1		option 1.2	option 2.1		option 2.2
R1 = a, c		R1 = a, x	R1 = d		R1 = d
R2 = d	OR	R2 = d, x	R2 = b, a	OR	R2 = b, x
R3 = b, x		R3 = b	R3 = c, x		R3 = a, c

~~R1 = a, x~~
~~R2 = d~~
~~R3 = b, x~~ .

(d) Datapath of the design
for minimum-size multipliers
code modification :

$a = b + c$ $\qquad$ $a = b + c$
$d = d + b$ $\longrightarrow$ $d = b + d$
$x = a - d$ $\qquad$ $x = a - d.$

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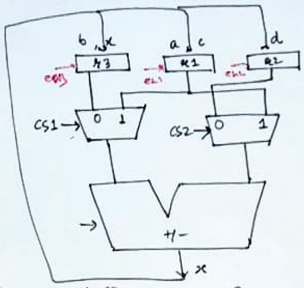
(d)

option 1.1



(e)

	cs1	cs2	en1	en2	e3
es1	0	1	1	0	0
es2	0	0	0	1	0
es3	1	0	0	0	1