1 point

1 point

1 point

1 point

Course outline

Prerequisite: Week 0

based VLSI Design

Week2: C-Based VLSI

Week3: C-Based VLSI

Week 4: C-Based VLSI

Week 5: C-Based VLSI Design: Allocation and

Week 6: C-Based VLSI

Week 7: C-Based VLSI

Lec 1: HLS for Arrays

Lecture Note for Lec1

Lec 2: HLS for Loops

Lecture Note for Lec3

Week 7: Feedback Form

Solution: Assignment 7

Week 8: C-Based VLSI

Week 9: C-Based VLSI

level Synthesis

Coding

Design: Hardware Efficient C

Design: Impact of Compiler

Optimizations in Hardware

Week 11: Securing Design

with High-level Synthesis

Week 12: Introduction to EDA

and Recent Advances in C-

Based VLSI Design

Download

Live Sessions

Week 10: Verification of High-

Lec3: HLS for Loop - pipeline

Quiz: Week 7: Assignment 7

Design: Allocation, Binding,

Design: Efficient Synthesis of

Data-path and Controller

Design: List Based

Design: Advanced

Scheduling

Scheduling

Binding

Generation

C Code

Design: Basic Scheduling

Week1: Introduction to C-

course work?

How does an NPTEL online

NPTEL » C-Based VLSI Design

Week 7: Assignment 7

The due date for submitting this assignment has passed.

Due on 2021-09-15, 23:59 IST.

As per our records you have not submitted this assignment.

 Consider the code-snippet given below: 2 points Let us assume that the array A is mapped to a Block RAM. Given one addition takes a single cycle and two adders are available, which of the following statements are correct? Assume that no source-code modification is done. Also, ignore the time needed to modify the loop iterator i. Only consider the time needed to execute the loop body.

- S1: A single-port RAM will take 10 cycles to execute the entire module.
- S2: A dual-port RAM will take 8 cycles to execute the entire module.

```
void fn(int A[20])
    for(i = 18; i < 20; i++)
        Sum[i] = A[i] + A[i-1] + A[i-2] + A[i-3];

    Both S1 and S2 are correct
```

- Only S1 is correct
- Only S2 is correct Neither S1 nor S2 is correct

No, the answer is incorrect. Score: 0

Accepted Answers: Both S1 and S2 are correct

- While merging multiple arrays vertically, extra locations on the RAM are :
 - padded with 1's. padded with 0's.
- padded with random values.
- not padded.
- Score: 0 Accepted Answers:

No, the answer is incorrect.

padded with 0's.

Consider the code-snippets given below: Assume that A and B are single-port RAMs and C is a dual-port RAM, all having width 32 bits where 32 bits is the size of an integer. Code snippet 2 is

obtained by combining A and B into C. What is the optimization done here?

Code snippet 1:

```
int A[1000], B[200];
for(i = 1 to 1000)
```

```
A[i] = value1;
        if(i<200)
            B[i] = value2;
    }
Code snippet 2:
    int C[1200];
    for(i = 1 to 1000)
        C[i] = value1;
        if(i<200)
            C[i+1000] = value2;
```

Array Horizontal merging

Array partitioning

- Array vertical merging
- Array access permutation
- No, the answer is incorrect.

2)

a1

a6

Score: 0 Accepted Answers:

Array Horizontal merging

a1

1)

4) Consider an array A is partitioned into multiple small arrays. Which of the following represents correct Block Array Partitioning?

```
0
a2
                         5
      3 6 9
                        a7
                                 a2
                   1
                         6
                                  5 6
                                         8
                        a8
                   2
                         7
   2 5 8
                        a9
                   3
                         8
   a1
                  a5
                        a10
                         9
                   4
    6 7 8 9
1) only
1) and 4)
```

3)

a1

- 3) only
 - 1), 3) and 4)
- No, the answer is incorrect. Score: 0

Accepted Answers:

only

 The interval in which outputs are produced Number of cycles needed to process one set of inputs.

Initiation interval in loop-pipelining is:

- Number of cycles between the start of two consecutive iterations. Number of cycles between two outputs.
- No, the answer is incorrect. Score: 0

Accepted Answers: Number of cycles between the start of two consecutive iterations.

Consider the code below. Assume that only one Single Port Block RAM R1 of size 1K and the word size of 70 bits is available. How can you

map the arrays A1 and A2 to R1 so that the below code can be executed using the RAM R1? Select the appropriate option. int A1[1000], A2[500];

```
for (i = 0; I < 1000; i++)
  A1[i] = some data;
  if (i<500)
     A2[i] = some data;
  Merge A1 and A2 vertically to RAM R1
  Merge A1 and A2 horizontally to RAM R1
  Partition RAM R1 to two RAMs vertically
```

- Partition RAM R1 to two RAMs horizontally
- No, the answer is incorrect. Score: 0 Accepted Answers:

Merge A1 and A2 vertically to RAM R1

7) Consider a loop in which each iteration of the loop is scheduled in 4 time steps. The loop is implemented in fully pipelined mode with initiation 1 point interval 1. The loop has 20 iterations. How many time steps is required to execute the loop body?

20 080

- No, the answer is incorrect.
- 23

O 21

Score: 0

Accepted Answers: 23

8) A loop in a C program is synthesized to RTL by HLS tool. Which of the following optimization are applied on Loop by the HLS tool? Select the 1 point

- Loop pipelining
- Score: 0

Accepted Answers: All of the above

best possible option. Loop Unrolling Rolled implementation of Loop All of the above No, the answer is incorrect.