C-Based VLSI (CS 577) Mid Sem Examination (Part A)

Total Marks: 50

Name:

Roll No:

Instructions: Write the answers on the question paper only for both parts. The supplementary sheet is for rough work only. It won't be evaluated. You need to submit your supplementary sheets as well.

1. Consider the following code. Assume that the array access requires no additional time and no operation chaining is allowed. Assume the loop is unrolled by 4. (3 + 3)

   for$(a[20], b[20], c[20], d[20])$ {
   $out[i] = a[i] + b[i] + c[i] + d[i];$
   }

   Case1: Assume that you have unbounded resources. What will be the total latency to execute the complete loop?

   Case2: Assume you have 4 Adders. What will be the total latency to execute the complete loop?

   Answer: Case1: 10 Case2: 15

2. Consider the following function. (4 + 4)

```
fun1(a, b, c ,d, e) {
    t1= a+b;
    t2= t1-c;
    t3= t2+d;
    t4= t3+e; }
```

   (a) For non-pipelined implementation with no operation chaining, the latency (L), initiation interval (II) and throughput (TP) respectively.

   Answer: L: 4 II: 4 TP: $1/4$ or 4

   (b) For the fully-pipelined version, the latency, initiation interval and throughput respectively.

   Answer: L: 4 II: 1 TP: 1

3. Consider the sequence graph in Figure 1 and answer the following questions with respect to ASAP and ALAP schedules. Delay of '+' is 2 , delay of '*' is 3 and the delay of '<' and '>' is 1. Find the ASAP solution. Then use the ASAP latency to find the ALAP schedule. (3 + 3 + 3)

   (a) The latency of ASAP schedule is : 9

   (b) If T_i^s is the ASAP schedule a node V_i and T_i^l is the ALAP schedule a node V_i. Find the value of

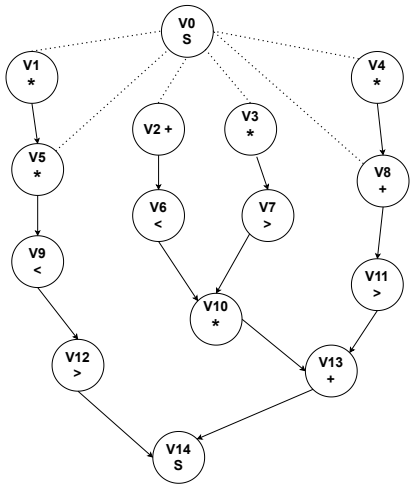

Figure 1: Sequence Graph for Question 3

   $2T_{12}^s + 3T_7^s - 5T_3^l$.

   Answer: 23

   (c) If 'x' is the number of operations with mobility 1, 'y' is the number of operations with mobility 2 and 'z' is the number of operations with mobility zero. Find the value of $xy - yz - zx + 2xyz$

   Answer: -36

4. Choose the correct option regarding the hardness of MRLC, MLRC and unconstrained scheduling. (2)

   (a) MRLC - P, MLRC - P, unconstrained - P

   (b) MRLC - NP-complete, MLRC - NP-complete, unconstrained - NP-complete

   (c) MRLC - NP-hard, MLRC - NP-hard, unconstrained NP-complete

   (d) None of the above.

5. Consider the following code snippet.

```
Void Fun(int A[30],int B[30]) {
   int sum = 0;
   for(int i=0; i<28; i++) {
      Sum = sum+A[i]+A[i+1]+A[i+2];
   }
   for (int i=0; i<27; i++) {
    Sum = sum+B[i]+B[i+2]+B[i+3]+B[i+1];
   }
```

   Assume that the array A and array B map to separate Dual

port RAM. Assume that reading from memory takes one clock cycle. (3 + 3)

(a) How many cycles of array read operation are required to read A and B from memory?

Answer: $56 + 54 = 110$

(b) Optimize the code to reduce array access. The objective is to read the array element once and store locally and reuse. In your optimized code, how many cycles of array read operation are required? (3)

Answer: $(2 + 27) + (2 + 26) = 57$

6. Consider an array of size 1024, say P[1024], and identify array partition styles given in Figure 2. (3)

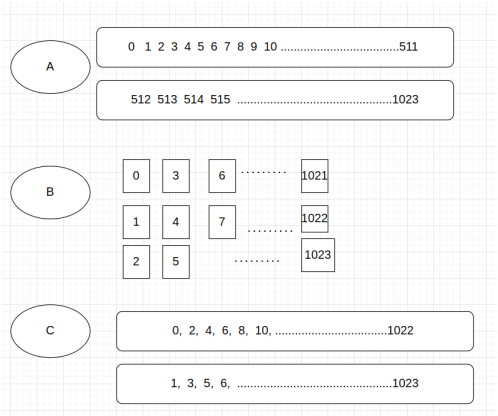

Figure 2: Array partition

(a) A: Cyclic, B: Block, C: Complete

(b) A: Cyclic, B: Complete, C: Block

(c) A: Block, B: Cyclic, C: Complete

(d) A: Block, B: Complete, C: Cyclic

7. Consider the arrays $A1 = 1000 * 32$ bits, $A2 = 512 * 32$ bits and $A3 = 256 * 64$ bits each and also RAM of size $1750 * 90$ bits. Select the correct option (3)

(a) Horizontal merging is possible, vertical merging is not possible

(b) Horizontal merging partitioning possible, vertical merging is possible

(c) Horizontal merging is not possible, vertical merging is possible

(d) Horizontal merging is not possible, vertical merging is not possible

8. The below code is not synthesizable by HLS due to system calls. How many system calls must be modified in the code to make it synthesizable? (2)

```
void randombytes(uint8_t *out, size_t outlen)
{
ssize_t ret;
while(outlen > 0) {
  ret = syscall(SYS_getrandom,out, outlen, 0);
        for(int i = 0; i < outlen; i++) {
                out[i] = 0;
        }
        if(ret == -1 && errno == EINTR)
                continue;
        else if(ret == -1)
                abort();
        out += ret;
        outlen -= ret;
}
```

Answer: 2

9. Given the following sequence graph and the following assumptions: There are 2 Multipliers and 2 ALUs available. The delay of Multipler is 2 units and the delay of ALU is 1. The priority function of node v is the longest path from it to the sink node. Schedule the graph with above constraints using MLRC List Scheduling. (3 + 2 + 2 + 2 + 2)

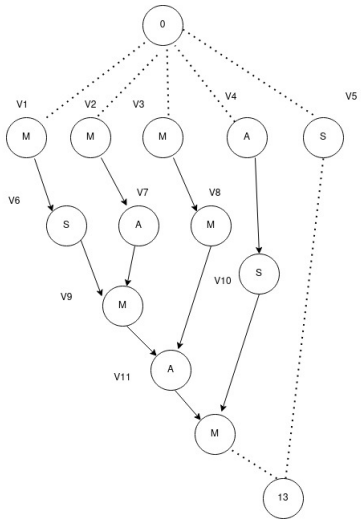

Figure 3: Data dependency graph, M: Multiplication, A: Addition, S: Subtraction

(a) What is the Latency of the schedule?

Answer: 9

(b) The start time of operation V9 is

Answer: 4

(c) The start time of operation V8 is

Answer: 5

(d) How many operations are running in time step 2?

Answer: 3

(e) What is the priority value of node V3?

Answer: 4

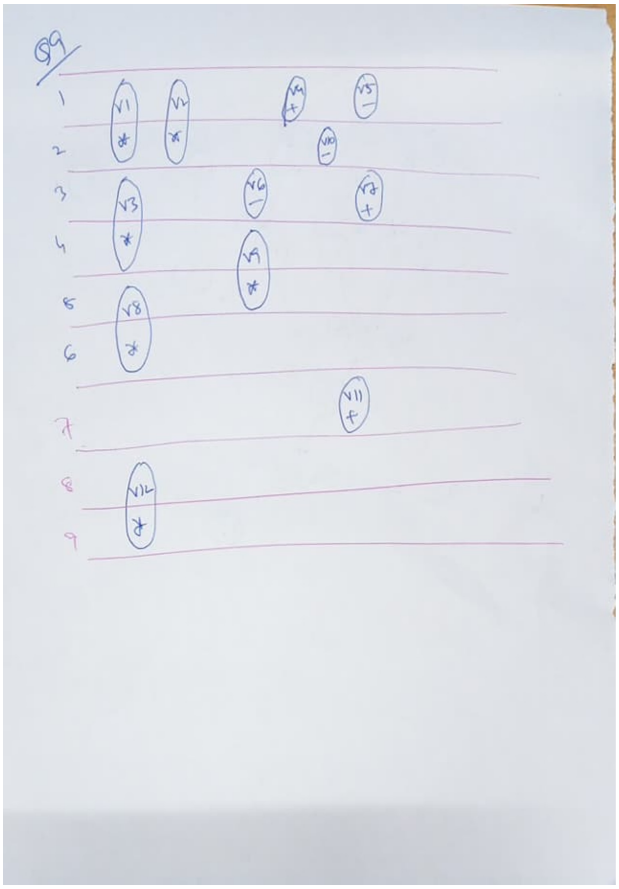

Figure 4: Q9 Sequence Graph.