CS577: C-Based VLSI Design
Mid Sem - Part 1

Questions: 20, Time: 30 mins, Total Marks: 40

Points: 17/40

✓ **Correct** 2/2 Points

1. **(Figure 1)**What is the ASAP and ALAP time of operation 7

(c) 3, 4

(b) 2, 4

(d) 1, 3

(a) 2, 3

✓ **Correct** 3/3 Points

2. **(Figure 3)** Let us assume that all operations can be executed using a same type of resource (i.e., multiprocessor scheduling) for the below sequence graph. Consider the Hu's algorithm for the same. If the latency bound is 4, what would be the minimum number of resource needed to schedule the below sequence graph?

3

✓ **Correct** 1/1 Points

3. Data dependencies among operations and the basic blocks are identified at which step of HLS

(d) Allocation phase

(a) Preprocessing phase

(b) Controller design phase.

(c) Scheduling phase.

✓ **Correct** 2/2 Points

4. **(Figure 1)** What is the probability of operation 3 at time step 1?

- (c) 0.5
- (a) 0.33
- (d) 0.125
- (b) 0.25

✗ **Incorrect** 0/3 Points

5. **(Figure 1)**The value of ALU resource type distribution at time step 2 is (select the nearest option)

- (a) 1
- (d) 1.33
- (b) 1.08
- (c) 1.17

✓ **Correct** 2/2 Points

6. **(Figure 1)** Select the correct ALAP time of operation 3 and 8

- (d) 3, 3
- (c) 4, 3
- (a) 3, 4
- (b) 4, 4

✗ **Incorrect** 0/2 Points

7. **(Figure 2)**Determine the correct inequality representing the dependency constraint between operations 3 and 7

- (c) X3,1 + 2X3, 2 + 3X3, 3 + 1 <= 2X7, 2 + 3X7, 3
- (b) X3,1 + 2X3, 2 + 1 <= 2X7, 2 + 3X7, 3 + 4X7, 4
- (d) X3,1 + 2X3, 2 + 1 <= 2X7, 2 + 3X7, 3
- (a) X3,1 + 2X3, 2 + 3X3, 3 + 1 <= 2X7, 2 + 3X7, 3 + 4X7

✓ **Correct** 1/1 Points

8. The correct/conventional order of steps in HLS are

- Scheduling, datapath and controller generation, Preprocessing, allocation and binding
- Preprocessing, allocation and binding, scheduling, datapath and controller generation
- Preprocessing, allocation and binding, scheduling, datapath and controller generation
- Preprocessing, scheduling, allocation and binding, datapath and controller generation

✓ **Correct** 2/2 Points

9. **(Figure 3)** The start time of node 7 by HU's algorithm is (Assume that in case of conflict we smaller label node is given more priority)

3

✓ **Correct** 2/2 Points

10. **(Figure 1)**What is the **Operation *interval*** of operation 9?

- (a) 3
- (d) 1
- (c) 4
- (b) 2

✗ **Incorrect** 0/2 Points

11. **(Figure 2)**Determine the correct inequality representing the **resource constraint** at time step 2 for MUL

- (b) X2, 2 + X4, 2 + X5, 2 <= 3
- (c) X2, 2 + X4, 2 + X5, 2 + X7, 2 <= 3
- (d) X2, 2 + X4, 2 + X5, 2 + X7, 2 + X10, 2 <= 3
- (a) X7, 2 <= 3

✗ **Incorrect** 0/2 Points

12. **(Figure 2) Constraint** for the unique start time of operation 5 is

- (c) X5,1 + X5,2 + X5,3 + X5,4 + X5,5=1
- (d) X5,1 + X5,2 + X5,3 + X5,4 + X5,5 + X5,6=1
- (a) X5,1+ X5,2 + X5,3=1
- (b) X5,1 + X5,2 + X5,3+ X5,4=1

✗ **Incorrect** 0/1 Points

13. What are the constraints must be satisfied on a sequence graph so that scheduling becomes polynomial time solvable? (more than one correct answer, no partial marking)

- [x] (ii) All operations have unit delay
- [x] (iii) There is a unique path between any two nodes in the sequence graph
- [ ] (iv) Operations are allowed to be multi-cycle.
- [x] (i) All operations are of the same type.

✗ **Incorrect** 0/3 Points

14. **(Figure 1)** The self-force for operation 3 on assigning it to time step 2 is (select the nearest option)

- (a) 0.165
- (c) 0.450
- (b) -0.165
- (d) -0.450

✗ **Incorrect** 0/2 Points

15. **(Figure 2)**Determine the correct inequality representing the **dependency constraint** between operations 1 and 6

- (c) X3,1 + 2X3, 2 + 3X3, 3 + 1 <= 2X7, 2 + 3X7, 3
- (b) X3,1 + 2X3, 2 + 1 <= 2X7, 2 + 3X7, 3 + 4X7, 4
- (d) X3,1 + 2X3, 2 + 1 <= 2X7, 2 + 3X7, 3
- (a) X3,1 + 2X3, 2 + 3X3, 3 + 1 <= 2X7, 2 + 3X7, 3 + 4X7, 4

✗ **Incorrect** 0/2 Points

16. **(Figure 1)** How many numbers of ALU and MUL are required for this MRLC schedule using forced directed schedule

- (b) 1, 2
- (a) 2, 1
- (c) 2, 2
- (d) 1, 3

✓ **Correct** 1/1 Points

17. Which of the following are TRUE?

S1: The general purpose processor is much faster that application specific hardware accelerator.

S2: HLS can be used to develop hardware accelerator from C/C++ specification.

- (c) S1: TRUE, S2: FALSE
- (d) S1: FALSE, S2: FALSE
- (b) S1: FALSE, S2: TRUE
- (a) S1: TRUE, S2: TRUE

✗ **Incorrect** 0/3 Points

18. **(Figure 1)** The value of MUL resource type distribution at time step 2 is (select the nearest option)

- (c) 2
- (b) 1.67
- (a) 1.33
- (d) 2.33

✓ **Correct** 1/1 Points

19. Which of the following advantages High-level Synthesis (HLS) provide for VLSI Designers?

A1: Easy Design space exploration

A2: Design Cycle is shortened

A3: Optimize an RTL design

- (d) Only A1
- (a) Only A1 and A2
- (c) Only A2 and A3
- (b) Only A1 and A3

✗ **Incorrect** 0/3 Points

20. **(Figure 1)** The assignment of operation 5 to time step 4 implies that the assignment of operation 10 to time step 5. Therefore, the successor force is (select the nearest option)

- (b) -0.83
- (d) -0.5
- (c) 0.5
- (a) 0.83