C-Based VLSI Design
End Semester Examination

Date: 10th May 2022 **Duration: 3 Hours** **Total Marks: 100**

Answer All Questions

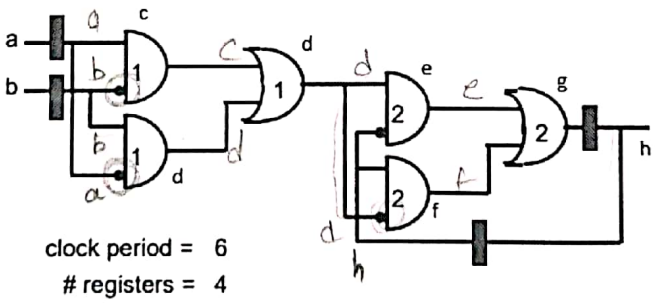
Q1: Consider the following behavior. **[6 + 6 + 6 + 6 + 10 + 6 = 40]**

```
m1 = in1 * in2;
m2 = in1 * 10;
m3 = in3 * 16;
m4 = in4 * in5;
m5 = in2 * in3;
a1 = m2 * in2;
a2 = m4 * 15;
a3 = m1 + a1;
a4 = a2 + m3;
a5 = a4 + m5;
```

Answer the following questions on High-level Synthesis. You do not need to follow any specific algorithm for the below tasks. Draw only a clear diagram for each step. No need to add explanation.

a) Draw the Sequence graph of the behavior.
b) Assume all operations are single cycle and there are three Multipliers and two Adders are available. You have to schedule the behavior in 4 cycles. Show the scheduled behavior.
c) Assume that you have to map only variables with name "m" and "a" to registers. You do not need to map the inputs "in" and constants to registers. Show the lifetimes of the variables and variable to register mapping with minimum of registers.
d) Show the functional unit (FU) mapping. You have MULT and ADD FUs in the hardware. The multiplication and addition operations are to be mapped to MULT and ADD, respectively.
e) Draw a Multiplexer based datapath based on your allocation and binding information.
f) Identify the minimum control signals required to control the datapath. Identify the control signal values at each time step of the controller.

Q2: Consider the following circuit. The number inside a logic gate is the delay of that gate. The registers are shown as rectangular block. The circuit achieves clock period 6 using 4 registers. Draw the retimed circuit that achieves target clock period 2.



To obtain the retimed circuit that achieve the clock period 2 from the original circuit, what would be the value of r(v) for each node v? Recall r(v) for node v represents the number of register moved from the output side to the input side of node v. **[5 + 10 = 15]**

Q3: Consider the following loop. Draw the abstract data path for (i) *the rolled implementation* and *(ii) the pipelined implementation of* the loop. Operation chaining is not allowed. Use minimum resource in both the implementation. **[7 + 8 = 15]**

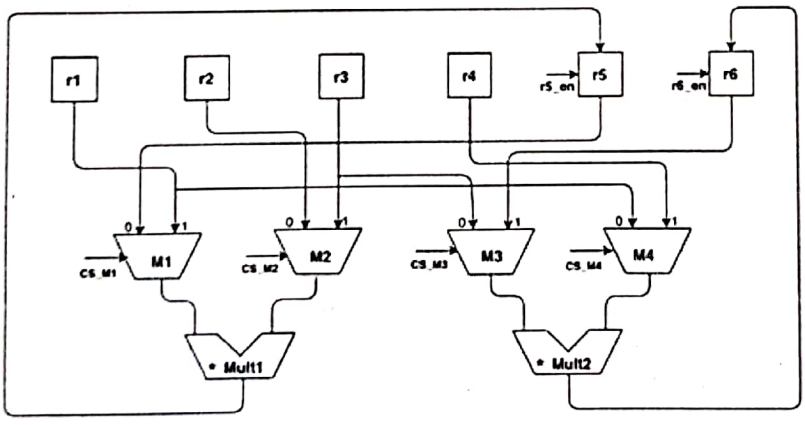
```
void fn(int a[100], int b[100], int c[100], int d[100], int &Y)
  {
      int i;
      for (i = 0; i < 100; i++)
           Y[i] = a[i] + b[i] + c[i] + d[i];

  }
```

Q4: Consider the following behavior. Let us assume that the width of the Integer is 32 bits. **[5 + 5 = 10]**

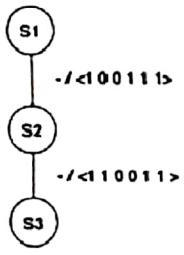
```
int A1[1000], A2[500];
for (i = 1 to 1000)
{
      A1[i] = value1;
      if (i<500)
            A2[i] = value2;
}
```

a) How can you rewrite the code so that the arrays can be mapped to *one dual port RAM* of size 2000 x 40? (i.e., there are 2000 locations and each location can store 40 bits).
b) How the arrays can be mapped to *one single port RAM* of size 1000 x 70?

Q5: The RTL generated by high-level synthesis which consists of data-path and the controller FSM is shown below. The order of the control signal in control assignment is < cs_M1, cs_M2, cs_M3, cs_M4, r5_en, r6_en >. Assume that the enable of other registers is always 0. Using the RTL to C reverse engineering approach, construct the finite state machine with data-path from this RTL behavior. **[10]**



(a) Datapath



(b) Controller FSM

Q6: Write short note on any TWO of the following topic. **[5 + 5 = 10]**

a) Logic Locking in High-level Synthesis
b) Data-flow optimization in High-level Synthesis
c) Logic Synthesis
d) Physical Synthesis