Week 6: Assignment 6

The due date for submitting this assignment has passed.

Due on 2021-09-08, 23:59 IST.

As per our records you have not submitted this assignment.

1) Which of the following statement(s) is/are correct in register allocation and binding? *1 point*

S1: conflict graph is always an interval graph for non-hierarchical sequential graph

S2: conflict graph is always an interval graph for hierarchical sequential graph

- Only S1
- Only S2
- Both S1 and S2
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Only S1

2) Circular-arc conflict graph is used for *1 point*

- If-else
- Function calls
- Loops
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Loops

3) Consider the below scheduling behaviour. *2 points*

Time – step 1: $v_3 = v_1 + v_2$; $v_{12} = v_1$
Time – step 2: $v_5 = v_3 + v_4$; $v_7 = v_3 * v_6$; $v_{13} = v_3$
Time – step 3: $v_8 = v_3 + v_5$; $v_9 = v_1 + v_7$; $v_{11} = v_{10} / v_5$
Consider we are binding the variables to register file. Assume there is only one port is available for memory binding. We want to map a subset of variables to that register file such that there won't be any access conflict. Which of the following mapping is correct?

- v_2, v_5, v_9
- v_1, v_3, v_8
- v_2, v_4, v_8
- v_{10}, v_{11}, v_{12}

No, the answer is incorrect.
Score: 0

Accepted Answers:
v_2, v_4, v_8

4) Which of the following shows the correct register mapping for the live variable analysis graph in Figure 1? *1 point*

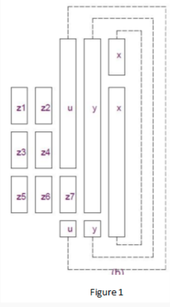

Figure 1

- R1: z1, z2, z5
  R2: z3, z4, z6
  R3: u, z7
  R4: y, x
- R1: z1, z3, u
  R2: z2, z4, z7
  R3: z5, z6
  R4: y, x
- R1: z1, z3, z5
  R2: z2, z4, z6
  R3: u, y
  R4: z7
  R5: x
- R1: z1, z3, z5
  R2: z2, z4, z6
  R3: u, z7
  R4: y
  R5: x

No, the answer is incorrect.
Score: 0

Accepted Answers:
R1: z1, z3, z5
R2: z2, z4, z6
R3: u, z7
R4: y
R5: x

5) Consider the data path in Figure 2. *1 point*

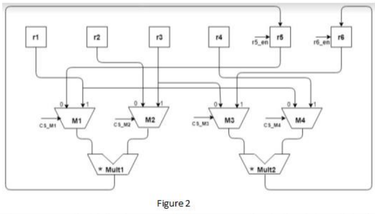

Figure 2

Let us assume that following operations are executing in the data path in time step S1.

r5 = r1 <Mult1> r2
r6 = r3 <Mult2> r4

what would be the control assertion pattern for the operations in time step S1, if the control assertion pattern order is (CS_M1, CS_M2, CS_M3, CS_M4, r5_en, r6_en)?

- (1, 0, 0, 0, 0, 0)
- (1, 0, 0, 1, 1, 1)
- (1, 0, 0, 1, 1, 0)
- (0, 1, 1, 0, 1, 1)

No, the answer is incorrect.
Score: 0

Accepted Answers:
(1, 0, 0, 1, 1, 1)

6) Considering the datapath in Figure 2 again, what would be the operations executed in the datapath, if the control signal assignment is (1, 1, 0, 0, 1, 1), where the order of control signals is CS_M1, CS_M2, CS_M3, CS_M4, r5_en, r6_en)? *2 points*

- r5 = r1 <Mult1> r2 and r6 = r3 <Mult2> r4
- r5 = r5 <Mult1> r3 and r6 = r1 <Mult2> r2
- r5 = r1 <Mult1> r3 and r6 = r3 <Mult2> r1
- r5 = r5 <Mult1> r2 and r6 = r1 <Mult2> r2

No, the answer is incorrect.
Score: 0

Accepted Answers:
r5 = r1 <Mult1> r3 and r6 = r3 <Mult2> r1

7) Which of the following statements are true? *1 point*

S1: Two registers can share a register if their respective lifetimes overlap.

S2: In the conflict graph obtained from lifetimes of variables, two variables can be mapped to the same register if the corresponding nodes have the same colour.

- ONLY S1 is TRUE
- ONLY S2 is TRUE
- BOTH S1 and S2 are True
- BOTH S1 and S2 are False

No, the answer is incorrect.
Score: 0

Accepted Answers:
ONLY S2 is TRUE

8) Conflict graph is an interval graph for non-hierarchical sequence graph and it is Polynomial time solvable by Left-edge algorithm. The above statement is *1 point*

- True
- False

No, the answer is incorrect.
Score: 0

Accepted Answers:
True