CS 577: C-Based VLSI Design

Announcements:

- Guest Lecture on Post Quantum Cryptography by Deepraj Soni on 27th January 2023, 7PM.
- Guest Lecture on HLS for Security by Prof. Ramesh Karri on 7th February 2023, 12PM.
- Welcome to CS 577 Course page
- **The Class will strat from 6th January 2023 (Friday) in 5G4**
- IMPORTANT: Any malpractice will lead to F grade without any explanation.

Instructors

- Dr. Chandan Karfa

Cource Overview

- High-level Synthesis (HLS) is the process of generating effecient hardware at register transfer level (RTL) from the input C-code (high-level code). HLS is an active domain of research in recent times in the domain of electronic Design Automation (EDA) of VLSI. This course will help the students to understand
  - the overall C to RTL synthesis flow,
  - how a C-code will be converted to its equivalent hardware,
  - how to write C-code for efficient hardware generation,
  - how the common software compiler optimizations can help to improve the circuit performance.
  - Hardware Acceleration of Machine Learning Algorithm
  - Secure Hardware generation using HLS
  - Equivalence checking between C and RTL.
  - The overall EDA tool flow.
- This course will help the students to take up research in the domain of HLS. Also, this course will help the students to become proficient for EDA industries.
- **Pre-requisites:** (1) Basic knowledge of digital circuits (2) Basic knowledge of Data structures and algorithms

Class Timing and Venue:

- Slot F in timetable for Open Electives
- **Friday**: 11AM-12PM, **Monday**: 12PM-1PM, **Tuesday**: 12AM-1PM
- **Venue**: 5G4, Class Room Complex

- **Mode of Lecture:** Live Class

Teaching Assistants:

- Praveen Karmakar - pkarmakar@iitg.ac.in
- Nilotpola Sarma - s.nilotpola@iitg.ac.in
- Rittick Mondal - rittickmondal@iitg.ac.in
- Divyanshu Nauni Divyanshu_nauni@iitg.ac.in

Syllabus:

- Electronic Design Automation flow: Overview of high-level synthesis, logic synthesis and physical synthesis;
- High-level Synthesis (HLS) Fundamentals: Overview HLS flow, Scheduling Techniques, Resource sharing and Binding Techniques, Datapath and Controller Generation Techniques;
- Impact of C-coding style on Hardware: Data types, Synthesis of Loops, Functions, RAM, ROM, Shift register inference from arrays;
- Impact of Compiler Optimization in HLS results: Impact of Compiler optimizations like copy propagation, constant propagation, common sub-expression elimination, loop transformations, code motions, etc., in HLS results;
- HLS for Security: RTL Locking, Logic Locking, Attack and Defense techniques;
- RTL Optimizations Techniques: Various optimization techniques to improve latency, area and power in C-based VLSI designs;
- High-level Synthesis Verification: BDD, Simulation based verification, Equivalence checking between C and RTL;
- Hardware acceleration of Machine Learning Algorithms
- Domain Specific High-level Synthesis

Text Book:

- `[Micheli]` G. De Micheli. Synthesis and optimization of digital circuits, McGraw Hill, India Edition, 2003.
- `[Elliot]` J. P. Elliot, Understanding Behavioural Synthesis: A Practical guide to High-level Synthesis, Springer, 2nd edition, 2000
- `[Kilts]` Steve Kilts, Advanced FPGA Design, Wiley, 2007.
- `[Parhi]` K. Parhi: VLSI Digital Signal Processing Systems: Design and Implementation, Jan 1999, Wiley.
- `[Huth]` M. Huth and M. Ryan, Logic in Computer Science: Modelling and Reasoning about Systems, 2nd Ed, Cambridge University Press, 2004.
- Various Research Papers.

References:

- `[Gajski]` D. D. Gajski, N. D. Dutt, A.C.-H. Wu and S.Y.-L. Lin, High-Level Synthesis: Introduction to Chip and System Design, Springer, 1st edition, 1992

- [BlueBook] Mike Fingeroff, High-Level Synthesis Blue Book, Mentor Graphics Corporation, 2010.
- Ryan Kastner, Janarbek Matai, and Stephen Neuendorffer, Parallel Programming for FPGAs, 2018.
- Philippe Coussy and Adam Morawiec, High-level Synthesis from Algorithm to Digital Circuit, Springer, 2008
- David. C. Ku and G. De Micheli, High-level Syntehsis of ASICs Under Timing and Synchronization Constraints, Kluwer Academic Publishers, 1992.
- T. F. Melham, Higher Order Logic and Hardware Verification, Cambridge University Press, 1993.

Grade Calculation

- Class Participation: 10%
- MidSem: 20%
- End Sem: 40%
- Project: 30%. A group of 4/5 students to be assigned to a project.

Classes

Lecture No	Date	Topic	Resources
1.	6th Jan 2023	Introduction to C-Based VLSI Design	Class notes
2.	9th Jan 2023	C to RTL with examples	Class notes
3.	10th Jan 2023	C to RTL with examples	Class notes
4.	13th Jan 2023	Introduction to HLS steps with example	Class notes
5.	16th Jan 2023	Introdution to HLS steps with example	Class notes
6.	17th Jan 2023	Vivado HLS tool Demo	
7.	23rd Jan 2023	Functional Pipelining in HLS	Class notes
8.	24th Jan 2023	Loop Pipeline in HLS	Class notes
9.	27th Jan 2023	HLS for Array	Class notes
10.	27th Jan 2023	Guest Lecture on Post Quantum Cryptography by Deepraj Soni	
11.	30th Jan 2023	HLS for Array, Unsuported Construct	Class notes

12.	31st Jan 2023	HLS Coding Style: Data type, nested loop, Array at Interface, Function	Class notes
13.	7th Feb 2023	Guest Lecture on HLS for Security by Prof. Ramesh Karri	
14.	13th Feb 2023	Scheduling Problem Formulation	Micheli: Ch. 5
15.	14th Feb 2023	Scheduling: ASAP, ALAP	Micheli: Ch. 5
16.	17th Feb 2023	ILP Formulation of Scheduling	Micheli: Ch. 5
17.	20th Feb 2023	Multiprocessor Scheduling	Micheli: Ch. 5
18.	21st Feb 2023	Multiprocessor Scheduling: HUs' Algorithm	Micheli: Ch. 5
19.	22nd Feb 2023	List Scheduling: MLRC and MRLC	Micheli: Ch. 5
20.	24th Feb 2023	Forced Directed Scheduling	Micheli: Ch. 5
21.	13th March 2023	Forced Directed Scheduling – ML-RC	Micheli: Ch. 5
22.	14th March 2023	Forced Directed Scheduling – MR-LC	Micheli: Ch. 5
23.	17th March 2023	Logic Locking Introduction	Paper shared in teams
24.	20th March 2023	RTL Logic Locking	Paper shared in teams
25.	21st March 2023	RLL, FLL, SLL	Paper shared in teams
26.	24th March 2023	SAT Attack	Paper shared in teams
27.	27th March 2023	SarLock, Anti-SAT, AND-Tree, Cycle Lock	Paper shared in teams
28.	28th March 2023	Sequential Locking	Paper shared in teams
29.	31st March 2023	FU Allocation and Binding	Micheli: Ch 6
30.	3rd April 2023	Left-Edge Algorithm, Complexity of Allocation and Binding	Micheli: Ch 6
31.	10th April 2023	Register Allocation and Binding	Micheli: Ch 6
32.	11th April 2023	Data path and Controller Optimizations	Micheli: Ch 6, Class notes
33.	17th April 2023	Data path and Controller Optimizations, Datapath and Controlelr Optmizations	Micheli: Ch 6, Class Notes

34.	18th April 2023	Front-end Optimizations	Class Notes
35.	21st April 2023	Guest Lecture on Formal Verification by Disha Puri	
36.	24th April 2023	RTL to C reverse Engineering	Class Notes, Paper shared
37.	24th April 2023	C to RTL Equivalence Checking	Class Notes, Paper shared
38.	28th April 2023	BDD, OBDD to ROBDD	Micheli: Ch 2.5
39.	1st May 2023	Direct ROBDD Construction of a function	Micheli: Ch 2.5
40	2nd May 2023	Introduction to Logic Synthesis	Video Link
41.	3rd May 2023	Introduction to Physical Synthesis	Video Link

Evaluation Schedule