CS577: C-Based VLSI Design

Read the Instructions and copy it to your notebook before starting the examination.

Instructions and Figure 1:

Each MUL (performs multiplication operation) and ALU (performs rest operations) operation **takes one unit of time (i.e., single cycle). The latency bound λ = 5.** Please note that the dummy operations 0 and n do not take any time step. Operations 1 to 11 will be scheduled during time steps 1 to 5. Answer the questions marked with Figure 1 in the Paper 1.

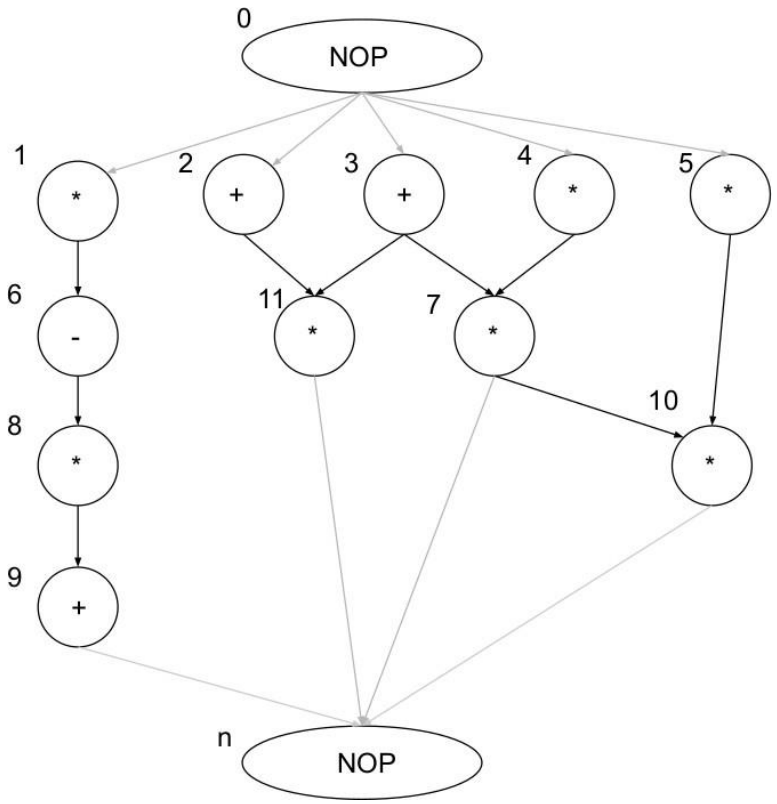

Figure 1: Sequence Graph for Questions marked with [Figure 1] in Paper 1

Instructions and Figure 2

Let $X_{i,j}$ = 1 represents the assignment of operation i to the time step j. **Latency bound is 7** and there are 3 MUL and 1 ALU available. Answer the following questions in Paper 1 marked with Figure 2. Consider **Multiplication is TWO** cycle and ALU operations are single cycle operation.

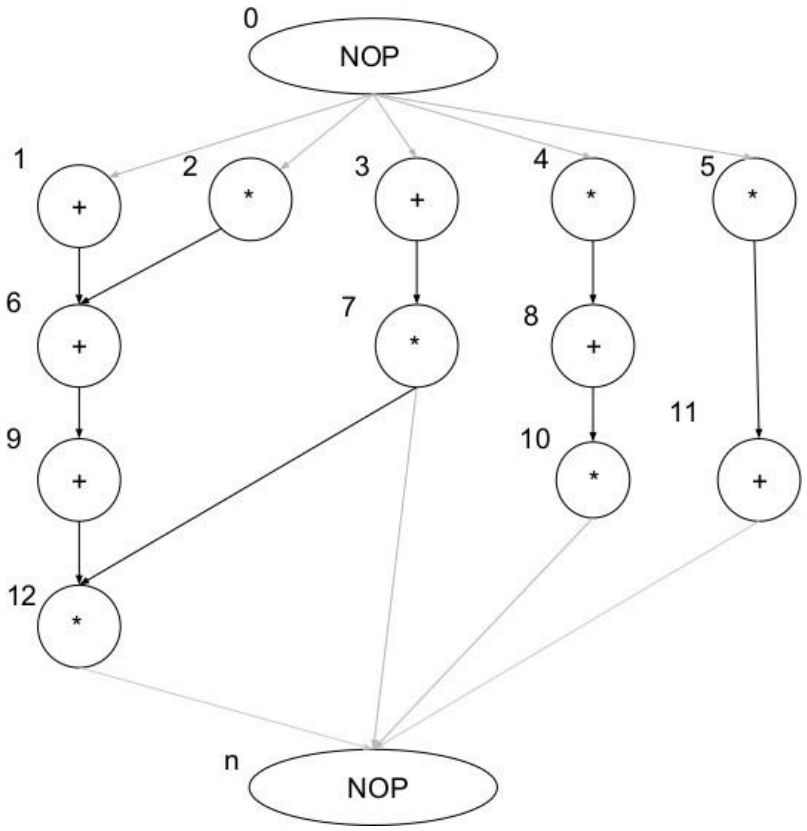

Figure 2: Sequence Graph for Questions marked with [Figure 2] in Paper 1

Instructions and Figure 3:

Let us assume that all operations can be executed using a same type of resource (i.e., multiprocessor scheduling) for the below sequence graph. Consider the Hu's algorithm for the same.

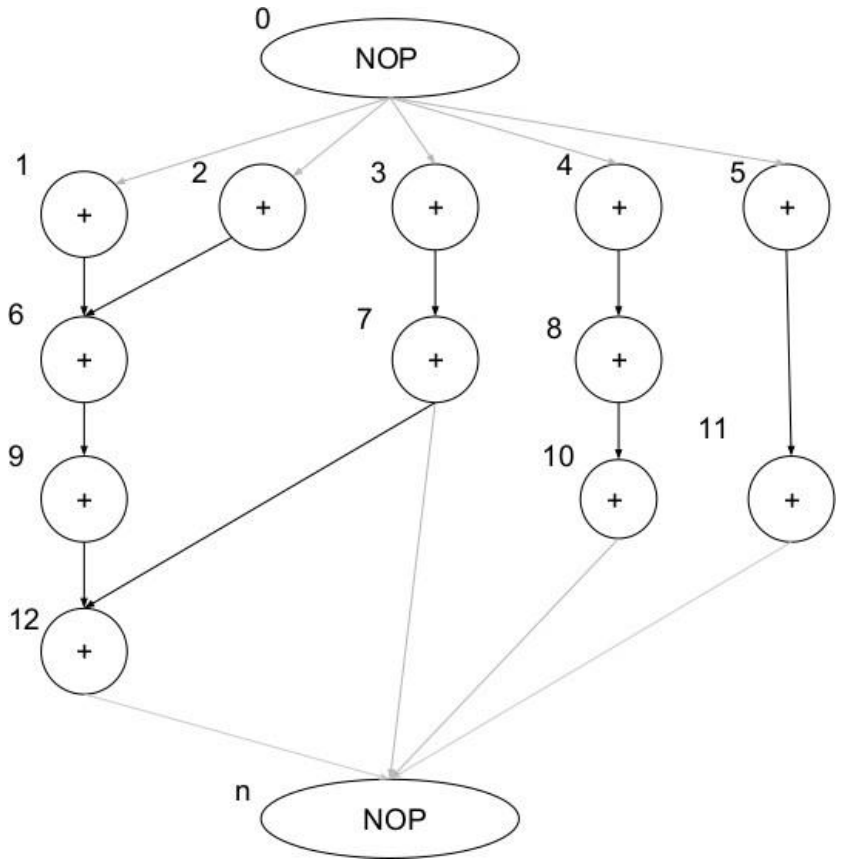

Figure 3: Sequence Graph for Questions marked with [Figure 3] in Paper 1