NPTEL » C-Based VLSI Design

## Course outline

How does an NPTEL online course work?

Prerequisite: Week 0

Week1: Introduction to Cbased VLSI Design

Week2: C-Based VLSI Design: Basic Scheduling

Week3: C-Based VLSI Design: List Based Scheduling

- Lec 1: Multiprocessor
- Scheduling

Lecture Note for Lec1

- Lec 2: Hu's algorithm for
- Lecture Note for Lec2
- Lec 3: List based Scheduling of MLRC

Multiprocessor Scheduling

Lecture Note for Lec3

Lecture Note for Lec4

- Lec 4: List based Scheduling of MRLC
- Quiz: Week 3: Assignment 3
- Week 3: Feedback form

Solution: Assignment 3

Week 4: C-Based VLSI

Design: Advanced Scheduling

Week 5: C-Based VLSI Design: Allocation and Binding

Week 6: C-Based VLSI Design: Allocation, Binding, Data-path and Controller Generation

Week 7: C-Based VLSI Design: Efficient Synthesis of C Code

Week 8: C-Based VLSI Design: Hardware Efficient C

Week 9: C-Based VLSI Design: Impact of Compiler Optimizations in Hardware

Week 10: Verification of Highlevel Synthesis

Week 11: Securing Design with High-level Synthesis

Week 12: Introduction to EDA and Recent Advances in C-Based VLSI Design

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## Week 3: Assignment 3

The due date for submitting this assignment has passed.

As per our records you have not submitted this assignment.

Due on 2021-08-25, 23:59 IST.

Consider the Sequential Graph shown in the figure below. Each MUL operation takes two-unit times, and ALU takes one unit of time. Given three MUL and one ALU, determine the minimum latency resource-constrained (MLRC) LIST-schedule and answer the following questions from 1 to 8?

```
LIST \mathcal{L}(G_s(V, E), \mathbf{a}) {
l = 1;
repeat {
        for each resource type k = 1, 2, ..., n_{res} {
                Determine candidate operations U_{l,k};
                Determine unfinished operations T_{l,k};
                Select S_k \subseteq U_{l,k} vertices, such that |S_k| + |T_{l,k}| \le a_k;
                Schedule the S_k operations at step l by setting t_i = l \ \forall i : v_i \in S_k;
        l = l + 1;
until (v_n is scheduled);
return (t);
```



1) Which one is the last operation to be scheduled by the MLRC schedule?

Only 9

Only 10 Either 8 or 10

No, the answer is incorrect.

Accepted Answers:

Either 8 or 10

2) The start time of operations 3 and 4 are

01,2 2, 2

01,1

2, 1

Score: 0

No, the answer is incorrect.

Accepted Answers:

1, 1

3) The latency of this MLRC schedule is

6 07

08

9

No, the answer is incorrect.

Score: 0

Accepted Answers:

4) Number of ALU (+) operation/s in time step 4 is

0  $\bigcirc$  1

02

None of the above

No, the answer is incorrect. Score: 0

Accepted Answers:

5) Number of MUL(\*) operation/s in time step 3 is

01

O 2

3

No, the answer is incorrect.

Accepted Answers:

Score: 0

6) The ALAP time of operation 8 is

8

07 **6** 

05

No, the answer is incorrect. Score: 0

Accepted Answers:

7) The ASAP time of operation 2 is

04 3

02 01

No, the answer is incorrect. Score: 0

Accepted Answers:

8) Time step 7 contains which operation

Only MUL Only ALU

O Both MUL and ALU None of the above

No, the answer is incorrect. Score: 0

Accepted Answers: Only ALU

2 points 1 point 0 points 1 point 1 point

0 points

1 point

1 point