Course outline

How does an NPTEL online course work?

Prerequisite: Week 0

Week1: Introduction to C-based VLSI Design

- Lec 1: Introduction to C-Based VLSI Design
- Lecture Notes for Lec1
- Lec 2: C-based VLSI Design: An Overview
- Lecture Notes for Lec2
- Lec 3: C-based VLSI Design: Problem Formulation
- Lecture Notes for Lec3
- Lec 4: C-based VLSI Design: Course Plan
- Lecture Notes for Lec4
- Quiz: Week 1: Assignment 1
- Week 1: Feedback form
- Week1 Assignment1 Solution

Week2: C-Based VLSI Design: Basic Scheduling

Week3: C-Based VLSI Design: List Based Scheduling

Week 4: C-Based VLSI Design: Advanced Scheduling

Week 5: C-Based VLSI Design: Allocation and Binding

Week 6: C-Based VLSI Design: Allocation, Binding, Data-path and Controller Generation

Week 7: C-Based VLSI Design: Efficient Synthesis of C Code

Week 8: C-Based VLSI Design: Hardware Efficient C Coding

Week 9: C-Based VLSI Design: Impact of Compiler Optimizations in Hardware

Week 10: Verification of High-level Synthesis

Week 11: Securing Design with High-level Synthesis

Week 12: Introduction to EDA and Recent Advances in C-Based VLSI Design

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Live Sessions

Week 1: Assignment 1

The due date for submitting this assignment has passed.

Due on 2021-08-18, 23:59 IST.

As per our records you have not submitted this assignment.

1) Which one of the following statement is correct? *1 point*

S1: Integrated circuits (ICs) which consists of millions of transistors are built using electronic design automation (EDA) tools

S2: High-level Synthesis (HLS) translates an untimed high-level behaviour into Register-transfer level (RTL)

- Only S1
- Only S2
- Both S1 and S2
- None of S1 and S2

No, the answer is incorrect.
Score: 0
Accepted Answers:
Both S1 and S2

2) Which of the following advantages High-level Synthesis (HLS) provide in VLSI Designers? *1 point*
A1: Easy Design space exploration
A2: Shorter Design Cycle
A3: Optimize an RTL design

- Only A1 and A2
- Only A1 and A3
- Only A2 and A3
- Only A1

No, the answer is incorrect.
Score: 0
Accepted Answers:
Only A1 and A2

3) The sub-steps of HLS are *1 point*

- Preprocessing, allocation and binding, scheduling, datapath and controller generation
- Scheduling, datapath and controller generation, Preprocessing, allocation and binding
- Preprocessing, allocation and binding, scheduling, datapath and controller generation
- Preprocessing, scheduling, allocation and binding, datapath and controller generation

No, the answer is incorrect.
Score: 0
Accepted Answers:
Preprocessing, scheduling, allocation and binding, datapath and controller generation

4) In HLS the identification of basic blocks and data dependencies among operations are identified at *1 point*

- Scheduling phase
- Allocation phase
- Preprocessing phase
- Controller design phase

No, the answer is incorrect.
Score: 0
Accepted Answers:
Preprocessing phase

5) The operations of the input behaviour are assigned a time step during HLS during *1 point*

- Preprocessing
- Scheduling
- Allocation and binding
- Datapath and controller generation

No, the answer is incorrect.
Score: 0
Accepted Answers:
Scheduling

6) Which is of the following are correct mapping between C constructs and RTL Constructs during HLS *1 point*

C Constructs	RTL Constructs
(a) Array	1. RAM/ROM
(b) Variable	2. Ports
(c) Function	3. Register
(d) Function Arguments	4. Module

- a-->1, b-->3, c-->4, d-->2
- a-->3, b-->1, c-->2, d-->4
- a-->1, b-->2, c-->3, d-->4
- a-->3, b-->1, c-->4, d-->2

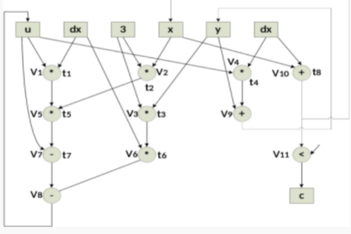
No, the answer is incorrect.
Score: 0
Accepted Answers:
a-->1, b-->3, c-->4, d-->2

7) Hardware accelerator brings following advantages *1 point*
A1: Speed up critical task
A2: Reduce power consumption and cost
A3: Increase energy efficiency

- Only A1
- Only A2 and A3
- Only A1 and A2
- All of A1, A2 and A3

No, the answer is incorrect.
Score: 0
Accepted Answers:
All of A1, A2 and A3

8) Consider the following behaviour given as direct acyclic graph (DAG). Here each node represents an operation and the edge between two nodes represents the data dependency. Let the operations are scheduled in four time steps: 1, 2, 3 and 4. Which one of the following is a part of a valid schedule of the operations? *1 point*



- Operations V1, V5, V7, V8 are scheduled in time step 1
- Operations V1, V5, V2, V4 are scheduled in time step 1
- Operations V1, V2, V3, V10 are scheduled in time step 1
- Operations V1, V3, V8, V10 are scheduled in time step 1

No, the answer is incorrect.
Score: 0
Accepted Answers:
Operations V1, V2, V3, V10 are scheduled in time step 1

9) The full form of VLSI is *1 point*

- Very Large Scope Integration
- Very Long Scale Integration
- Very Long Scale Integer
- Very Large Scale Integration

No, the answer is incorrect.
Score: 0
Accepted Answers:
Very Large Scale Integration

10) Which one of the following statements are correct? *1 point*

S1: C is an untimed behaviour
S2: C is a timed behaviour
S3: In RTL, operations scheduled in a time step will execute sequential manner.
S4: In RTL, operations scheduled in a time step will execute in parallel.

- S1 and S3
- S1 and S4
- S2 and S3
- S2 and S4

No, the answer is incorrect.
Score: 0
Accepted Answers:
S1 and S4