

Suppose
 L → input skew is 60ps
 and op load is 50fF
 then
 y_{15} is the delay of a cell

Suppose

↳ input skew is 60ps
and OIP load is 50fF
then

\downarrow
 y_{IS} is the delay of a cell

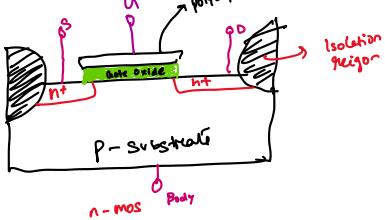
Delay

Where does this table come from?

From Spice simulation
We have learnt about delay models \Rightarrow accuracy of these models

NMOS

↳ n-channel on p-substrate



Threshold Voltage (V_t) =

+ $V_{GS} = 0$

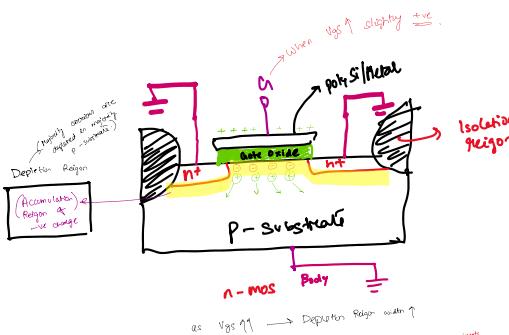
* Drain, Source, Bulk \rightarrow GND

* Substrate Source (BS) \times Substrate Drain (BD) form p-n junction diode

* Both junc. are "off" due to 0V bias

* Hence, S-D resistance is "high"

* Apply +ve V_{GS} Voltage.

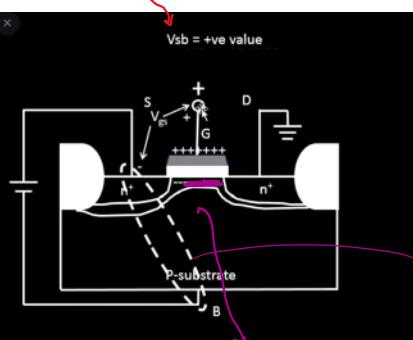
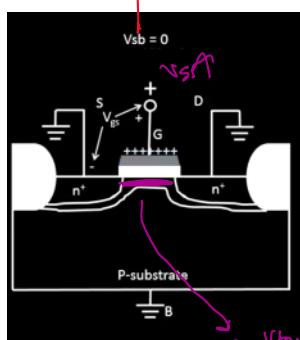


(Point of inversion \rightarrow Threshold Voltage)

Threshold Voltage

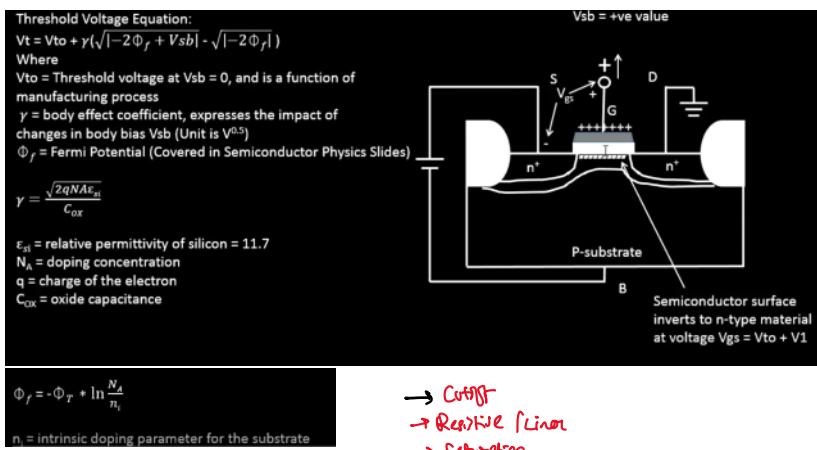
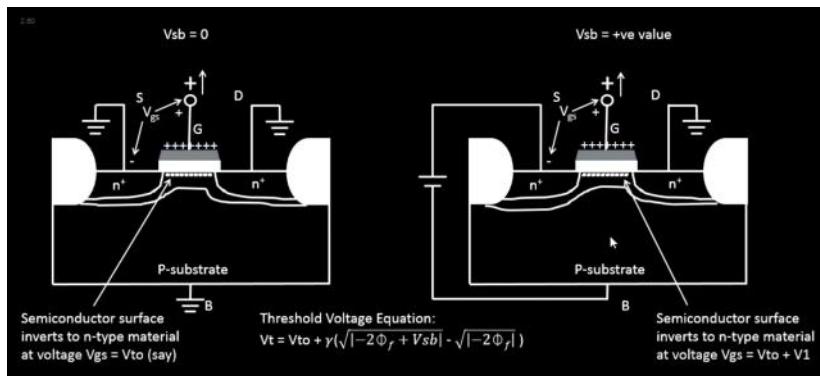
- $V_{GS} = 0$
- Drain, Source, Bulk connected to GND
- Substrate-Source (B-S) and Substrate-Drain (B-D) form p-n junction diode
- Both junctions are 'off' due to 0V bias
- Hence, S-D resistance is 'high'
- Apply +ve V_{GS} voltage
- Increase gate voltage ' V_{GS} '
- This phenomenon is called 'strong inversion'
- The ' V_{GS} ' voltage at which 'strong inversion' occurs is called *threshold voltage* (V_t)
- Further, increase ' V_{GS} '
- No Change in depletion layer width
- Electrons from heavily doped 'n+' source region are drawn in region under gate 'G'
- Continuous n-channel formation from S-D, whose conductivity is modulated by ' V_{GS} '

TWO scenarios \rightarrow
case 1: $B=0$ case 2: $B \neq 0$



Due to +ve V_{SB} , few charges from channel are pulled towards source 'S'.

Additional Reverse bias between source 'S' and substrate (or Bulk) 'B'
Therefore, depletion layer width is slightly high near 'S'
Increase ' V_{GS} '



Resistive Operation / Linear Region

Resistive Operation

- Since, $V_{gs} = V_t$, let us observe what happens at different voltages of ' $V_{gs} > V_t$ '

$$V_{gs} > V_t$$

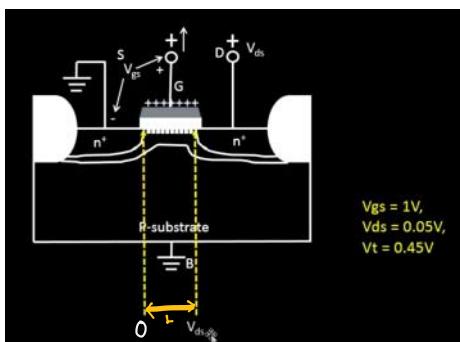
as $V_{gs} - V_t \uparrow \rightarrow$ the induced charge in accumulation channel increases

Turn on voltage $\rightarrow V_{gs} - V_t$.

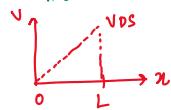
Suppose we apply now little bit of drain to source (V_{ds}) voltage

$V_{ds} < V_{gs} - V_{th}$ \rightarrow Linear region

$0.05V \quad 1V \quad 45V$ \therefore Suppose CASE 1

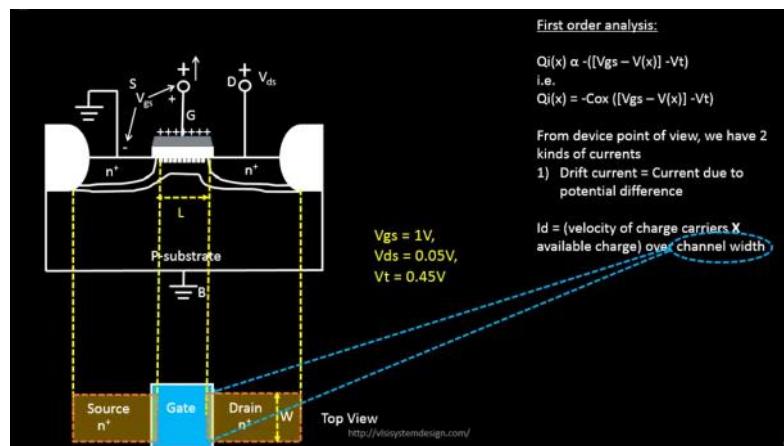


there will be a voltage gradient



$V_{gs} - V(x) \rightarrow$ Gate to channel voltage at that point.

$$Q_s(x) \propto -[(V_{gs} - V(x)) - V_t] \quad \text{induced charge in channel.}$$



$$Q_i(x) \propto -[(V_{gs} - V(x)) - V_t] \quad \text{induced charge in channel.}$$

$$Q_i(x) = -C_{ox} ([V_{gs} - V(x)] - V_t)$$

Gate oxide capacitance

From device point of view, 2 currents

- (i) Drift current \rightarrow Current due to potential difference
- (ii) Diffusion current \rightarrow Current due to difference in carrier conc.

$$I_d \rightarrow (\text{velocity of charge} \times \text{Available charge}) \frac{\text{over channel width}}{\text{channel width}}$$

$$I_d = -\underbrace{v_n(x)}_{\mu_n \frac{dv}{dx}} \times Q_i(x) \times W$$

mobility \times E.F.
 $\mu_n \frac{dv}{dx}$

$$I_d = -(\mu_n \frac{dv}{dx}) \times (-C_{ox} (V_{gs} - V(x) - V_t)) \cdot W$$

$$\int_0^L I_d \cdot dx = \int_0^L \mu_n \times C_{ox} (V_{gs} - V(x) - V_t) \cdot dV$$

$dV \rightarrow 0 \text{ to } V_{ds}$
 $dx \rightarrow 0 \text{ to } L$

On integration we get:

$$I_{ds} = \frac{\mu_n C_{ox} W}{L} \left[(V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

Technological constraint.

$K_n^1 \rightarrow$ process transconductance

$$I_{ds} = K_n^1 \frac{W}{L} \left[(V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

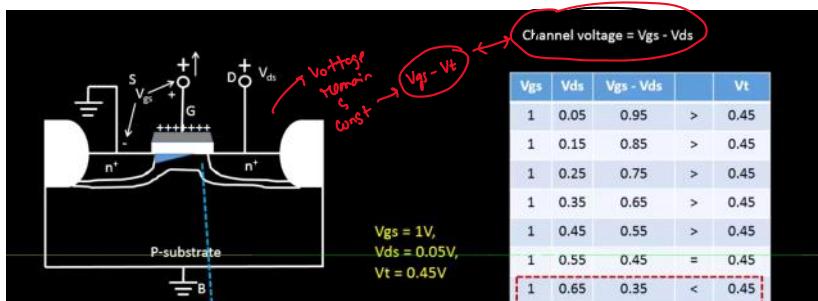
K

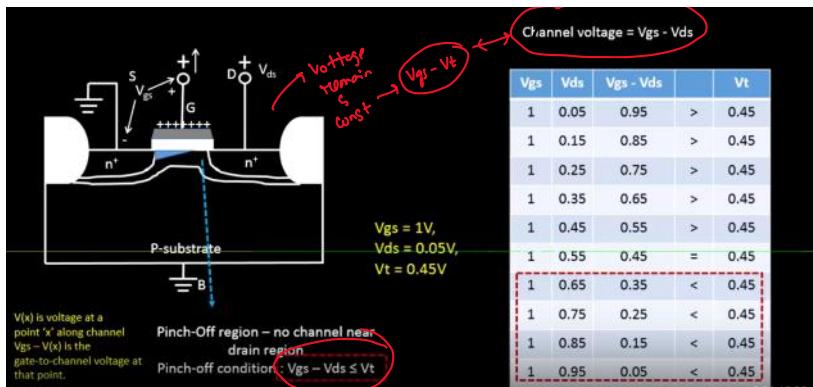
$$I_{ds} = K \left[(V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

$\rightarrow 0 \rightarrow$ when $V_{ds} < V_{gs} - V_{th}$

$$I_{ds} = K \left[(V_{gs} - V_{th}) V_{ds} \right]$$

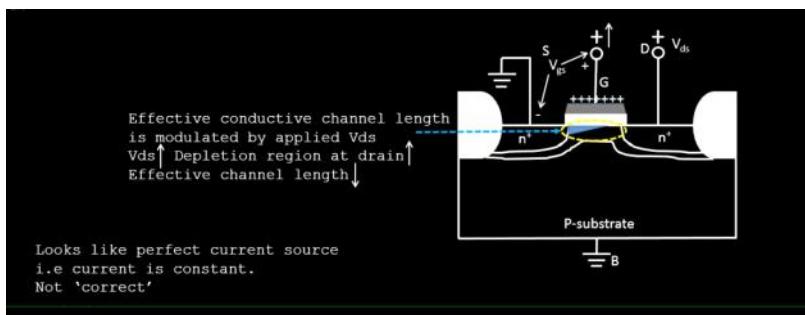
Linear Region Eqn





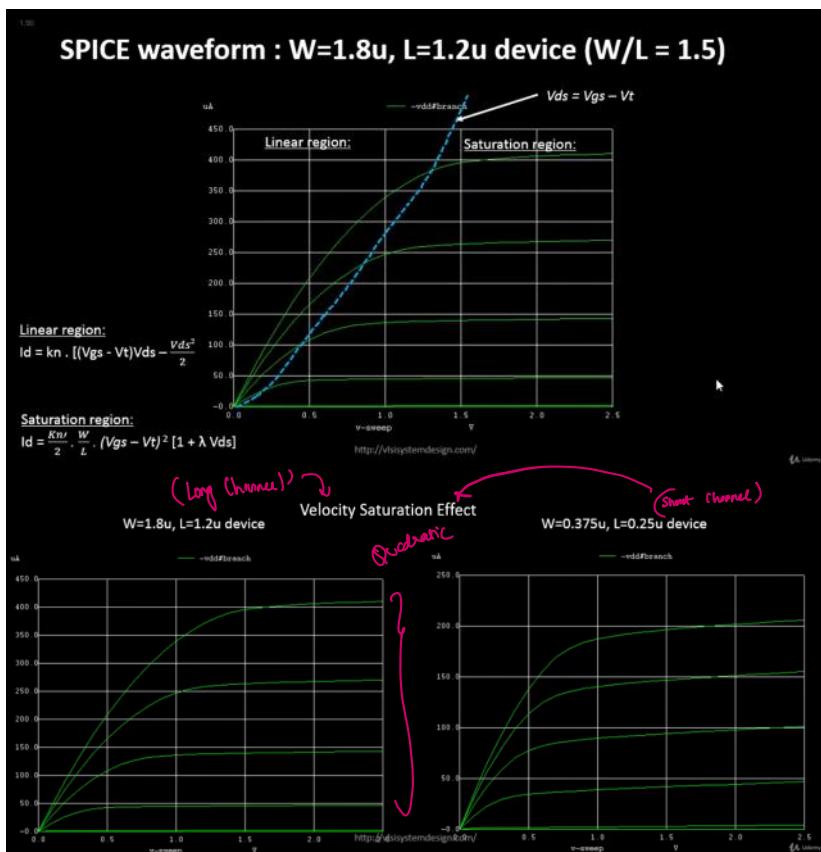
$$V_{ds} \approx V_{gs} - V_t \quad \text{correct}$$

$$I_d = \frac{k_n}{2} (V_{gs} - V_t)^2$$

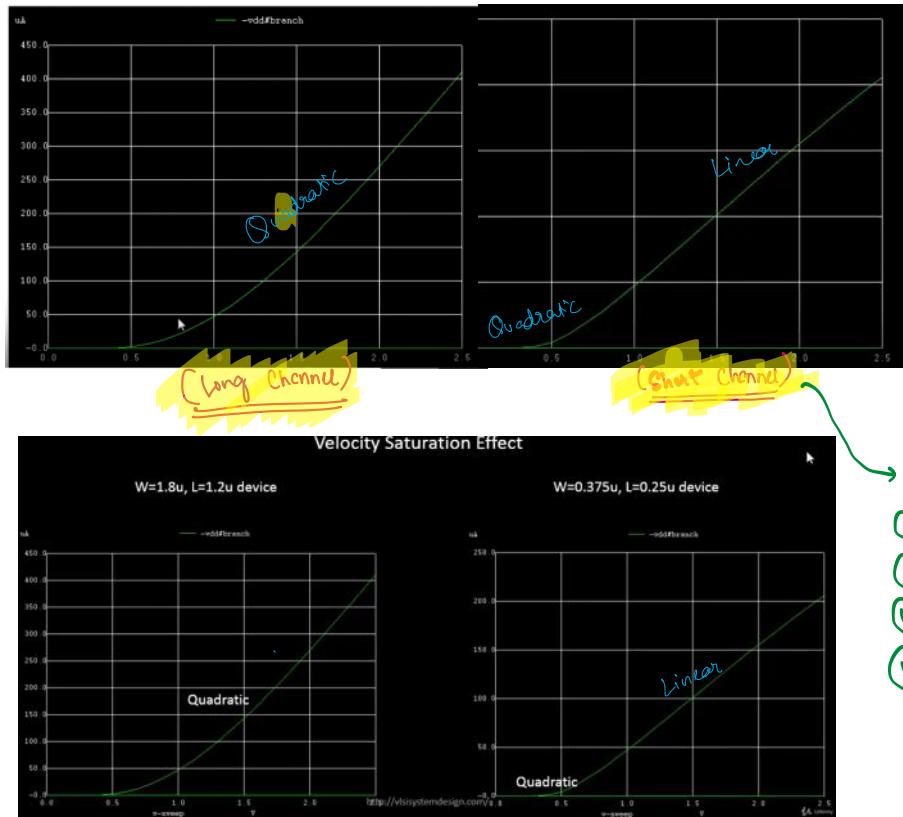


$$I_d = \frac{k_n}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_t)^2 (1 + \lambda V_{ds})$$

↓
 Channel length Modulation }



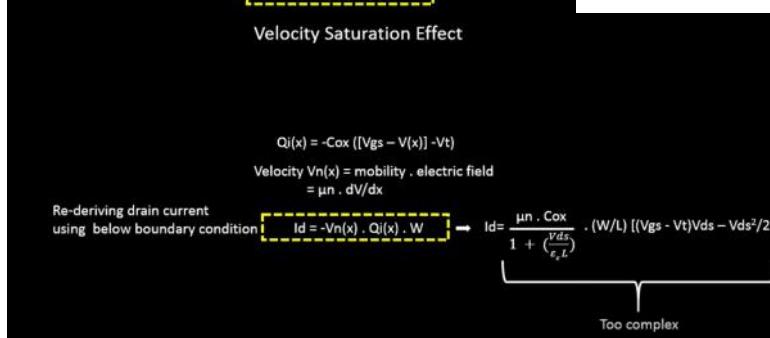
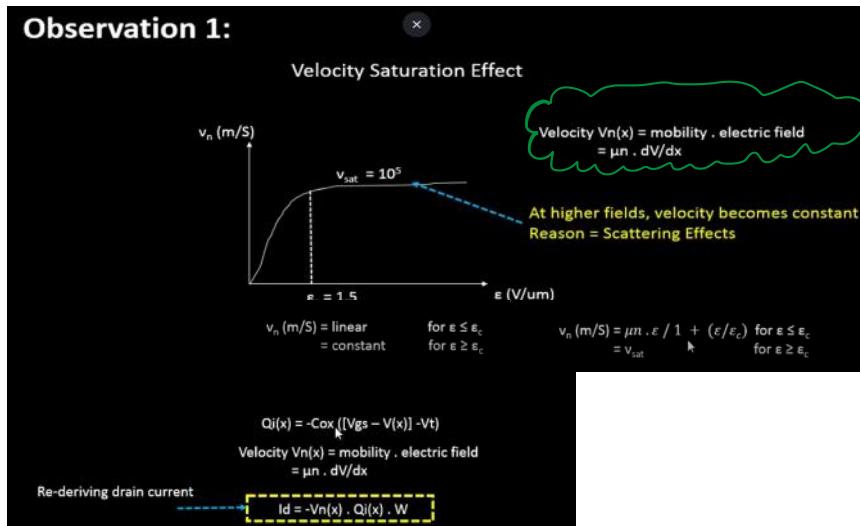
Effect called Velocity Saturation



Four Regions

- ① Cutoff
- ② Linear
- ③ Saturation
- ④ Velocity Saturation

Observation 1:



Velocity Saturation Effect

Let's come up with one model

Operation modes

Long Channel (>250nm)	Short Channel (<250nm)
Cutoff	Cutoff
Resistive	Resistive
	Velocity Saturation
Saturation	Saturation

Observation 1:

Velocity Saturation Effect

Let's come up with one model

Operation modes

Let's call $(V_{gs} - V_t) = V_{gt}$

Long Channel (>250nm)	Short Channel (<250nm)
Cutoff	Cutoff
Resistive	Resistive
	Velocity Saturation
Saturation	Saturation

$I_d = 0$, for $V_{gt} < 0$, cutoff mode

For all other modes, let's use below model

$$I_d = k_n \cdot [(V_{gt} \cdot V_{min}) - \frac{V_{min}^2}{2}] \cdot [1 + \lambda V_{ds}]$$

Where $V_{min} = \min(V_{gt}, V_{ds}, V_{dsat})$

Drain Current Model.

Velocity Saturation Effect

Let's come up with one model

Operation modes

Let's call $(V_{gs} - V_t) = V_{gt}$

Long Channel (>250nm)	Short Channel (<250nm)
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$$I_d = k_n \cdot [(V_{gt} \cdot V_{min}) - \frac{V_{min}^2}{2}] \cdot [1 + \lambda V_{ds}]$$

Where $V_{min} = \min(V_{gt}, V_{ds}, V_{dsat})$

For e.g., If $V_{gt} = \text{minimum value}$

$$I_d = K_n \cdot \left[\frac{V_{gt}}{2} \right] \cdot [1 + \lambda V_{ds}]$$

<http://vlsiystemsdesigns.com/>

For Short Channel Model

Technology parameter

Saturation voltage i.e. voltage at which device velocity saturates and is independent of V_{gs} or V_{ds}

Now if

$$V_{ds} = V_{min}$$

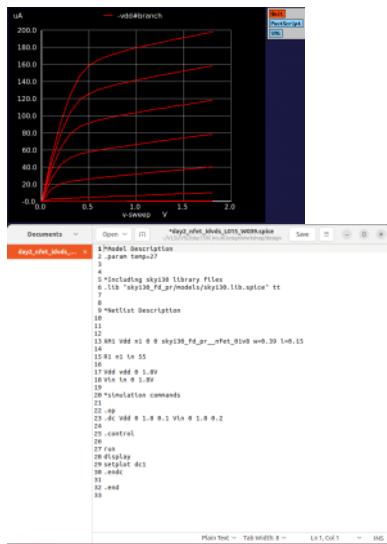
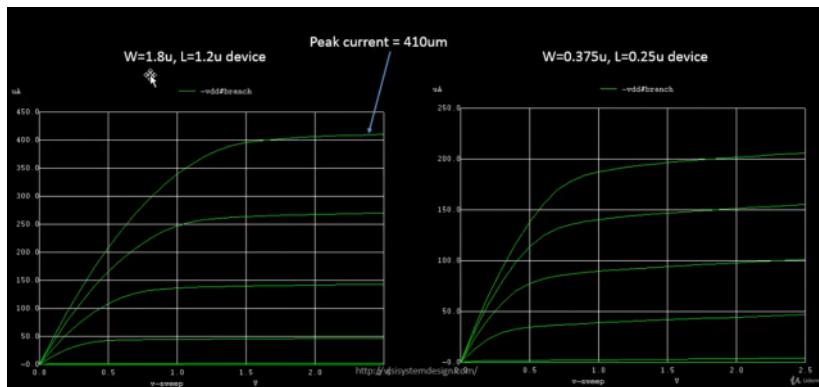
$$I_d = k_n \left[\frac{V_{gt} \cdot V_{ds}}{2} \right] [1 + \lambda V_{ds}]$$

Now if

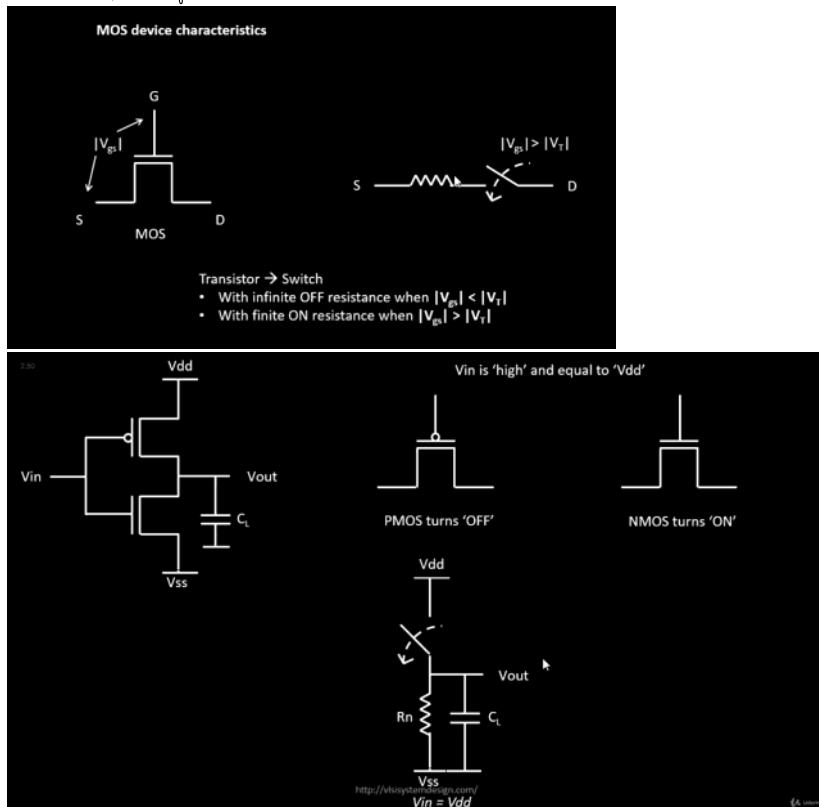
$$V_{min} = V_{dsat}$$

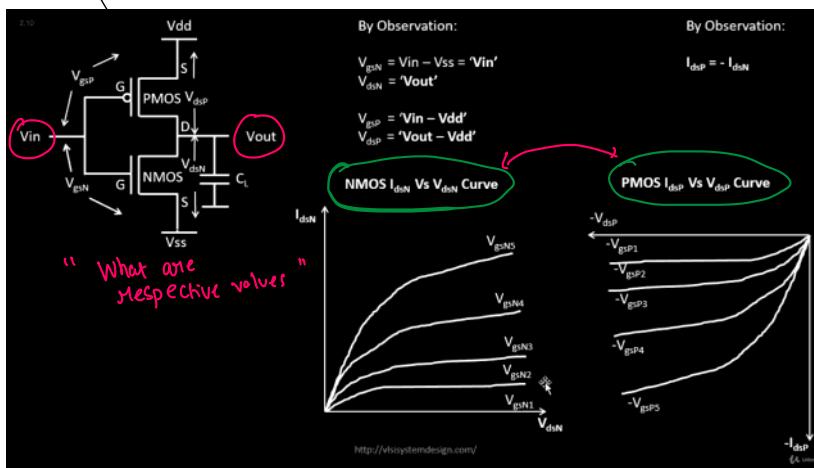
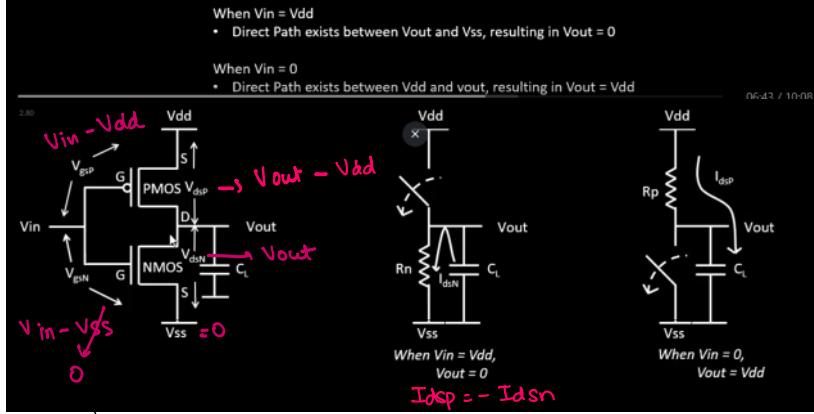
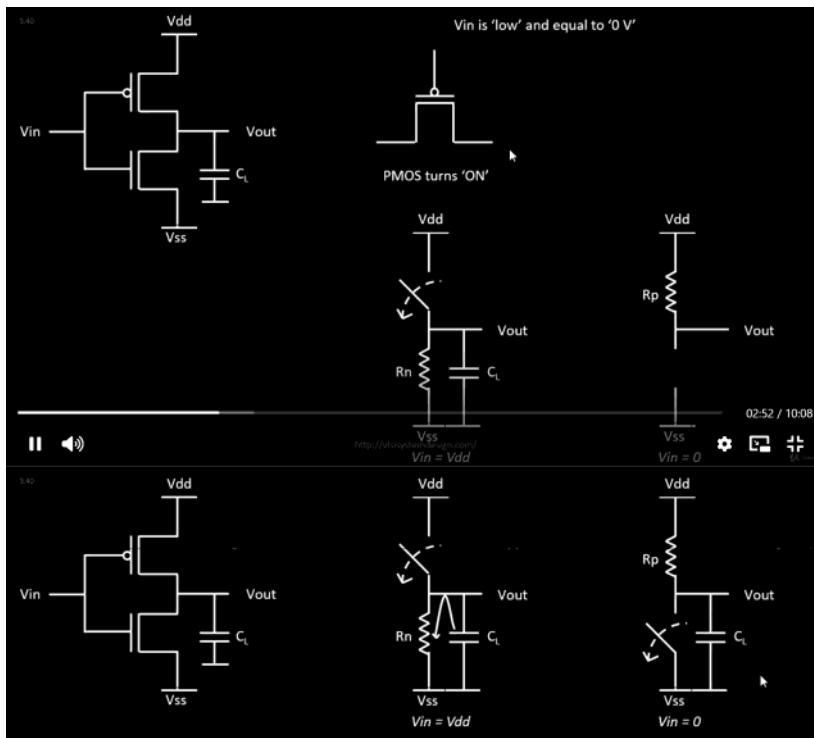
$$I_d = K_n \left\{ V_{gt} \cdot V_{dsat} \right\} - \frac{V_{dsat}^2}{2} \cdot (1 + \lambda V_{ds})$$

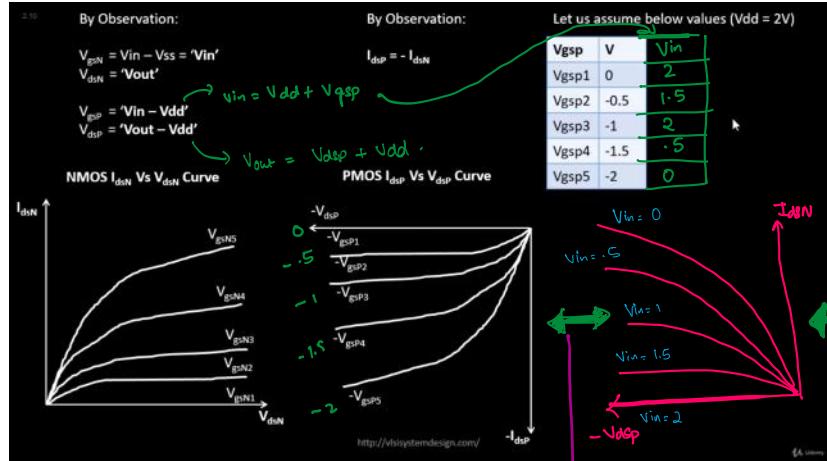
$$\left(N_a \cdot \lambda \cdot \frac{W}{L} \right) \left\{ V_{gt} \cdot V_{dsat} - \frac{V_{dsat}^2}{2} \right\}$$



(Voltage Transfer Characteristics)

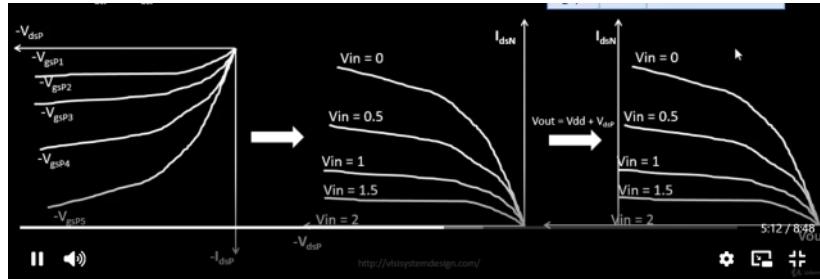






we got rid of \sqrt{qsp} \rightarrow (VII)

Now we need to get rid of (V_{dp})



Idson.

$V_{ds} + V_{dd} = V_{out}$

$V_{in} = 0$

$V_{in} = 1$

$V_{in} = 1.5$

$V_{in} = 2$

$V_{in} = 5$

V_{out}

V_{in}

V_{ds}

V_{out}

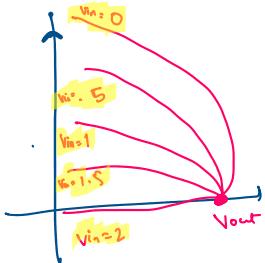
we eliminated
 V_{ds} = .

$V_{in} \vee/s V_{out}$

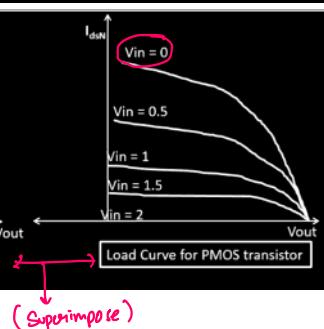
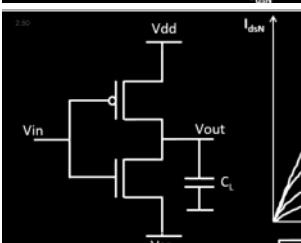
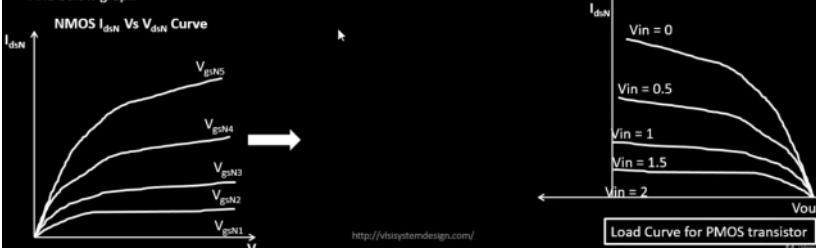
(so) that we can get

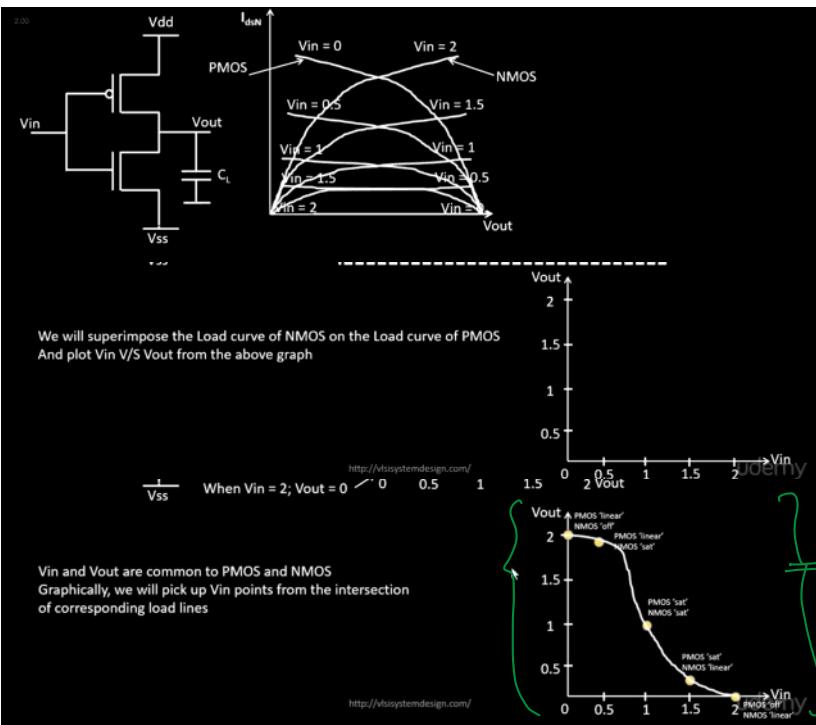
Obtain Load Curve

$$V_{DSN} = \frac{V_{IN}}{I_{DSN}} \quad V_{DSR} = \frac{V_{OUT}}{I_{DSR}}$$

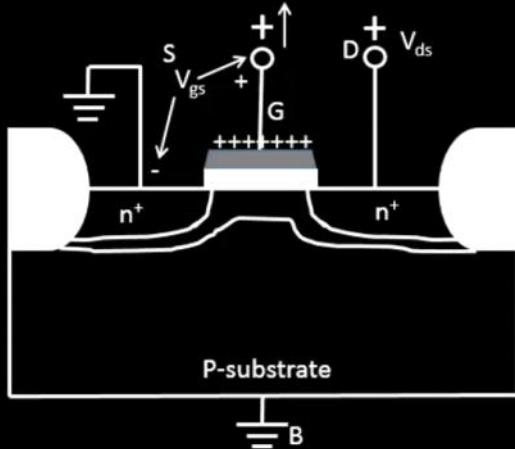


Let us obtain the Load Curve for NMOS transistor using the above equations
And below graph





SPICE setup



Threshold Voltage Equation:

$$V_t = V_{to} + \gamma (\sqrt{|-2\Phi_f + V_{sb}|} - \sqrt{|-2\Phi_f|})$$

$$\gamma = \frac{\sqrt{2qNA\varepsilon_{si}}}{C_{ox}}$$

$$\Phi_f = -\Phi_T * \ln \frac{N_A}{n_i}$$

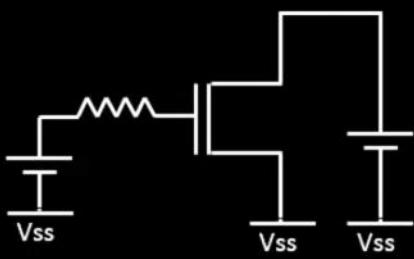
Linear region:

$$I_d = kn \cdot [(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}]$$

Saturation region:

$$I_d = \frac{Kn}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_t)^2 [1 - \lambda V_{ds}]$$

SPICE setup



SPICE model parameters

+ SPICE netlist

SPICE
SOFTWARE

Threshold Voltage Equation:

$$V_t = V_{to} + \gamma (\sqrt{|-2\Phi_f + V_{sb}|} - \sqrt{|-2\Phi_f|})$$

$$\gamma = \frac{\sqrt{2qNA\varepsilon_{si}}}{C_{ox}}$$

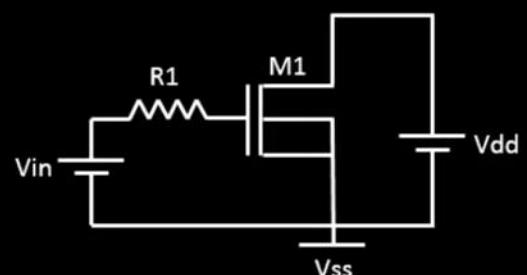
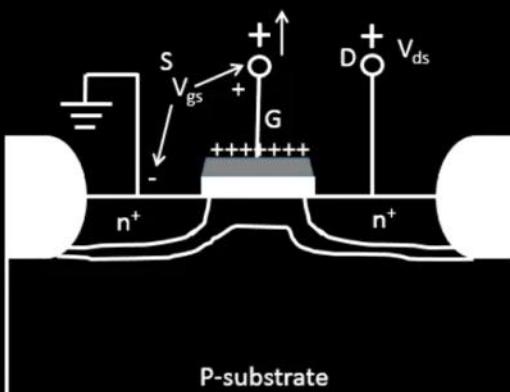
$$\Phi_f = -\Phi_T * \ln \frac{N_A}{n_i}$$

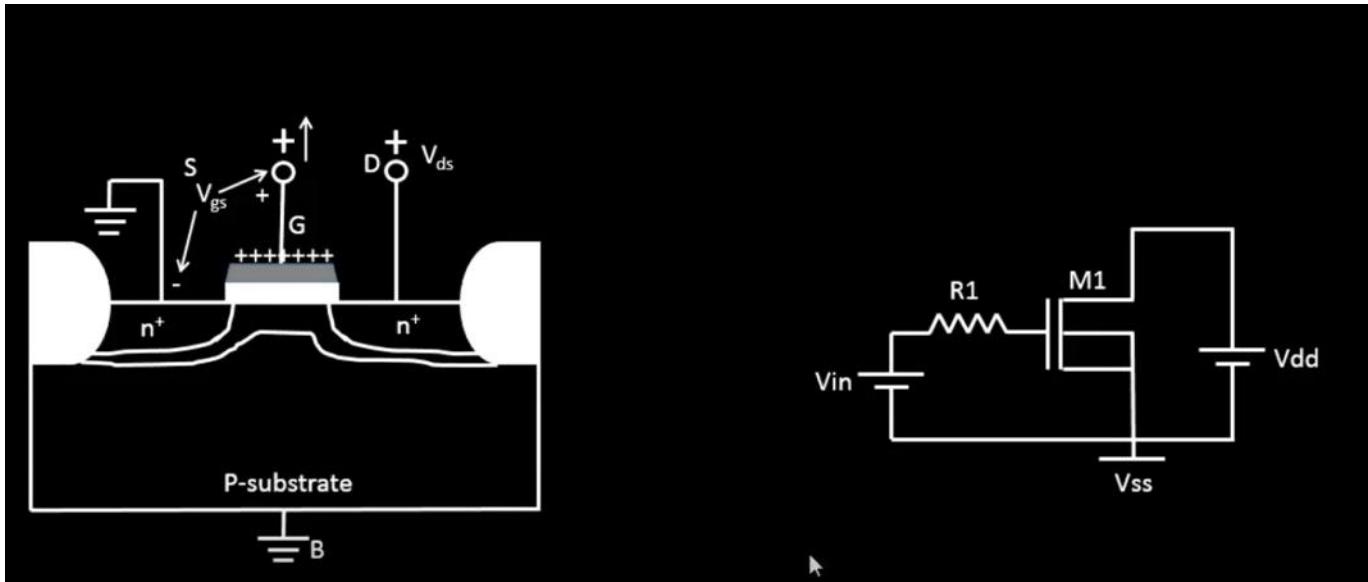
Linear region:

$$I_d = kn \cdot [(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}]$$

Saturation region:

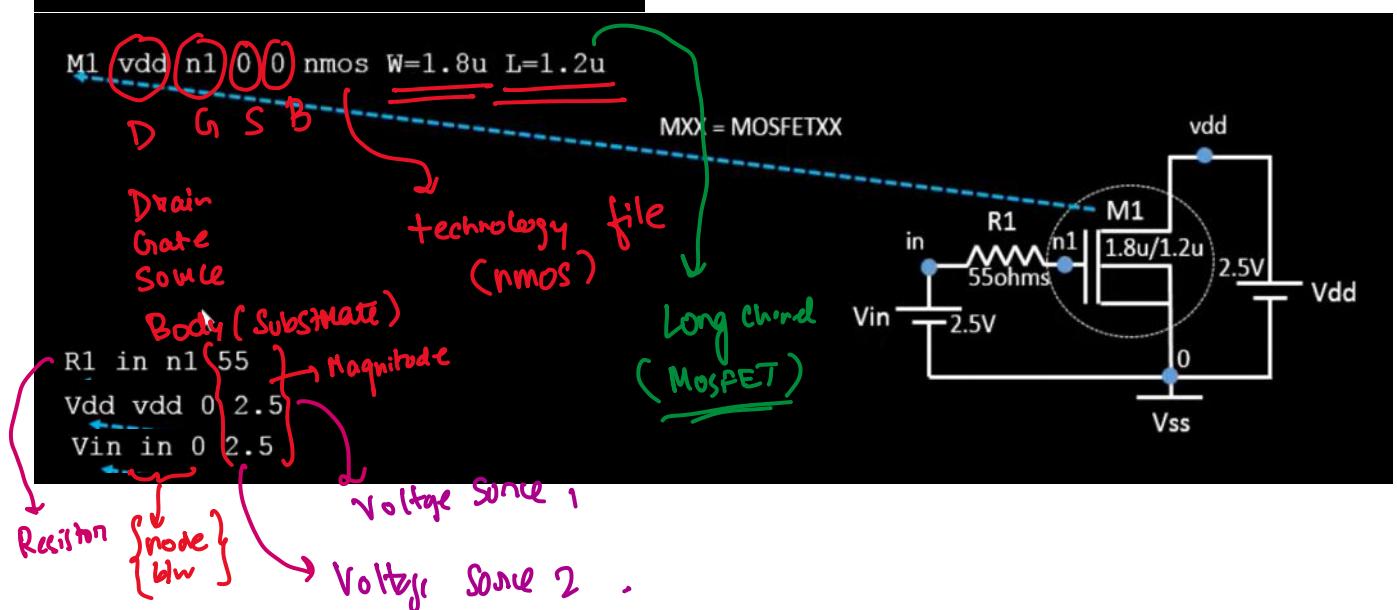
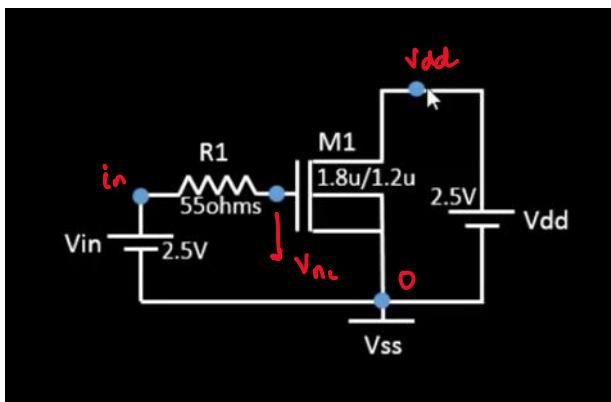
$$I_d = \frac{Kn}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_t)^2 [1 - \lambda V_{ds}]$$





SPICE netlist

① Define the nodes



```
.MODEL nmos NMOS (...  
+ ....)  
.MODEL pmos PMOS (...  
+ ....)  
.endl
```

SPICE netlist

Technology file

```
M1 vdd n1 0 0 nmos W=1.8u L=1.2u  
R1 in n1 55  
Vdd vdd 0 2.5  
Vin in 0 2.5
```

Threshold Voltage Equation:
$$V_t = V_{to} + \gamma \left(\sqrt{|-2\Phi_f + V_{sb}|} - \sqrt{|-2\Phi_f|} \right)$$
$$\gamma = \frac{2qN\epsilon_s}{C_{ox}}$$

$$\Phi_f = -\Phi_T * \ln \frac{N_A}{n_i}$$

```
.MODEL nmos NMOS (TOX = ..  
+ VTH0 = .. U0 = .. GAMMA1 = ..)
```

Linear region:

$$I_d = k_n \cdot [(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}]$$

Saturation region:

$$I_d = \frac{k_n}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_t)^2 [1 - \lambda V_{ds}]$$

```
*** NETLIST Description ***  
M1 vdd n1 0 0 nmos W=1.8u L=1.2u  
R1 in n1 55  
Vdd vdd 0 2.5  
Vin in 0 2.5  
*** .include xxxx_lum_model.mod ***  
.LIB "xxxx_025um_model.mod" CMOS_MODELS
```

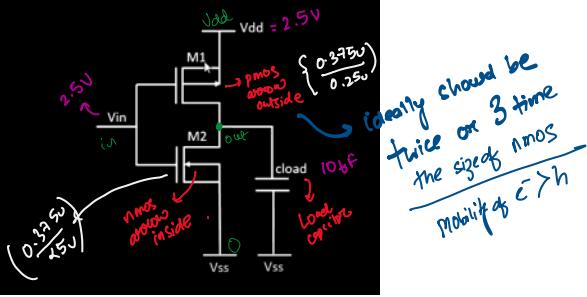
"Complete Netlist
Simulation."

SPICE deck

- Component connectivity
- Component values
- Identify "nodes"
- Name "nodes"

Writing SPICE deck

D GSB → order of defining nodes



```
*** MODEL Descriptions ***
*** NETLIST Description ***
M1 out in vdd vdd pmos W=0.375u L=0.25u
M2 out in 0 0 nmos W=0.375u L=0.25u
```

SPICE deck

```
*** MODEL Descriptions ***
*** NETLIST Description ***
M1 out in vdd vdd pmos W=0.375u L=0.25u
M2 out in 0 0 nmos W=0.375u L=0.25u

cload out 0 10f

Vdd vdd 0 2.5
Vin in 0 2.5
*** SIMULATION Commands ***
.op
.dc Vin 0 2.5 0.05
*** .include tsmc_025um model.mod ***
.LIB "tsmc_025um model.mod" CMOS MODELS
.end
```

SPICE waveform : $W_n=W_p=0.375\mu$, $L_n, p=0.25\mu$ device
($W_n/L_n=W_p/L_p = 1.5$)

Charge guns width [] plot out v/s in { goto spice deck }

SPICE waveform : $W_n=0.375$, $W_p=0.9375\mu$, $L_n, p=0.25\mu$ device
($W_n/L_n=1.5$, $W_p/L_p = 2.5$)

plot (out v/s in) → goto spice deck -

plot (out v/s time in)

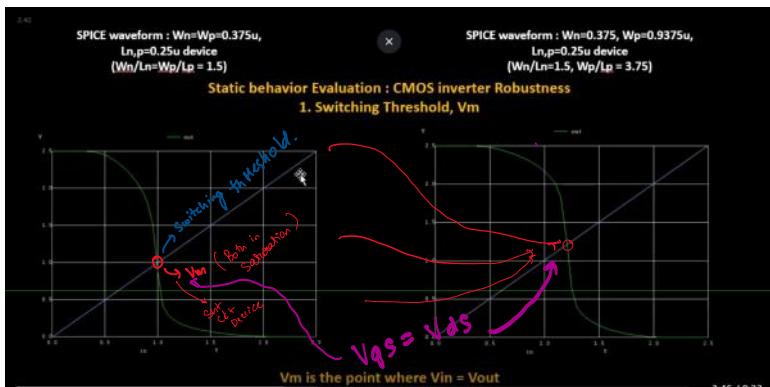
t_R rise delay

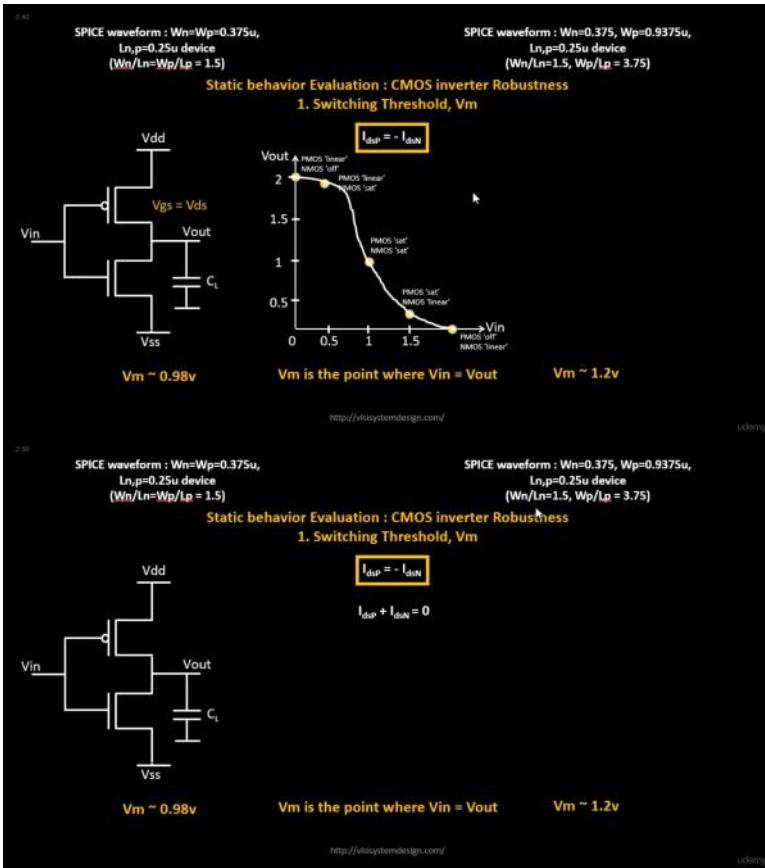
t_f Fall Delay.

ngspice
day 3 VTC
find threshold voltage

→ for simulation [ngspice]

CMOS → ROBUST DEVICE
(widely used logic)





We know

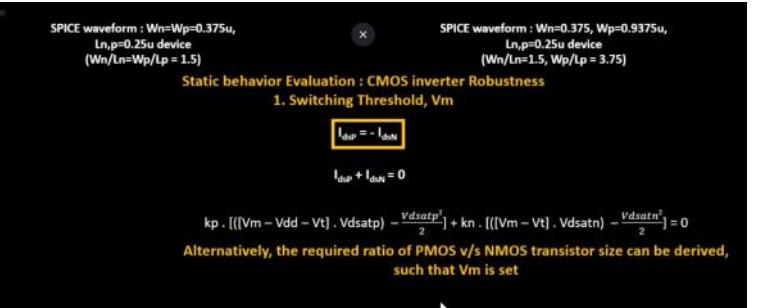
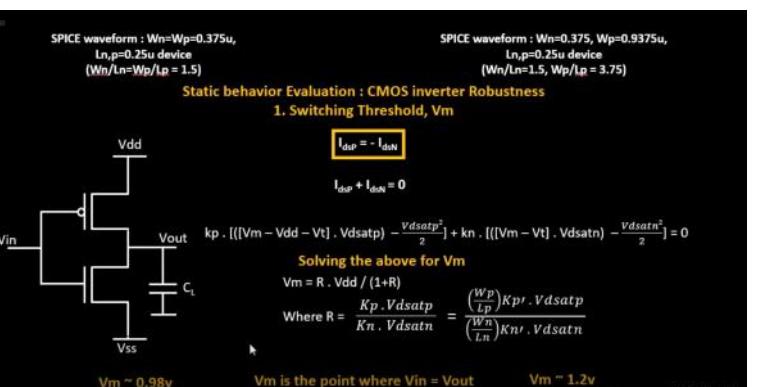
$$I_{d_{sp}} = -I_{d_{N}}$$

$$\Rightarrow I_{d_{N}} + I_{d_{sp}} = 0$$

$$\left\{ \begin{array}{l} I_{d_{N}} = K_n \left[(V_m - V_t) V_{d_{satN}} - \frac{V_{dsatN}^2}{2} \right] \\ I_{d_{sp}} = K_p \left[(V_m - Vdd - V_t) V_{d_{satP}} - \frac{V_{dsatP}^2}{2} \right] \end{array} \right.$$

$$+ \quad \text{Solving} \Rightarrow \left(V_m = R \frac{Vdd}{1+R} \right) = 0$$

where $R = \frac{K_p (V_{d_{satP}})}{K_n (V_{d_{satN}})} = \frac{(W_p)(L_n)}{(W_n)(L_p)}$



SPICE waveform : $Wn=Wp=0.375u$,
 $Ln,p=0.25u$ device
 $(Wn/Ln=Wp/Lp = 1.5)$

SPICE waveform : $Wn=0.375$, $Wp=0.9375u$,
 $Ln,p=0.25u$ device
 $(Wn/Ln=1.5, Wp/Lp = 3.75)$

Static behavior Evaluation : CMOS inverter Robustness

1. Switching Threshold, V_m

$I_{dsP} = -I_{dsN}$

$I_{dsP} + I_{dsN} = 0$

$kp \cdot [([V_m - Vdd - Vt] \cdot Vdsatp) - \frac{Vdsatp^2}{2}] + kn \cdot [([V_m - Vt] \cdot Vdsatn) - \frac{Vdsatn^2}{2}] = 0$

Alternatively, the required ratio of PMOS v/s NMOS transistor size can be derived, such that V_m is set

$kn \cdot [([V_m - Vt] \cdot Vdsatn) - \frac{Vdsatn^2}{2}] = -kp \cdot [([V_m - Vdd - Vt] \cdot Vdsatp) - \frac{Vdsatp^2}{2}]$

$V_m \approx 0.98v$ V_m is the point where $Vin = Vout$ $V_m \approx 1.2v$

Alternatively, the required ratio of PMOS v/s NMOS transistor size can be derived, such that V_m is set

$Kn \cdot Vdsatn \cdot [([V_m - Vt]) - \frac{Vdsatn}{2}] = Kp \cdot Vdsatp \cdot [([-V_m + Vdd + Vt]) + \frac{Vdsatp}{2}]$

such that V_m is

$$\frac{Kp \cdot Vdsatp}{Kn \cdot Vdsatn} = \frac{([V_m - Vt]) - \frac{Vdsatn}{2}}{([-V_m + Vdd + Vt]) + \frac{Vdsatp}{2}}$$

such that V_m is set

$$\frac{\left(\frac{W_p}{L_p}\right)}{\left(\frac{W_n}{L_n}\right)} = \frac{Kn \cdot Vdsatn([V_m - Vt]) - \frac{Vdsatn}{2}}{Kp \cdot Vdsatp([-V_m + Vdd + Vt]) + \frac{Vdsatp}{2}}$$

$$V_m = R \cdot Vdd / (1+R)$$

$$\text{Where } R = \frac{Kp \cdot Vdsatp}{Kn \cdot Vdsatn} = \frac{\left(\frac{W_p}{L_p}\right) Kp \cdot Vdsatp}{\left(\frac{W_n}{L_n}\right) Kn \cdot Vdsatn}$$

$$\frac{\left(\frac{W_p}{L_p}\right)}{\left(\frac{W_n}{L_n}\right)} = \frac{Kn \cdot Vdsatn([V_m - Vt]) - \frac{Vdsatn}{2}}{Kp \cdot Vdsatp([-V_m + Vdd + Vt]) + \frac{Vdsatp}{2}}$$

SPICE waveform : $Wn=Wp=0.375u$,
 $Ln,p=0.25u$ device
 $(Wn/Ln=Wp/Lp = 1.5)$

SPICE waveform : $Wn=0.375$, $Wp=0.9375u$,
 $Ln,p=0.25u$ device
 $(Wn/Ln=1.5, Wp/Lp = 3.75)$

Static behavior Evaluation : CMOS inverter Robustness

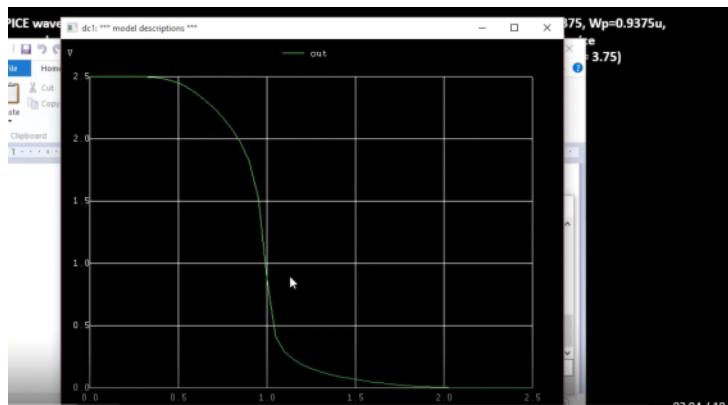
1. Switching Threshold, V_m

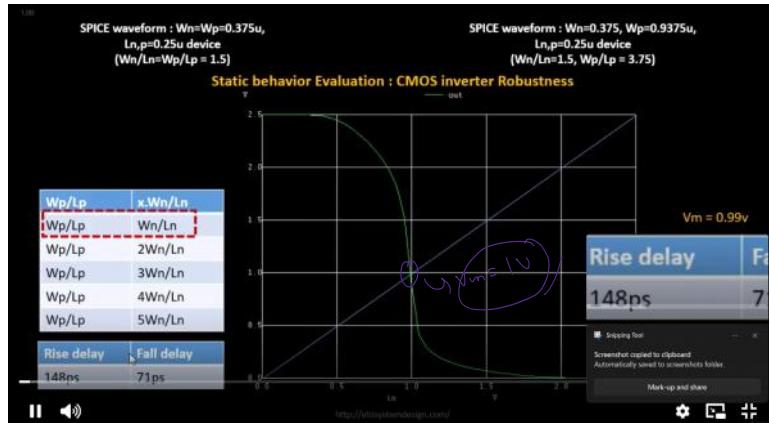
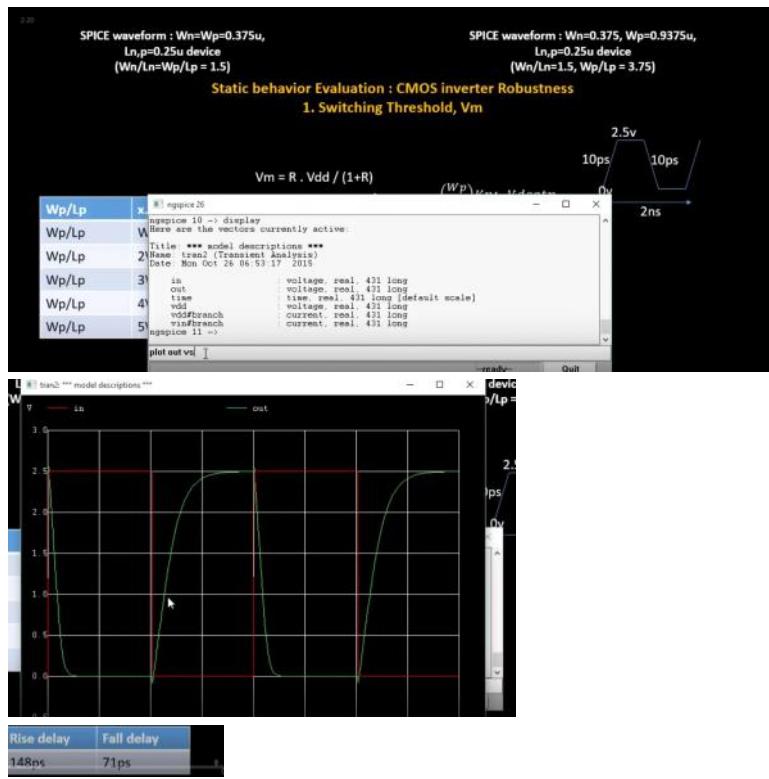
$$V_m = R \cdot Vdd / (1+R)$$

$$\text{Where } R = \frac{Kp \cdot Vdsatp}{Kn \cdot Vdsatn} = \frac{\left(\frac{W_p}{L_p}\right) Kp \cdot Vdsatp}{\left(\frac{W_n}{L_n}\right) Kn \cdot Vdsatn}$$

$$\frac{\left(\frac{W_p}{L_p}\right)}{\left(\frac{W_n}{L_n}\right)} = \frac{Kn \cdot Vdsatn([V_m - Vt]) - \frac{Vdsatn}{2}}{Kp \cdot Vdsatp([-V_m + Vdd + Vt]) + \frac{Vdsatp}{2}}$$

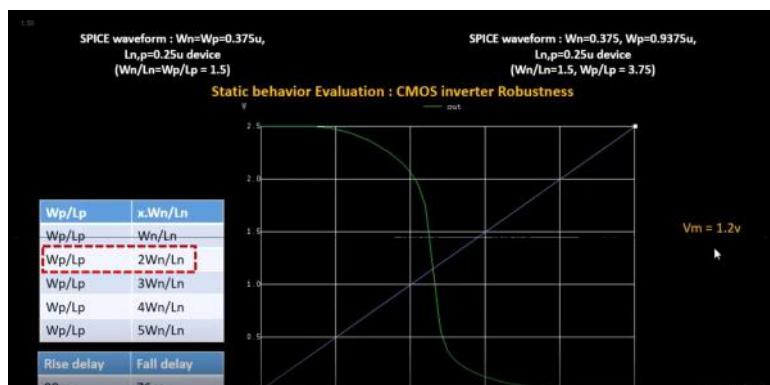
V_m is the point where $Vin = Vout$



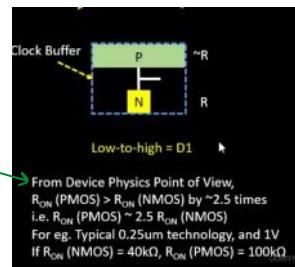
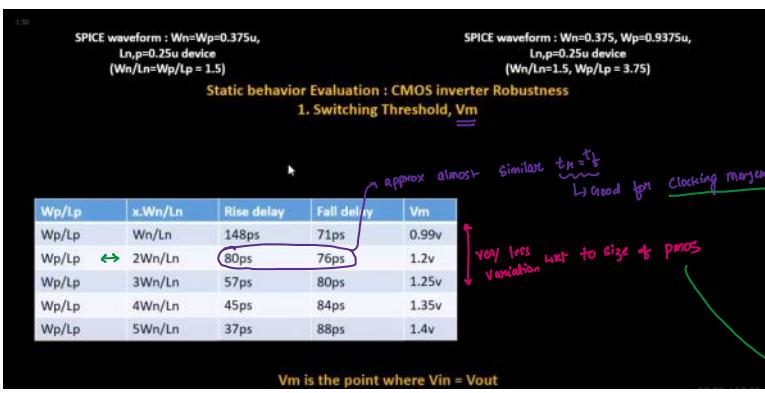
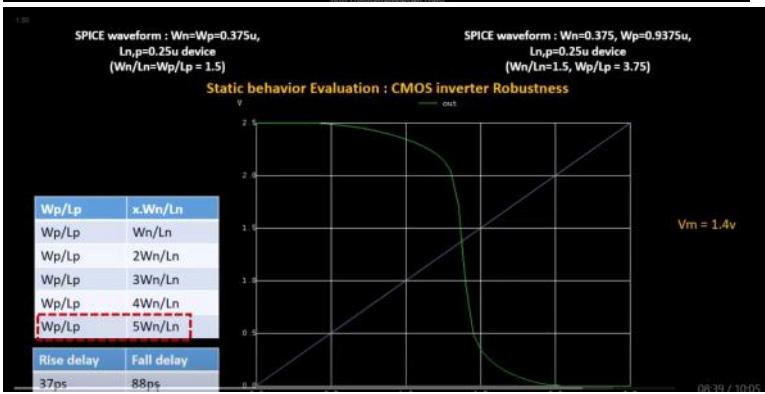
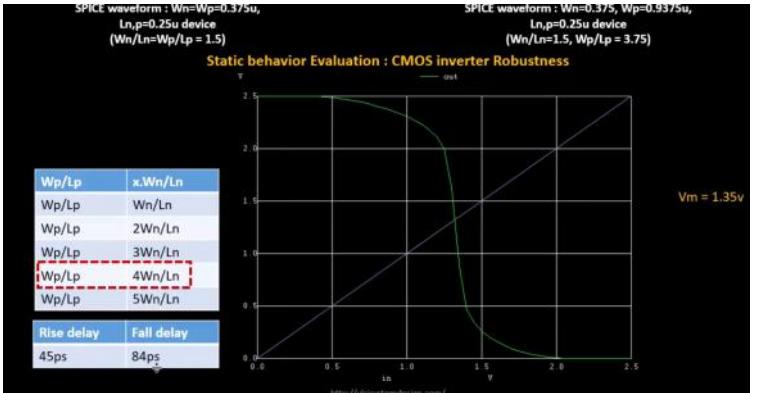
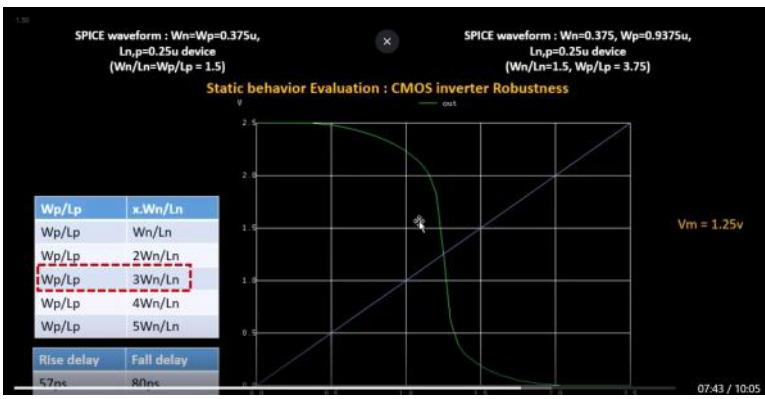


$$0.375 \times 2 = 0.75 \text{ v.}$$

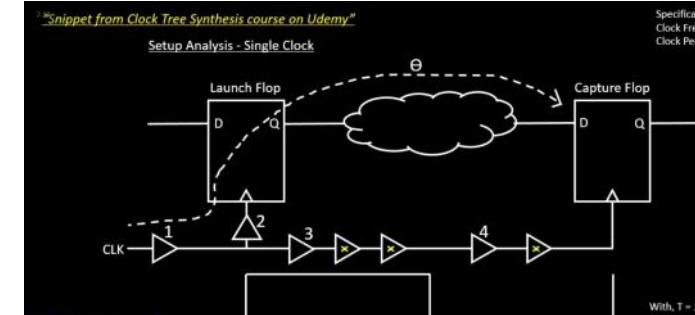
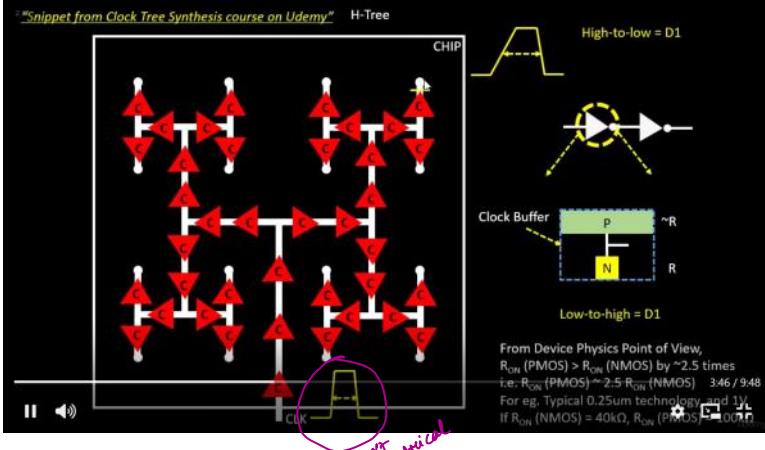
when we
double
what is
another
rise or fall delay.



Rise delay ↓ as PMOS ↑



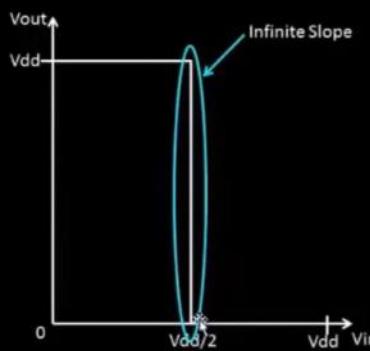
From Device Physics Point of View,
 $R_{ON}(PMOS) > R_{ON}(NMOS)$ by ~ 2.5 times
i.e. $R_{ON}(PMOS) \sim 2.5 R_{ON}(NMOS)$
For e.g. Typical 0.25um technology, and 1V
If $R_{ON}(NMOS) = 40k\Omega$, $R_{ON}(PMOS) = 100k\Omega$



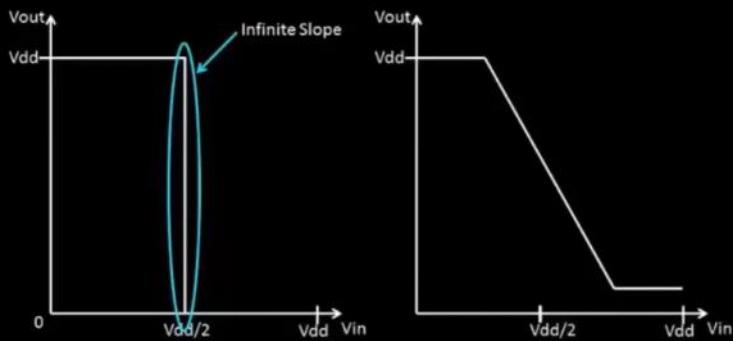
Static behavior Evaluation : CMOS inverter Robustness

2. Noise Margin, NM_H and NM_L

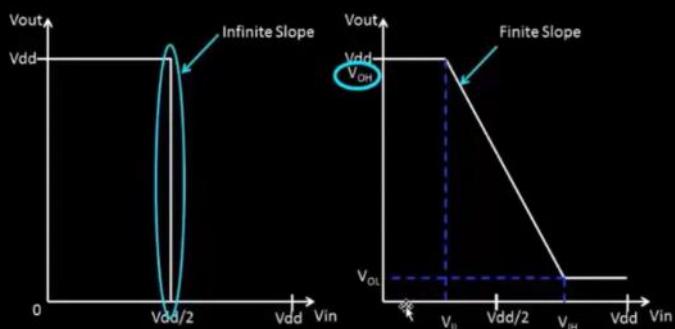
Noise Margin



Ideal I/O Characteristic of a Inverter with Infinite Slope

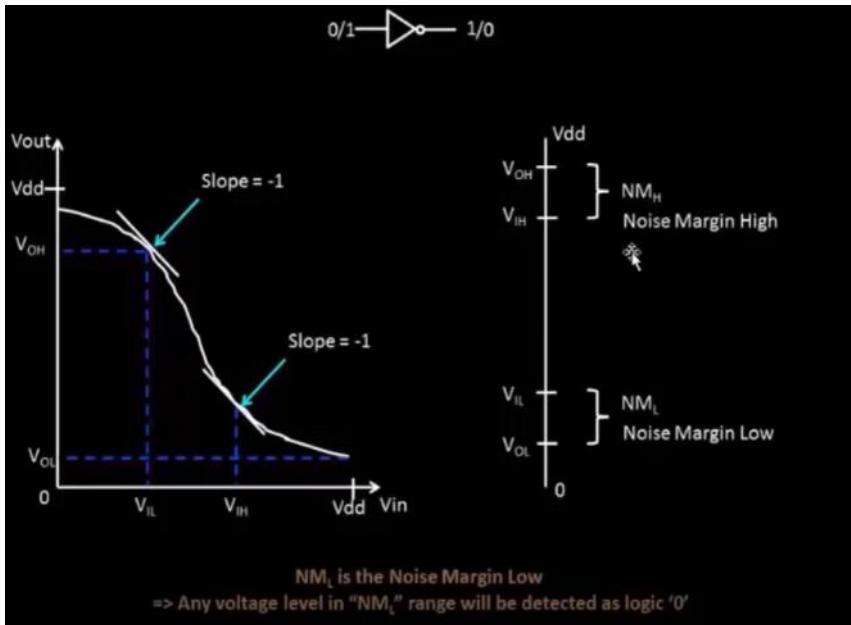
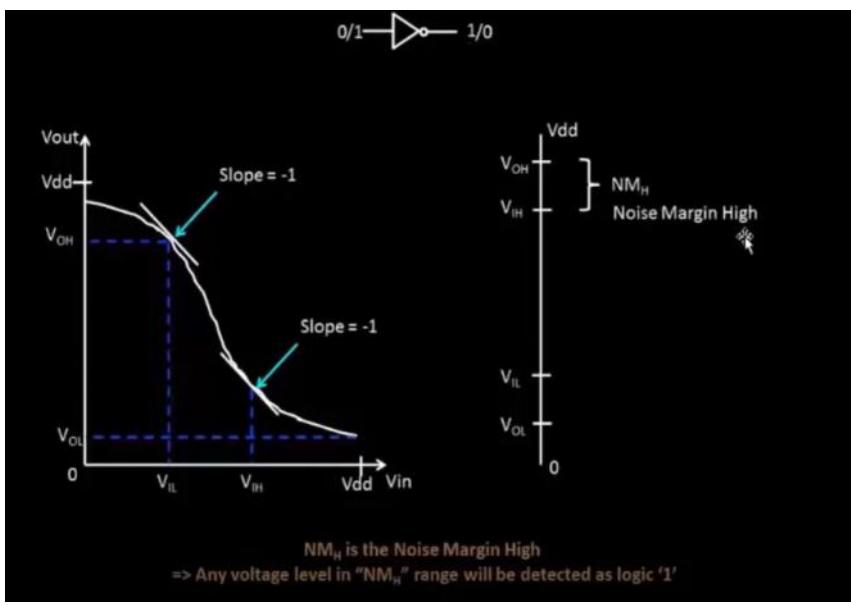
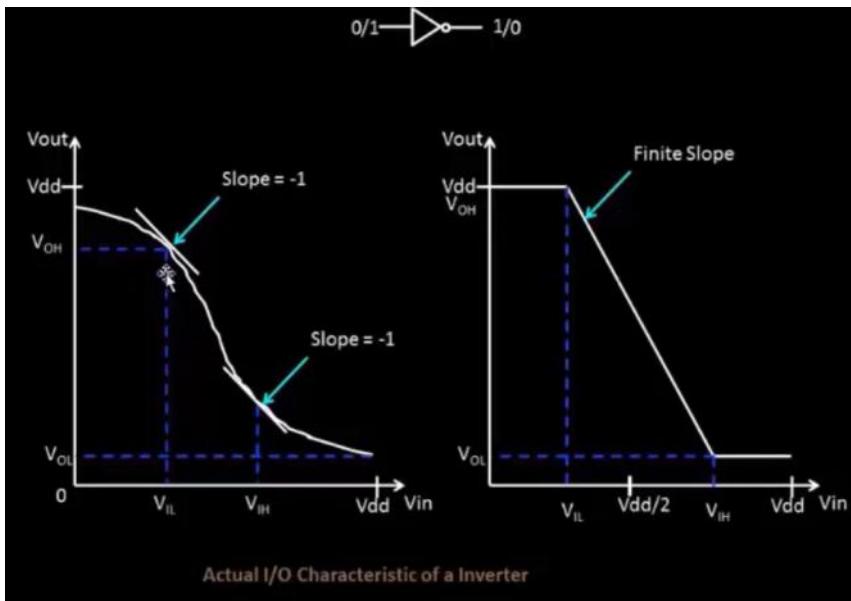


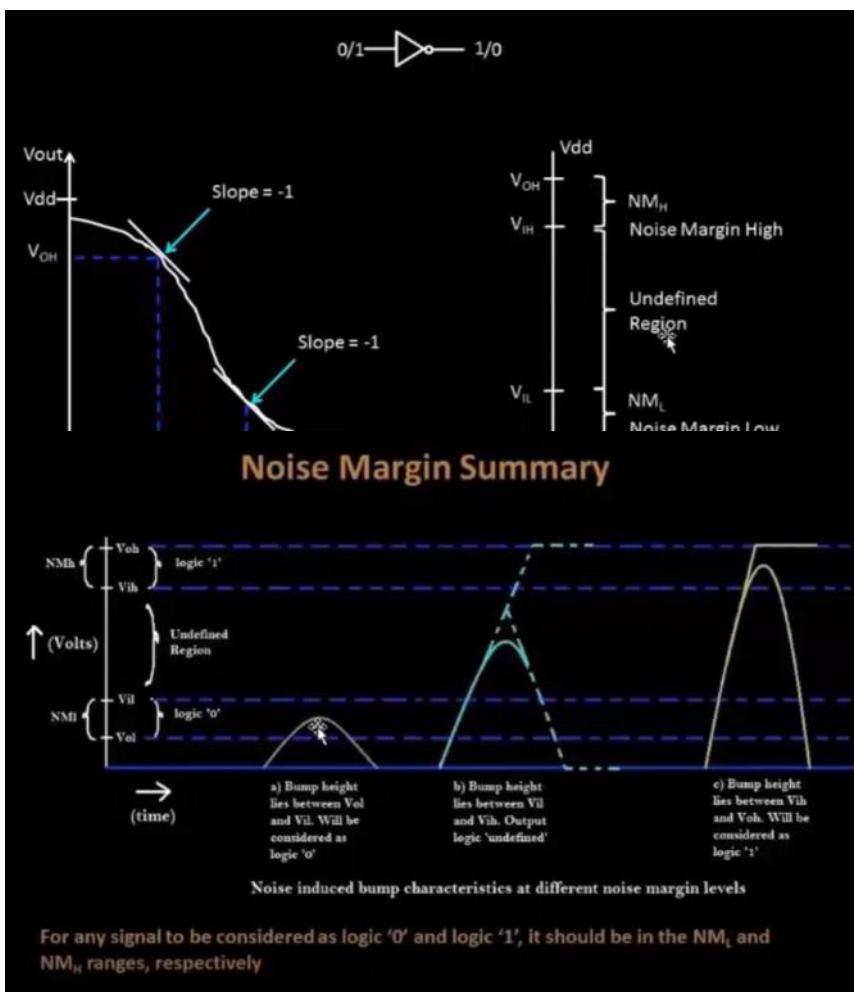
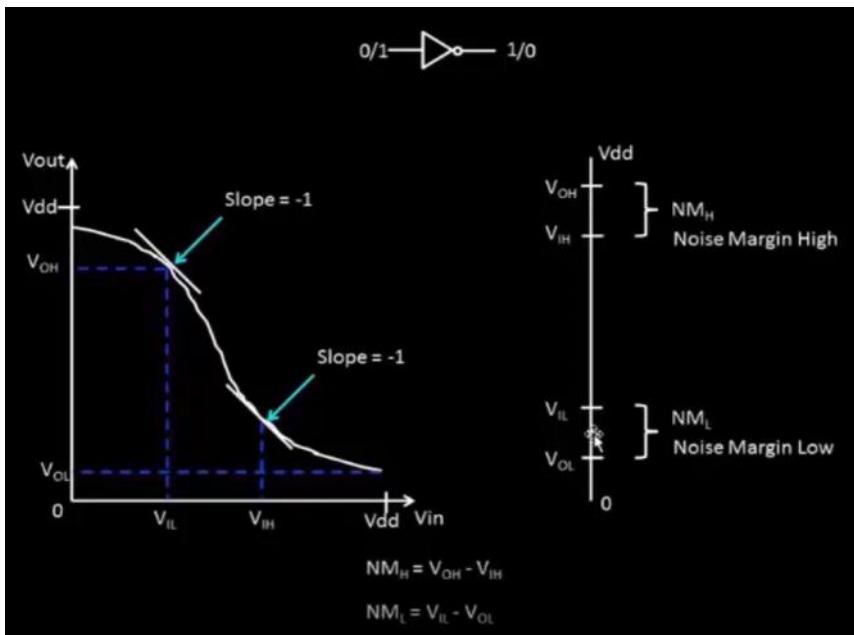
Actual I/O Characteristic of a Inverter with Finite Slope



V_{OH} is Output High Voltage

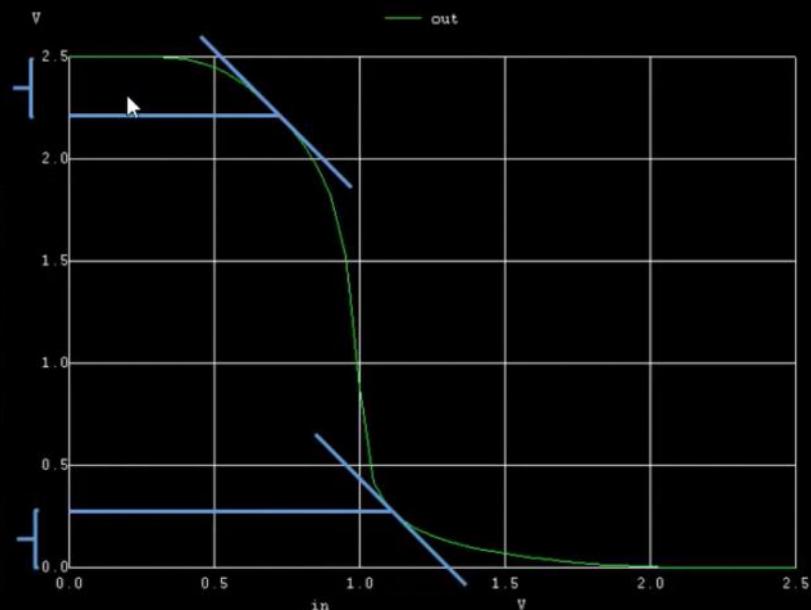
=>Any output voltage level between V_{OH} and V_{OO} will be treated as logic '1'





Static behavior Evaluation : CMOS inverter Robustness

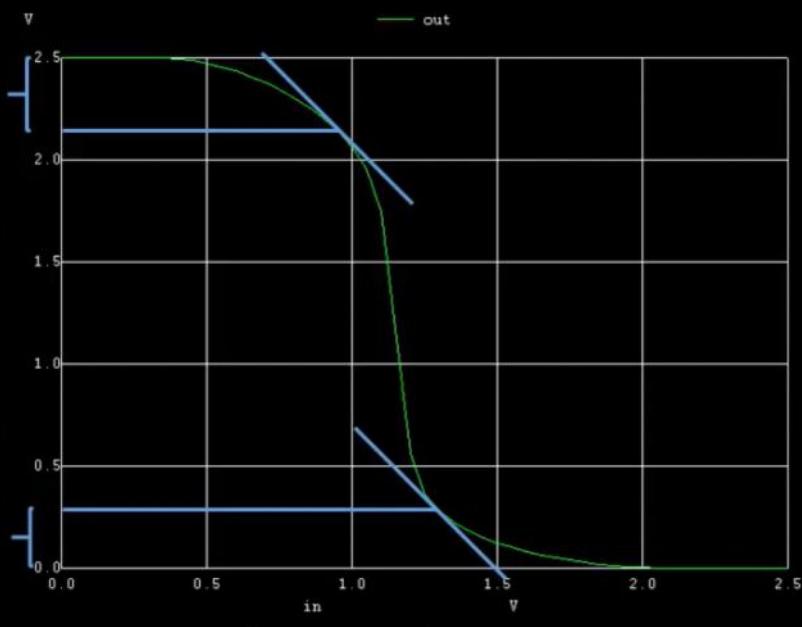
2. Noise Margin, NM_H and NM_L



udemy

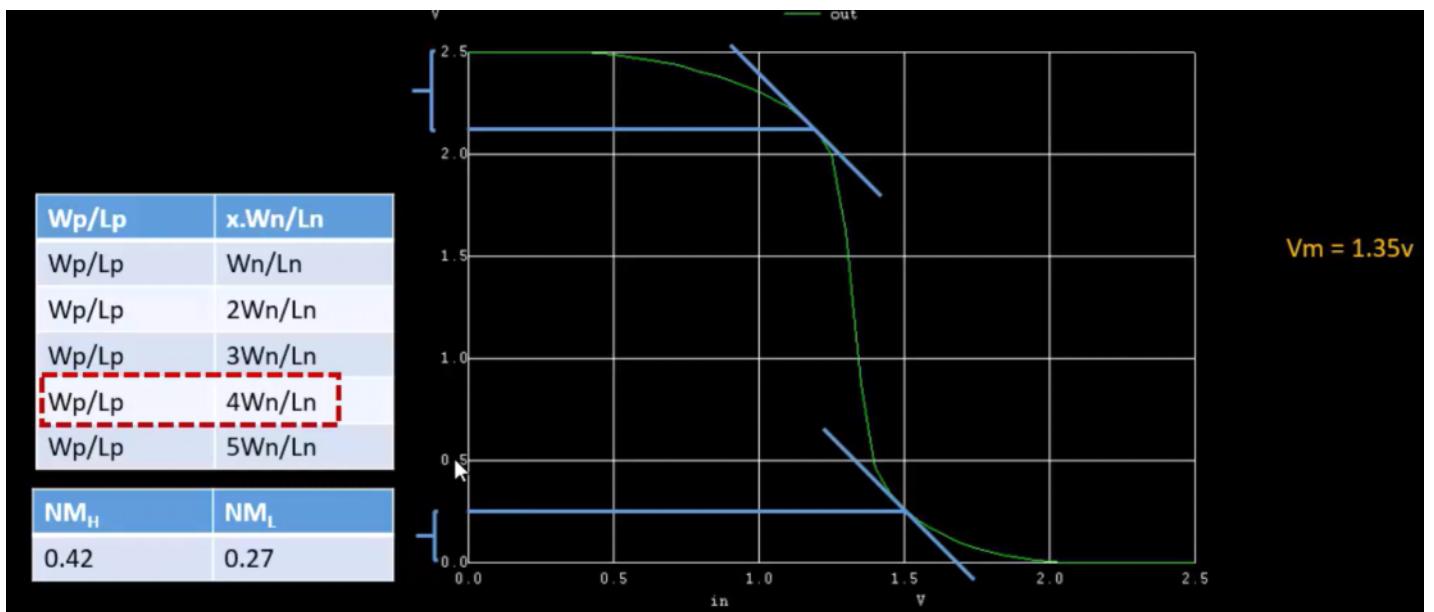
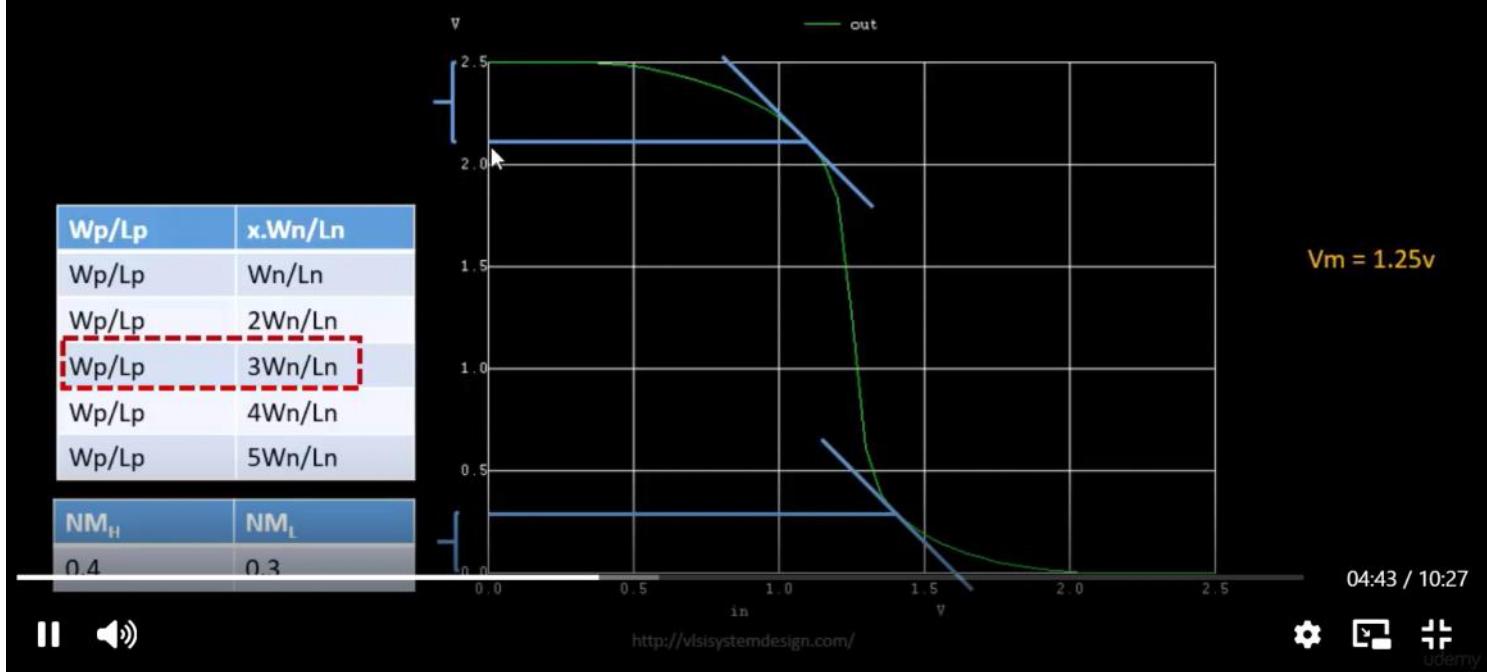
Static behavior Evaluation : CMOS inverter Robustness

2. Noise Margin, NM_H and NM_L



udemy

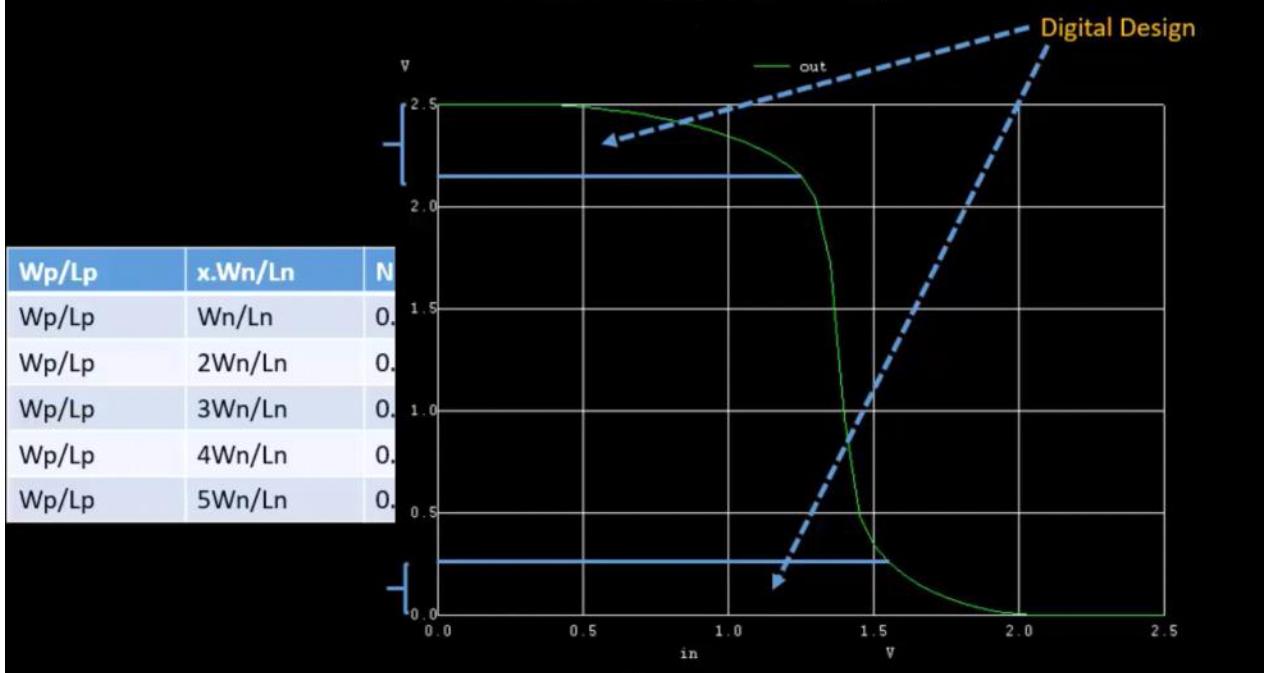
Static behavior Evaluation : CMOS inverter Robustness
2. Noise Margin, NM_H and NM_L



W_p/L_p	$x.W_n/L_n$	NM_H	NM_L	V_m
W_p/L_p	W_n/L_n	0.3	0.3	$0.99v$
W_p/L_p	$2W_n/L_n$	0.35	0.3	$1.2v$
W_p/L_p	$3W_n/L_n$	0.4	0.3	$1.25v$
W_p/L_p	$4W_n/L_n$	0.42	0.27	$1.35v$
W_p/L_p	$5W_n/L_n$	0.42	0.27	$1.4v$

Static behavior Evaluation : CMOS inverter Robustness

2. Noise Margin, NM_H and NM_L



```

File Edit View Search Terminal Tabs Help
radhika@radhika-VirtualBox:~/sky130CircuitDesignWorkshop/design$ radhika@radhika-VirtualBox:~/cmos_workshop/inv
radhika@radhika-VirtualBox:~/sky130CircuitDesignWorkshop/design$ ls
bsim4v5.out          day2_nfet_idvgs_015_W039.spice  day4_inv_noisemargin_wpi_wn036.spice      sky130_fd_pr
day1_nfet_idvds_L2_W5.spice   day3_inv_tran_Wp084_Wn036.spice  day5_inv_devcvariation_wp7_wn042.spice
day2_nfet_idvds_1015_W039.spice  day3_inv_vtc_Wp084_Wn036.spice  day5_inv_supplyvariation_wpi_Wn036.spice
radhika@radhika-VirtualBox:~/sky130CircuitDesignWorkshop/design$ vim day4_inv_noisemargin_wpi_wn036.spice
radhika@radhika-VirtualBox:~/sky130CircuitDesignWorkshop/design$ ngspice day4_inv_noisemargin_wpi_wn036.spice
*****
** ngspice-27 : Circuit level simulation program
** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California.
** Please get your ngspice manual from http://ngspice.sourceforge.net/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Tue Dec 26 17:10:20 UTC 2017
*****
```

```

ngspice 1 -> plot out vs in
ngspice 1 ->
x0 = 0.774138, y0 = 1.708882
x0 = 0.975862, y0 = 0.114706

```

Vih and vol
Find NMH and NMI

Power Supply Scaling

18 October 2025 18:04

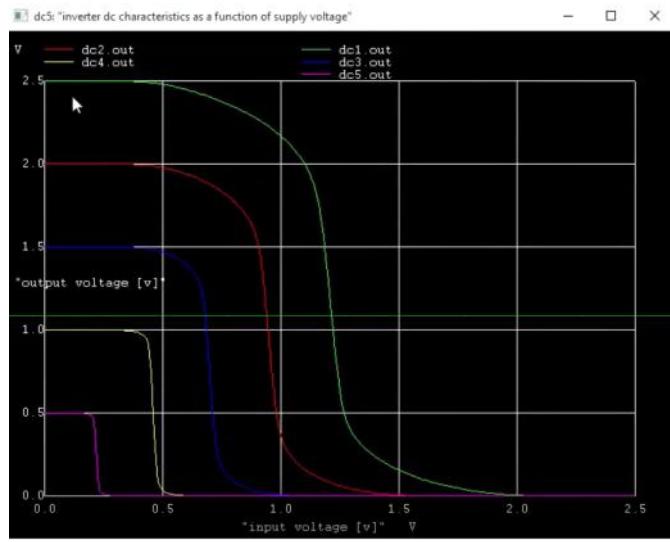
```
Vdd vdd 0 2.5
Vin in 0 2.5
```

```
.control
let powerSupply = 2.5
alter Vdd = powerSupply
```

```
let voltageSupplyVariation = 0
dowhile voltageSupplyVariation < 5
  dc Vin 0 2.5 0.01
  let powerSupply = powerSupply - 0.5
  alter Vdd = powerSupply
  let voltageSupplyVariation = voltageSupplyVariation + 1
end
```

VOLTAGE POWER SWEEP , BY USING Spice,

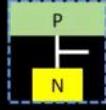
```
plot dc1.out vs in dc2.out vs in dc3.out vs in dc4.out vs in
dc5.out vs in xlabel "input voltage [V]" ylabel "output voltage
[V]" title "Inverter dc characteristics as a function of supply
voltage"
* quit
```



Static behavior Evaluation : CMOS inverter Robustness 3. Power Supply Scaling

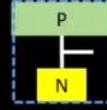
SPICE Simulation

Vdd = 2.5



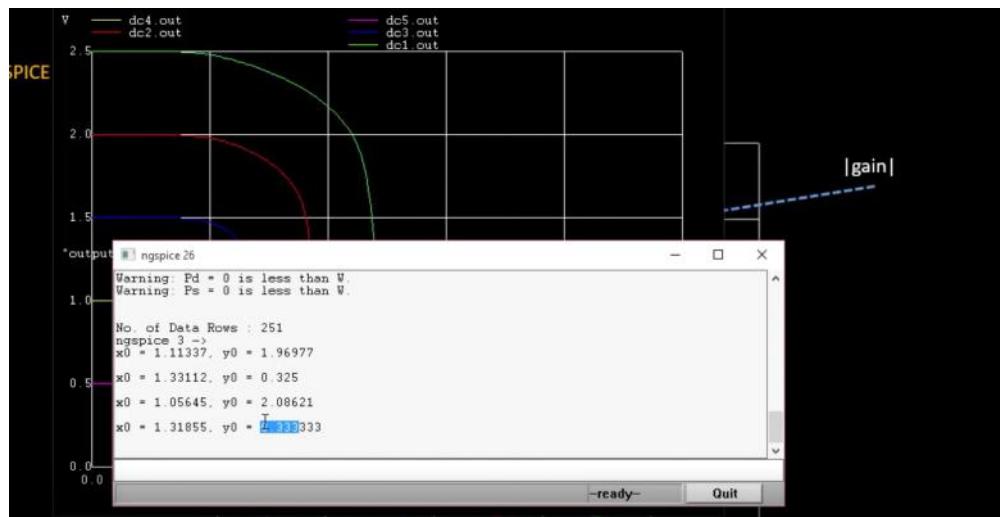
Wp = 0.9375u
Wn = 0.375u

Vdd = 1



Wp = 0.9375u
Wn = 0.375u

Vdd = 2.5V → 1V

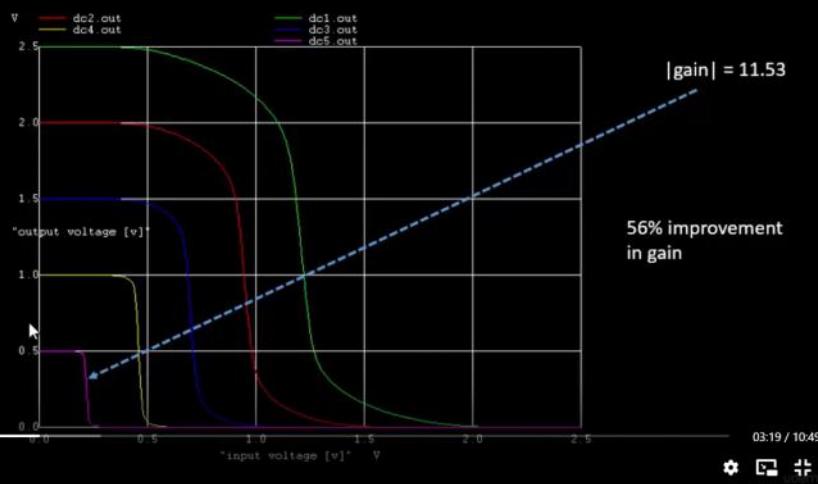


GAIN CHANGE , Change in output voltage vs change in input voltage .

Static behavior Evaluation : CMOS inverter Robustness

3. Power Supply Scaling

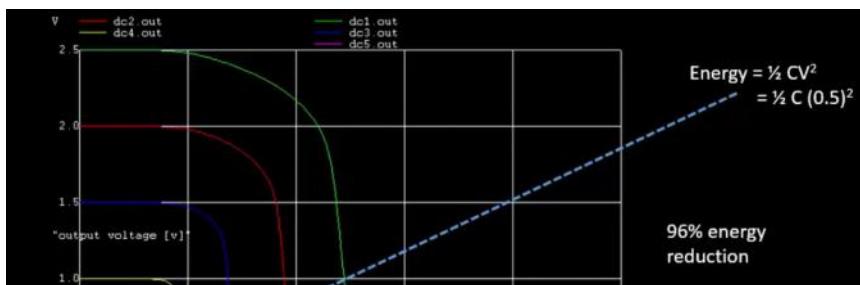
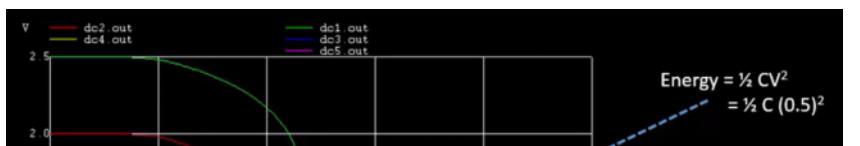
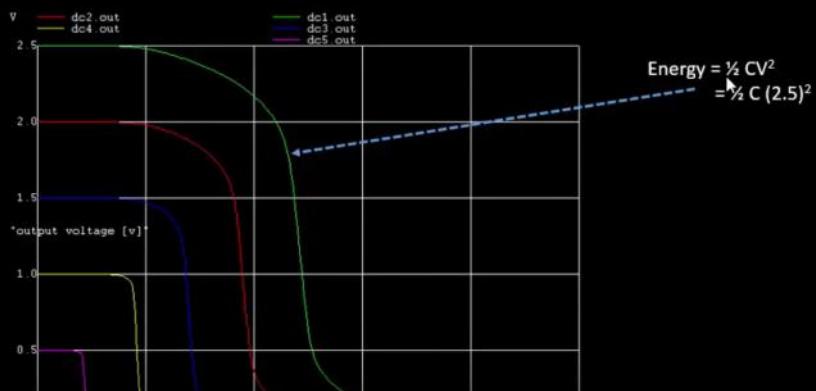
SPICE Simulation



Static behavior Evaluation : CMOS inverter Robustness

3. Power Supply Scaling

SPICE Simulation

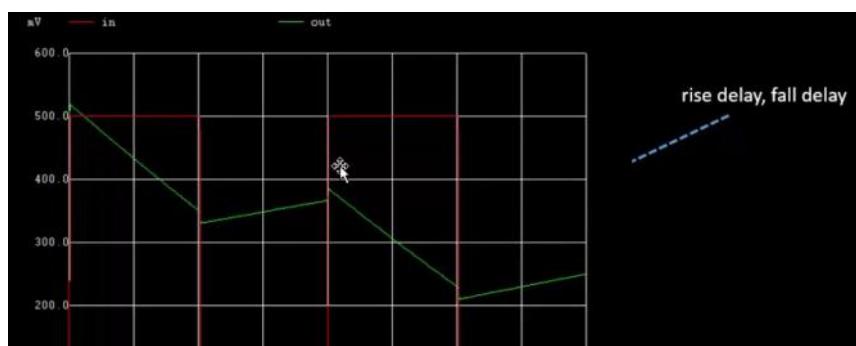
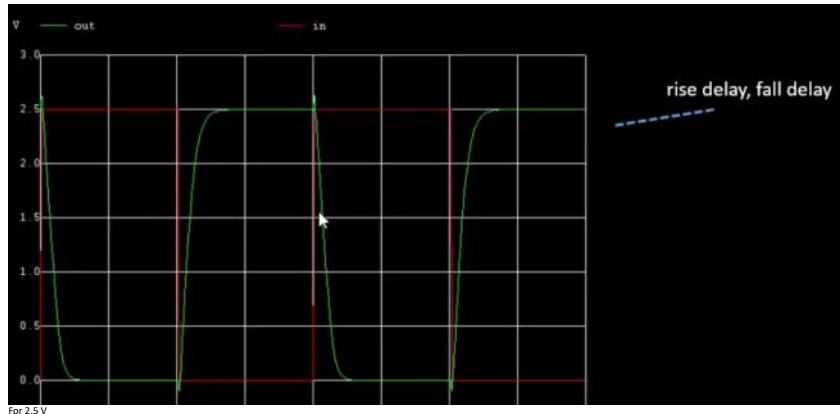


3. Power Supply Scaling

SPICE Simulation

Advantages of using 0.5V supply

1. Increase in gain (close to 50% improvement)
2. Significant reduction in energy (close to 90% improvement)



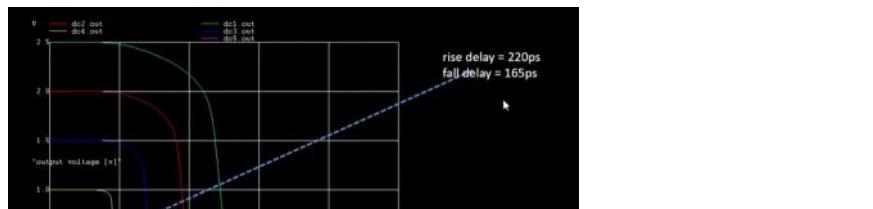
SPICE Simulation

Advantages of using 0.5V supply

1. Increase in gain (close to 50% improvement)
2. Significant reduction in energy (close to 90% improvement)

Disadvantages

1. Performance impact (Prime topic of discussion in next course “Circuit design and SPICE simulation - Dynamic”)



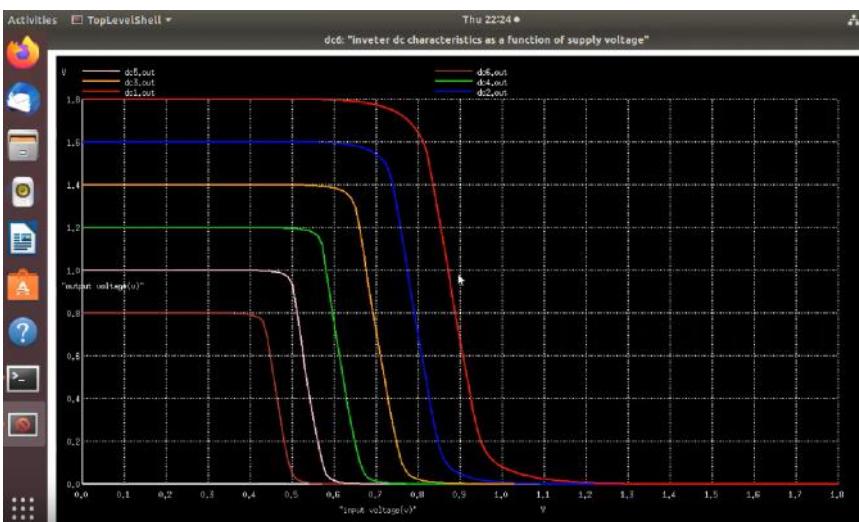
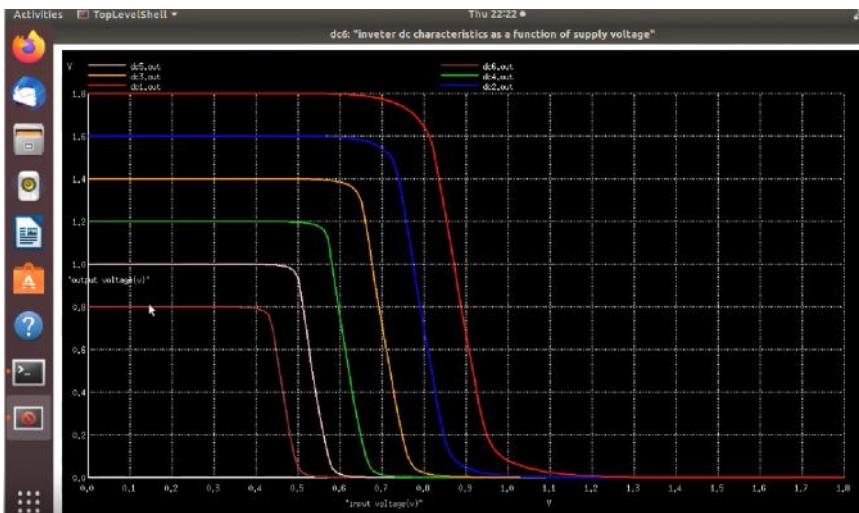
*Netlist Description

```

XH1 out in vdd vdd sky130_fd_pr_pfet_01v8 w=1 l=0.15
XH2 out in 0 0 sky130_fd_pr_nfet_01v8 w=0.36 l=0.15

Cload out 0 50fF
Vdd vdd 0 1.8V
Vin in 0 1.8V
.control
let powersupply = 1.8
alter Vdd = powersupply
  let voltagesupplyvariation = 0
    if voltagesupplyvariation < 0
      dc Vin 0 1.8 0.01
    let powersupply = powersupply - 0.2
    alter Vdd = powersupply
    let voltagesupplyvariation = voltagesupplyvariation + 1
  end
plot dc1.out vs in dc2.out vs in dc3.out vs in dc4.out vs in dc5.out vs in xlabel "input voltage(V)" ylabel "output voltage(V)" title "Inverter dc characteristics as a function of supply voltage"
.endc

```

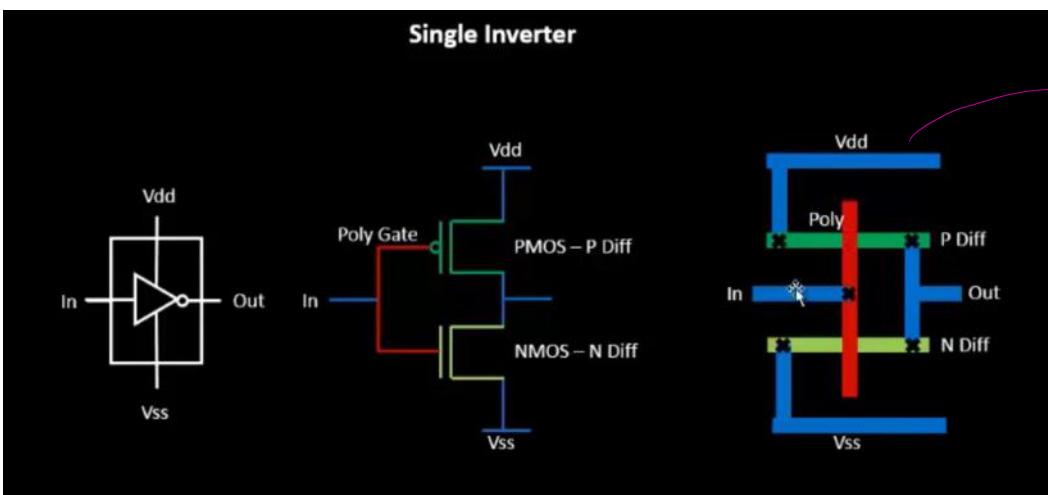


CMOS is least responsive to

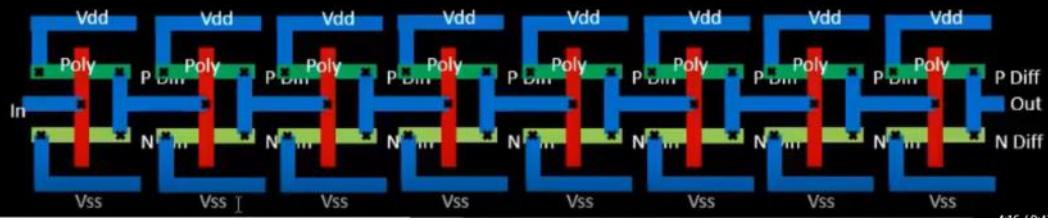
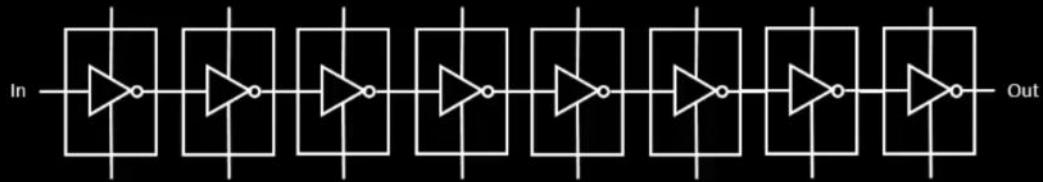
Device Variation

SOURCES OF VARIATION, Sources of Variation : Etching Process Variation

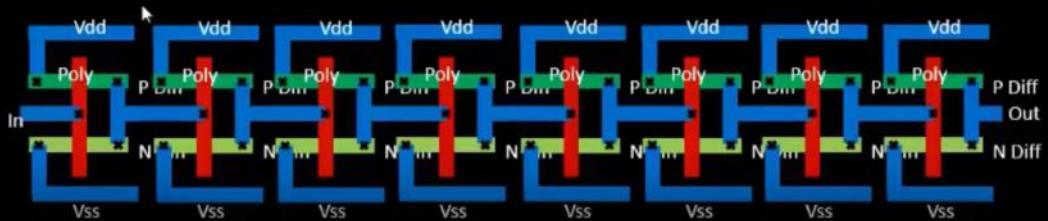
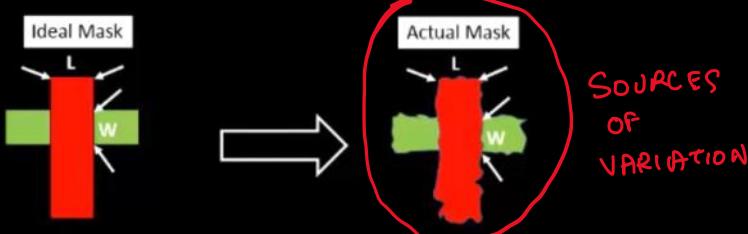
Etching
Oxide



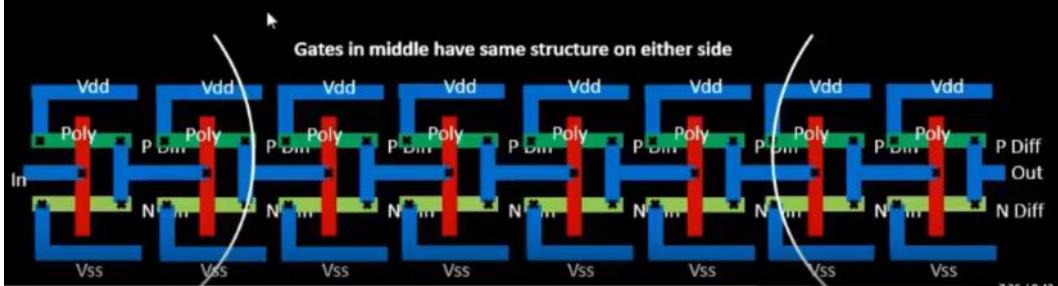
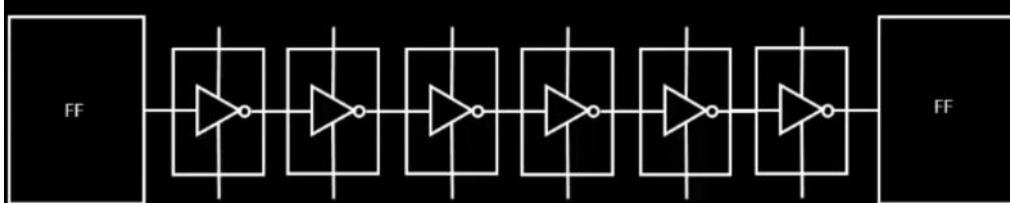
Inverter Chain



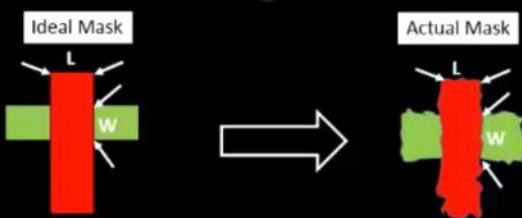
Inverter Chain



Inverter Chain



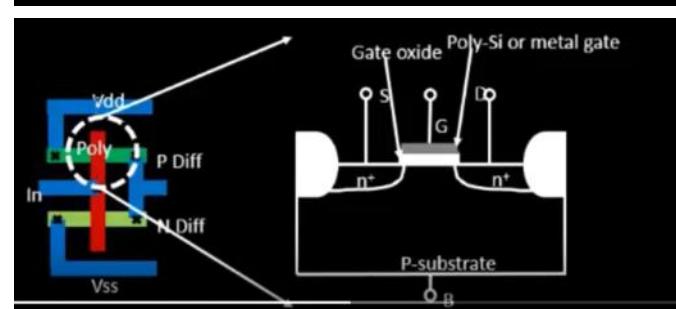
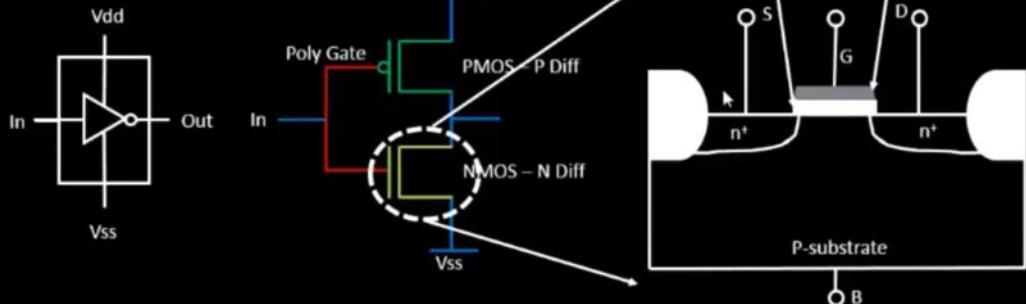
Inverter Chain

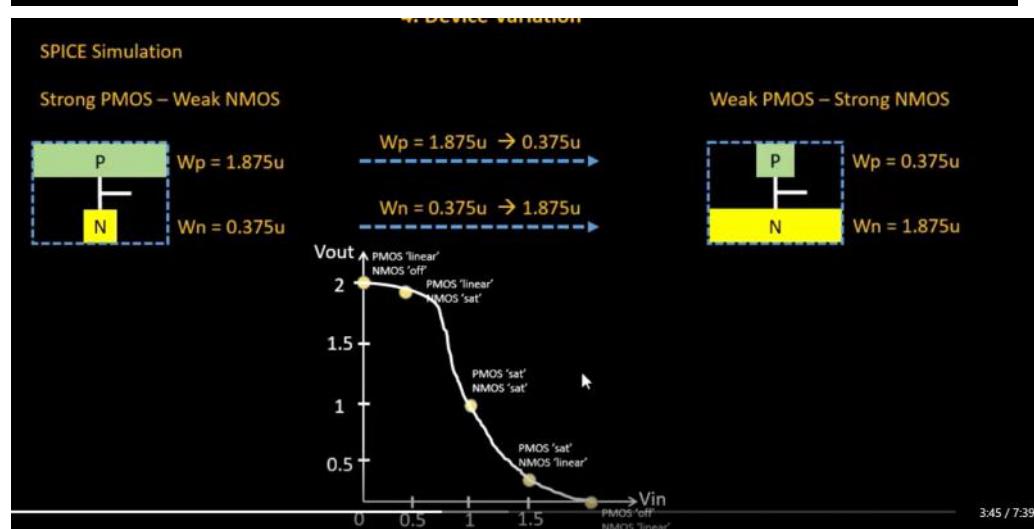
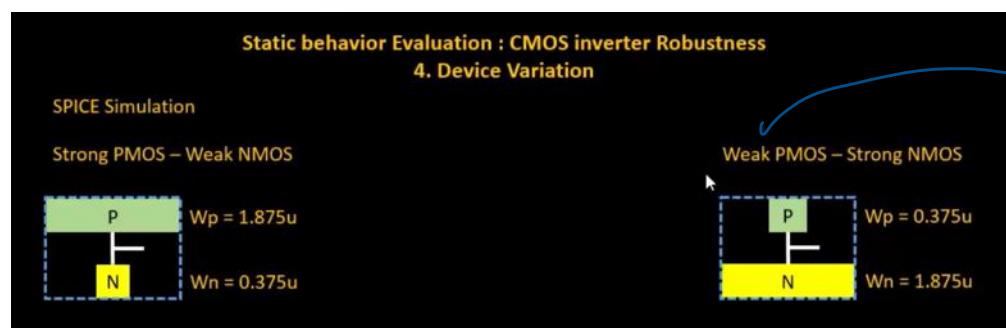
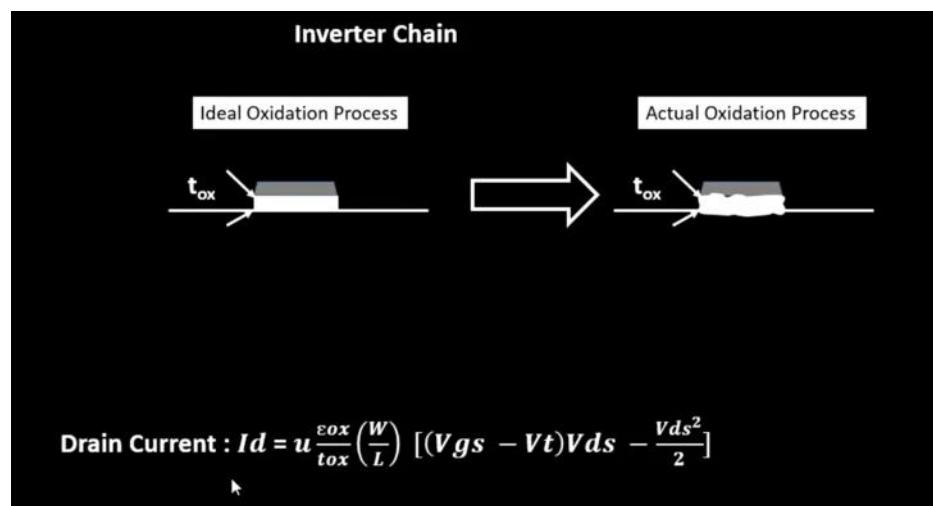
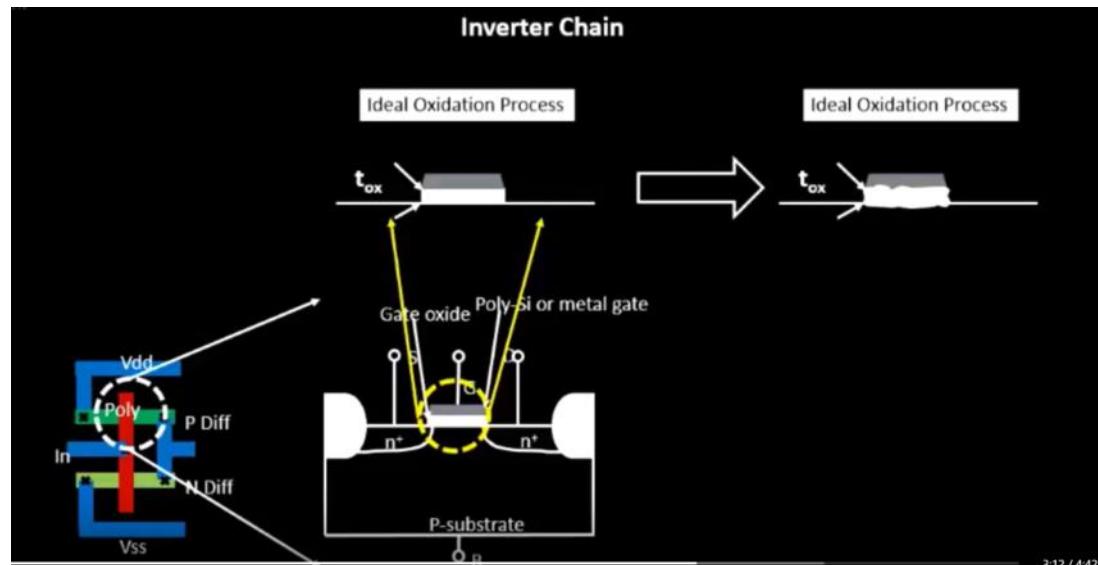


$$\text{Drain Current : } Id = u Cox \left(\frac{W}{L} \right) [(Vgs - Vt)Vds - \frac{Vds^2}{2}]$$

$$\text{Drain Current : } Id = u Cox \left(\frac{W}{L} \right) [(Vgs - Vt)Vds - \frac{Vds^2}{2}]$$

Single Inverter





```
alter M2 W = nmoswidth
let pmoswidth = 1.875u
alter M1 W = nmoswidth
```

```

0 0.5 1 1.5
FROM: 0.5
NOMOS width
343 / 733

alter M2 W = nmoswidth
let pmoswidth = 1.875u
alter M1 W = pmoswidth
let widthVariation = 0
dowhile widthVariation < 5
  echo "nmos width is $nmoswidth"
  echo "pmos width is $pmoswidth"
  do Vin 0 2.5 0.01
  let nmoswidth = nmoswidth + 0.375u
  let pmoswidth = pmoswidth - 0.375u
  alter @M2[W] = nmoswidth
  alter @M1[W] = pmoswidth
  let widthVariation = widthVariation + 1
end

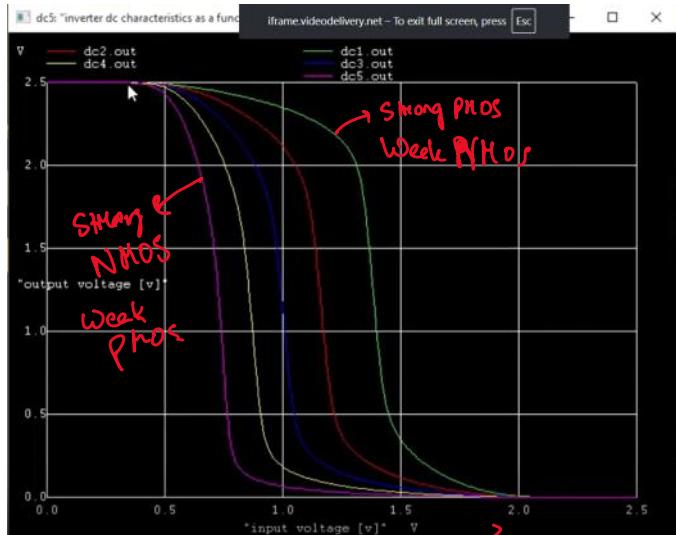
plot dc1.out vs in dc2.out vs in dc3.out vs in dc4.out vs in
5.out vs in xlabel "input voltage [V]" ylabel "output voltage
}" title "Inverter dc characteristics as a function of NMOS
width"
quit

```

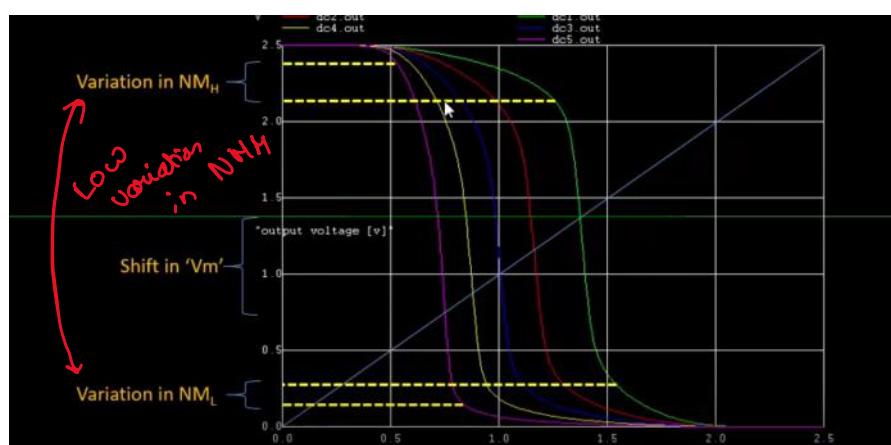
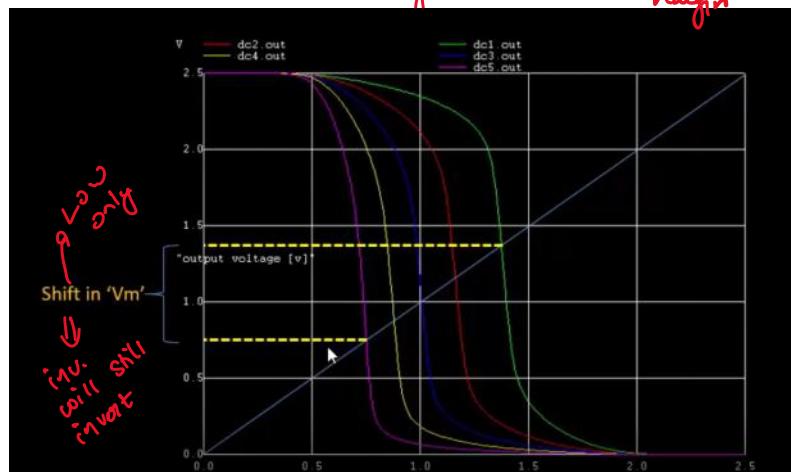
Device Variation Exp

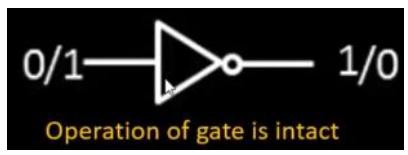
different Spice

simulation for different widths,



→ DC characteristics
→ switching threshold., Noise Margin





\Rightarrow Variation is intact
even after
different device variation

Device Variation Day 5

```

File Edit View Search Terminal Help
*Model Description
.param temp=27

*Including sky130 library files
.lib "sky130_fd_pr/models/sky130.lib.spice" tt

*Netlist Description

XH1 out in vdd vdd sky130_fd_pr__pfet_01v8 w=7 l=0.15
XH2 out in 0 0 sky130_fd_pr__nfet_01v8 w=0.42 l=0.15

Cload out 0 50fF
vdd vdd 0 1.8V
Vin in 0 1.8V

*simulation commands
.op
.dc Vin 0 1.8 0.01
.control
run
setplot dc1
display
.endc
.end

"day5_inv_devicevariation_wp7_wn042.spice" 3SL, 39iC

```

