

Lab Reports

Workshop on Semiconductor Technology

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This document contains the schedule and key activities and report conducted during the workshop.

Index

- **DATE: 16th December 2024**
 - Cleanroom: Safety Protocols and Wafer Cleaning
 - Lab: I-V Characteristics of Solar Cell
- **DATE: 17th December 2024**
 - CLEWIN tutorial for Mask Design
- **DATE: 18th December 2024**
 - Training Lecture on – Development & Future Trends of 3D-IC Packaging Technology
- **DATE: 19th December 2024**
 - Training Lecture on – Manufacturing processes of Advanced Nano Devices
- **DATE: 20th December 2024**
 - Training Lecture on –The trends of Advanced Heterogeneous Integration Packaging
- **DATE: 23rd December 2024**
 - Cleanroom:
 - * E1: Dry film resist patterning for making molds
 - * E2: Using molds to make multilayer devices
- **DATE: 24th December 2024**
 - Cleanroom:
 - * E1: SOP (Standard Operating Procedure) of Mask Aligner and sample preparation
 - * E2: Sample exposure, development, and inspection
 - * E3: CVD process for making Graphene and Plasma Generator
 - Lab:
 - * Hands-on with Vacuum fittings, MFCs, pump, and chamber
- **DATE: 25th December 2024 (Extra Session)**
 - Cleanroom:
 - * E1: Wafer Cleaning + Lithography (Designed new pattern of IDE electrodes for Gas sensor)
- **DATE: 26th December 2024**
 - Cleanroom:
 - * E1: Sputtering (DC)
 - * E2: EUV
 - * E3: Lift Off process
- **DATE: 27th December 2024**
 - Cleanroom: E-Beam Lithography
 - E1: SEM
 - E2: TEM
 - E3: XRD
- **DATE: 28th December 2024**
 - T-Matrix Simulation
 - Ellipsometry
 - Oxidation
- **DATE: 30th December 2024**
 - Cleanroom: Reactive-Ion Etching (RIE)
 - MOS-CAP C/V Characteristics
 - Fourier Optics Demonstration

1 Lab: I-V Characteristics of Solar Cell

1.1 Aim

To measure the dark and light I-V characteristics of a solar cell using a DC voltage source, multimeter, and series resistor, and to determine important parameters such as open-circuit voltage (V_{oc}), short-circuit current (I_{sc}), fill factor, and efficiency.

1.2 Theory

A solar cell is a semiconductor device that converts light energy into electrical energy through the photovoltaic effect. When light strikes the solar cell, it generates electron-hole pairs, creating a current when connected in a circuit. The I-V characteristics of a solar cell are crucial for understanding its performance.

Under dark conditions, the solar cell behaves like a diode, with its current primarily determined by the applied voltage. Under illumination, the solar cell generates a photocurrent, shifting the I-V curve to the fourth quadrant, where power can be extracted. Key parameters include the open-circuit voltage (V_{oc}), which is the maximum voltage at zero current; the short-circuit current (I_{sc}), the maximum current at zero voltage; and the fill factor (FF), which indicates the quality of the solar cell. Efficiency (η) is the ratio of the maximum electrical power output to the input light power.

To prevent excessive current that might damage the solar cell or measuring instruments, a $1\text{ k}\Omega$ resistor is included in series with the circuit.

Filling Factor of a Solar Cell The filling factor (FF) is defined to be:

$$\text{FF} = \frac{P_{\max}}{I_{SC}V_{OC}}$$

which represents an important parameter used to evaluate the quality of the solar cell.

1.3 Procedure

The solar cell is connected in series with a $1\text{ k}\Omega$ resistor, and the circuit is powered by a DC voltage source. A multimeter is used to measure the voltage across the solar cell and the current through the circuit. The experiment is conducted in two phases:

1. **Dark I-V Measurements:** The solar cell is shielded from light, and the DC voltage is varied from -2 V to +2 V in small increments. At each step, the current and voltage are recorded.

2. **Light I-V Measurements:** The solar cell is illuminated with a uniform light source. The same voltage variation is applied, and the corresponding current and voltage values are measured.

The observations are used to plot I-V curves and extract key parameters such as V_{oc} , I_{sc} , and P_{\max} , which are used to calculate the fill factor and efficiency.

1.4 Circuit Diagram

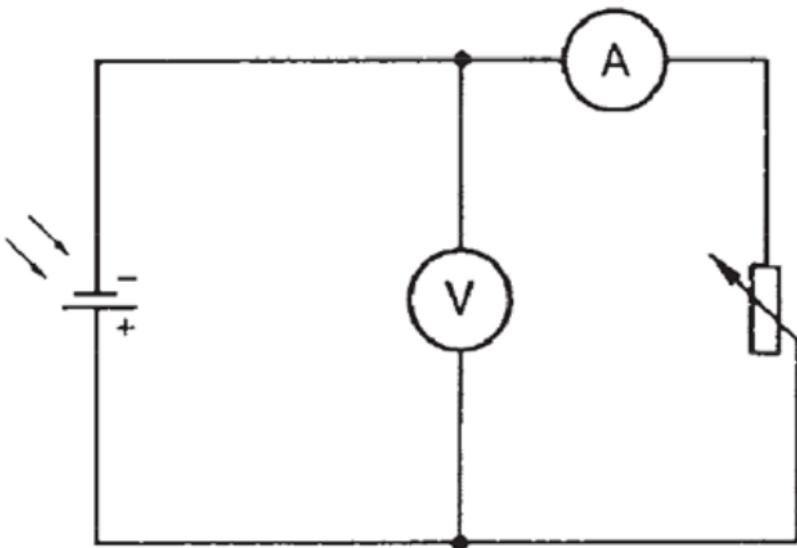


Figure 1: Schematic of the experimental setup.

1.5 Observations Table

Voltage (V)	Current (mA)	Voltage (V)	Current (mA)
-0.7	-350	-0.7	-400
-0.6	-320	-0.6	-400
-0.5	-290	-0.5	-400
-0.4	-260	-0.4	-400
-0.3	-240	-0.3	-400
-0.2	-220	-0.2	-380
-0.1	-200	-0.1	-350
0.0	-180	0.0	-300
0.1	-160	0.1	-250
0.2	-140	0.2	-200
0.3	-120	0.3	0
0.4	-100	0.4	100
0.5	-80	0.5	200
0.6	-60	0.6	300
0.7	-40	0.7	350
0.8	-20	0.8	370
0.9	0	0.9	400
1.0	10	1.0	450
1.1	20	1.1	500
1.2	30	1.2	550
1.3	40	1.3	600
1.4	50	1.4	650
1.5	60	1.5	700
1.6	70	1.6	750
1.7	80	1.7	800
1.8	90	1.8	850
1.9	100	1.9	900
2.0	110	2.0	950
2.1	120	2.1	1000
2.2	130	2.2	1050
2.3	140	2.3	1100
2.4	150	2.4	1150
2.5	160	2.5	1200
2.6	170	2.6	1250
2.7	180	2.7	1300
2.8	190	2.8	1350
2.9	200	2.9	1400
3.0	210	3.0	1450

(a) Dark I-V measurements.

(b) Light I-V measurements.

Table 1: Observation Tables: Dark and Light I-V Measurements.

1.6 Plots

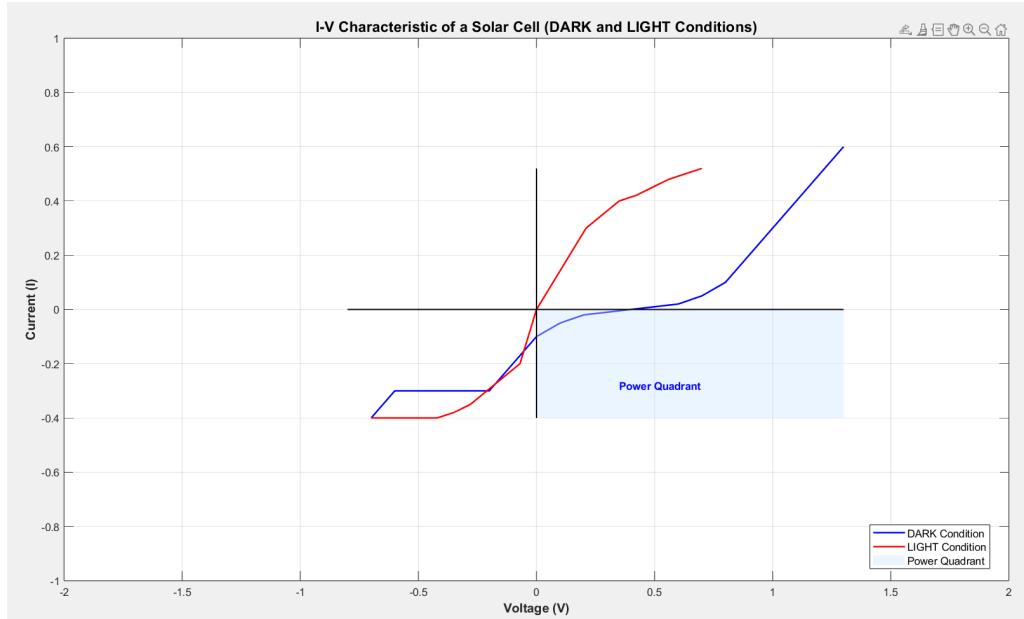


Figure 2: Schematic of the experimental results.

1.7 Conclusion

The experiment successfully measured the I-V characteristics of the solar cell under dark and illuminated conditions. The parameters V_{oc} and I_{sc} were determined, and the fill factor and efficiency were calculated. These values provide insight into the performance and quality of the solar cell. Minor discrepancies in results could be attributed to variations in light intensity, contact resistance, or measurement precision.

2 Conclusion for Day 1 : Training Lecture on – Development Future Trends of 3D-IC Packaging Technology

In this section, we explored advanced semiconductor packaging concepts, including Wafer-Level Packaging (WLP), Panel-Level Packaging (PLP), and their comparisons, as well as reliability testing for substrates. We discussed techniques like underfilling flip chips, System-in-Package (SCM) versus Multi-Chip Module (MCM) architectures, and homogeneous versus heterogeneous packaging. Signal routing strategies with logical switches at the chip and interposer levels were highlighted alongside the transition from Through-Silicon Via (TSV) to Non-Through Interposers (NTI).

Finally, NVIDIA's contributions to AI computation and packaging innovations, such as NVIDIA NIM and Project Ceiba, underline the intersection of semiconductor technology with AI advancement. These developments signify the industry's ongoing drive toward more efficient, scalable, and cost-effective solutions.

3 Conclusion for Day 2 : – Manufacturing processes of Advanced Nano Devices

- Integrated Circuit (IC) fabrication involves wafer preparation, fabrication, testing, assembly, and final testing.
- Key trends in semiconductor manufacturing include increased performance, reduced chip prices, and smaller feature sizes (from 350nm to 1-2nm).
- Devices are classified as micrometre and nanometer devices.
- Technological advancements are guided by Moore's Law, with wafer sizes increasing from 50mm to 300mm over time.
- FinFETs are 3D transistors that overcome the limitations of planar MOSFETs at the nanoscale.
- The advantages of FinFETs include reduced current leakage, improved power efficiency, and faster switching speeds.
- The FinFET fabrication process includes substrate preparation, fin formation, and chemical-mechanical planarization (CMP).
- Yield, price, equipment limitations, and competition are crucial factors in semiconductor manufacturing for cost-effectiveness and innovation.
- Precision, patience, and teamwork are key for success in the semiconductor industry.
- 2nm technology faces yield challenges, making larger nodes more practical for mass production.
- Silicon is purified from sand and grown into single crystals through the Czochralski process for semiconductor use.
- Oxidation forms SiO_2 , which acts as an insulator and dielectric material in MOSFETs.
- Dry oxidation provides better electrical characteristics compared to wet oxidation.
- Lithography is a critical process that involves patterning, photomasks, light spectrum control, and resolution management.
- The lithography process has evolved from traditional methods to advanced techniques such as immersion lithography, which uses liquid between the lens and wafer to improve resolution.
- Lithography technologies such as DUV, EUV, and E-beam lithography are compared based on parameters like resolution, mask patterns, cost, and applications.
- Thin film deposition techniques, such as Physical Vapor Deposition (PVD) and Chemical Vapor Deposition (CVD), are compared based on process conditions, temperature, surface coverage, and material flexibility.
- Plasma, as the fourth state of matter, is used in processes like PECVD, sputtering, and etching, with DC and RF plasma variations providing different characteristics.

The second day covered essential aspects of semiconductor manufacturing, focusing on the stages from wafer production to advanced lithographic techniques. FinFETs significantly improve transistor performance, while immersion and EUV lithography enhance miniaturization capabilities. Yield, precision, and cost-effectiveness remain vital, and emerging technologies such as Gate-All-Around FETs (GAAFETs) and improved deposition methods are driving future innovation. These advancements ensure the semiconductor industry can continue meeting the increasing demands of modern electronics.

4 Conclusion for Day 3 : –The trends of Advanced Heterogeneous Integration Packaging

1. **Trends in Advanced Packaging Technology Development:** Advanced packaging technologies are evolving to meet the demand for higher performance, miniaturization, and integration. Key trends include heterogeneous integration, 3D packaging, and system-on-package designs. These innovations enable the integration of diverse components like processors, memory, and sensors into compact, high-performance platforms.
2. **Driving Forces for Heterogeneous Integration:** The demand for multifunctionality, reduced power consumption, and compact form factors drives heterogeneous integration. This approach integrates various components into a single platform, enhancing system efficiency and functionality.
3. **Thermal and Mechanical Stress Management:** Thermal management is critical for maintaining reliability and performance. Effective packaging designs address heat dissipation through materials and structures, ensuring system stability and reducing risks like cracking or delamination. Reliability testing under various conditions validates long-term operational stability.
4. **Wafer Level Chip Scale Package (WLCSP):** WLCSP offers extreme miniaturization and integrates semiconductor devices directly onto a wafer, eliminating traditional substrates. This reduces size, increases performance, and enhances both thermal and electrical performance, making it ideal for mobile, automotive, and IoT applications.
5. **Integrated Circuit Fabrication Technologies:** The evolution from 2D to 3D IC technologies has improved performance, reduced power consumption, and minimized form factors. 2.5D and 3D ICs provide pathways for enhanced multi-die integration, addressing challenges such as heat dissipation and manufacturing complexity.
6. **Advanced Semiconductor Packaging: 2.5D vs. EMIB:** Both 2.5D Interposer and EMIB enable high-density integration but differ in design, cost, and thermal management. EMIB offers localized high-density connections with reduced manufacturing complexity compared to traditional 2.5D approaches.
7. **Thermal Management Techniques:** Effective thermal management is achieved through passive and active heatsinks, and advanced packaging technologies like Fan-Out Wafer-Level Packaging (FOWLP) that enhance heat dissipation. Thermal stress management, along with strategies like thermal cycling and vibration tests, ensures reliability in semiconductor packaging.
8. **Semiconductor Outlook for 2025 - Hsinchu Science Park:** Hsinchu Science Park continues to lead Taiwan's semiconductor industry with a focus on innovation, collaboration between academia and industry, and advancements in technology such as AI-driven semiconductor processes and regional supply chain development.

5 Lab Report: Soft Lithography

To understand and execute the steps involved in soft lithography for microfabrication, emphasising the fabrication of patterns using photolithography and soft lithography processes.

5.1 Materials and Equipment

1. **Photoresists:** Positive (e.g., S1813) and negative resists
2. **Substrate:** Silicon wafer or glass slides
3. **Mask:** Chrome-coated glass slide with the desired pattern
4. **Spin coater**
5. **UV Light Source:** For photolithography
6. **Developer:** Acetone or other suitable developer solutions
7. **PDMS (Polydimethylsiloxane):** Transparent elastomer
8. **Plasma Treatment Device:** For bonding PDMS to substrates
9. **Dry Film Resist (DFR):** Negative resist
10. **Chrome Etchant (CR + BR)**
11. **Tools:** Punch tools, curing oven, laminator

5.2 Procedure

5.2.1 Step 1: Design of the Pattern

- The design of the microfabrication pattern was created using CAD tools. This design was transferred to a chrome-coated glass slide (mask) through claviation or GTSP methods.

5.2.2 Step 2: Preparation of Substrate

- The silicon wafer or glass substrate was cleaned thoroughly.
- Spin coating of S1813 photoresist was performed to create a uniform layer on the substrate. The thickness of the resist was determined by spin speed and time.

5.2.3 Step 3: Photolithography

1. Mask Alignment and Exposure:

- The chrome-coated mask with the pattern was aligned on top of the substrate.
- The substrate was exposed to UV light. Depending on the process, the photoresist can be positive or negative:
 - *Positive Resist:* Areas exposed to UV light become soluble.
 - *Negative Resist:* Areas exposed to UV light polymerize and become insoluble.

2. Development:

- The substrate was immersed in a developer solution to remove unwanted areas of the resist.
- An acetone wash was used to remove residuals.

3. Etching:

- Chrome etchant (CR + BR) was applied to remove the unprotected chrome layer on the mask.
- The mask was then cleaned to reveal the patterned substrate.

5.2.4 Step 4: Soft Lithography with PDMS

1. Casting PDMS:

- PDMS prepolymer and curing agent were mixed in a 10:1 ratio and degassed to remove air bubbles.
- The mixture was poured over the patterned substrate and cured in an oven to solidify.

2. Peeling and Punching:

- Once cured, the PDMS layer was carefully peeled off from the substrate.
- Channels and features in the PDMS layer were punched to prepare fluidic inlets and outlets.

3. Bonding:

- The PDMS channel was plasma-treated to enhance bonding.
- The treated PDMS was bonded to a glass slide to form a microfluidic device.

5.2.5 Step 5: DFR-based Lithography

- Dry Film Resist (DFR) was used as a negative resist. It was laminated onto the substrate and exposed to UV light through the mask.
- The development time was optimized to achieve precise patterns.

5.2.6 Step 6: Finalization

- PDMS was solidified and prepared for further applications. The final microstructures were validated for uniformity, precision, and bonding quality.

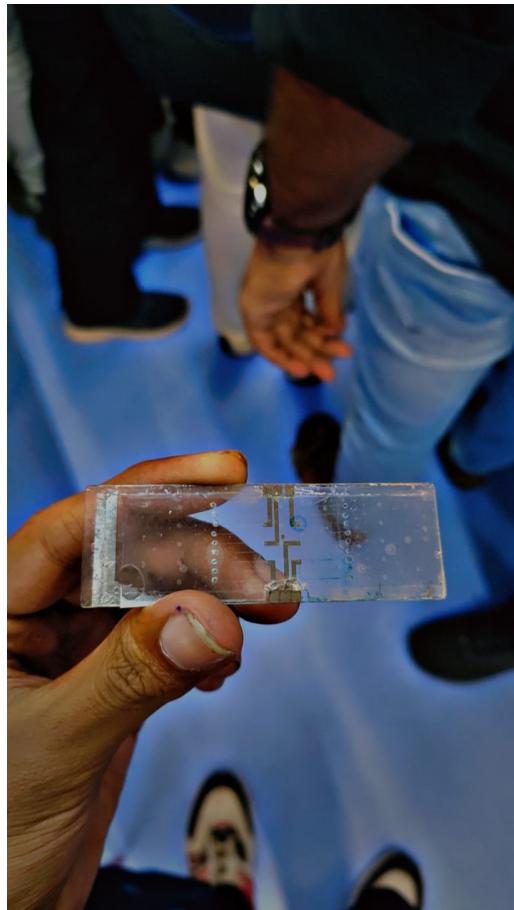


Figure 3: PDMS bonded glass substrate

5.3 Observations

1. Dry Film Resist:

- Easy to handle and laminate onto flat surfaces.
- Uniformity issues and edge bead formation observed on larger substrates.

2. PDMS:

- Transparent and biocompatible.
- Conductivity can be introduced by mixing alloys.

5.4 Results

- Successfully fabricated microfluidic channels with a height determined by the thickness of the photoresist.
- Developed uniform PDMS layers bonded to glass substrates with plasma treatment.

5.5 Conclusion

Soft lithography provides a versatile and effective method for fabricating microfluidic devices. The process's success depends on accurate photolithography and optimized PDMS handling.

6 Lab Report: Wafer Cleaning Process

6.1 Aim

To clean silicon wafers effectively by removing organic matter, particles, and metallic contaminants, preparing them for spin coating.

6.2 Objective

- To ensure the silicon wafer surface is free of contaminants.
- To create a hydrophilic surface suitable for subsequent processes.
- To protect the wafer from contamination using passivation layers.

6.3 Materials Required

1. Personal protective equipment (PPE):

- Shoe covers
- Bunny suits
- Head covers
- Gloves

2. Cleanroom with laminar airflow setup

3. Chemicals:

- Ammonium hydroxide
- Hydrogen peroxide
- Hydrochloric acid
- Sulfuric acid
- Deionized water

4. Quartz tanks (heated)

5. Nitrogen gas blower

6.4 Steps to Follow

6.4.1 Preparation

1. Wear PPE in the following order: shoe covers, bunny suits, head cover, and gloves.
2. Enter the cleanroom and remain under the laminar airflow for 10–15 seconds to remove any surface contaminants.

6.4.2 Wafer Cleaning Procedure

1. Step A: SC1 Cleaning

- Prepare the APM solution (ammonium hydroxide-hydrogen peroxide-water).
- Use this solution to remove organic matter and particles from the silicon wafer surface.

2. Step B: SC2 Cleaning

- Prepare the HPM solution (6 parts deionized water, 1 part hydrochloric acid, 1 part hydrogen peroxide).
- Use this solution to remove metallic contaminants left after SC1 cleaning.
- Allow the process to form a thin passivation layer that protects the wafer from contamination.

3. Step C: Piranha Etch Cleaning

- Prepare the Piranha solution (3 parts sulfuric acid to 1 part hydrogen peroxide).
- Use the solution to remove residual organic materials.
- **Note:** Perform this step in heated quartz tanks and handle the solution with care due to its highly corrosive nature.

6.4.3 Post-Cleaning Procedure

1. Blow nitrogen gas through the blower to remove any remaining droplets from the wafer surface.
2. Ensure the wafer is dry and clean, ready for spin coating.

6.5 Conclusion

The wafer cleaning process ensures the removal of contaminants and prepares the silicon wafer with a hydrophilic surface for subsequent processes like spin coating. Each step, SC1, SC2, and Piranha etch, contributes to thorough cleaning and passivation of the wafer surface. Proper handling and adherence to protocols ensure safety and efficiency.

7 Lab Report: Spin Coating Process

7.1 Aim

To uniformly coat a silicon wafer with photoresist using the spin coating method and achieve the desired resist thickness.

7.2 Objective

- To apply a uniform layer of photoresist on the silicon wafer.
- To control the thickness of the photoresist based on process requirements.
- To prepare the wafer for subsequent lithography processes.

7.3 Materials Required

1. Cleaned silicon wafer
2. Oven or hot plate (set to ~110°C)
3. Spin coater
4. Positive photoresist (e.g., S1813)
5. Graph for resist thickness vs. rpm
6. Timer

7.4 Steps to Follow

7.4.1 Preparation

1. Bake the Wafer:

- Heat the cleaned silicon wafer at ~110°C to remove any remaining liquid droplets.

7.4.2 Spin Coating Procedure

1. Photoresist Application:

- Place the baked wafer in the spin coater.
- Pour droplets of S1813 positive photoresist onto the wafer surface.

2. Set Spin Parameters:

- Refer to the provided graph to determine the rpm required for the desired photoresist thickness.

3. Spin Coating Process:

- **Part A:** Spin the wafer at ~500 rpm for the first 5 seconds to evenly distribute the photoresist.
- **Part B:** Increase the rpm and spin for 50–55 seconds to achieve the desired resist thickness.

4. Result:

- Remove the wafer with the desired thickness of photoresist, ensuring it is ready for further processing.

7.5 Conclusion

Spin coating provides a controlled and uniform photoresist layer on silicon wafers. By adjusting the spin speed and time, the desired thickness is achieved, preparing the wafer for subsequent laser writing step.

8 Lab Report: Chemical Vapour Deposition

8.1 Aim

To study the theoretical aspects and practical implementation of Chemical Vapor Deposition (CVD) in a laboratory setup, with a focus on observing the operation of the CVD chamber controlled by Raspberry Pi and associated equipment.

8.2 Theory

Chemical Vapor Deposition (CVD) is a widely used method for depositing thin films and coatings by chemically reacting gaseous precursors in a reaction chamber. The process involves several interconnected phenomena such as fluid flow, diffusion, gas-phase nucleation, product desorption, surface reactions, and flame growth. Below is a comprehensive explanation of the key aspects and equipment involved in CVD, as well as specific details about graphene synthesis using CVD.

8.2.1 Main Aspects of CVD

Deposition by “surface-mediated reaction of adsorbed precursors from the gas phase”

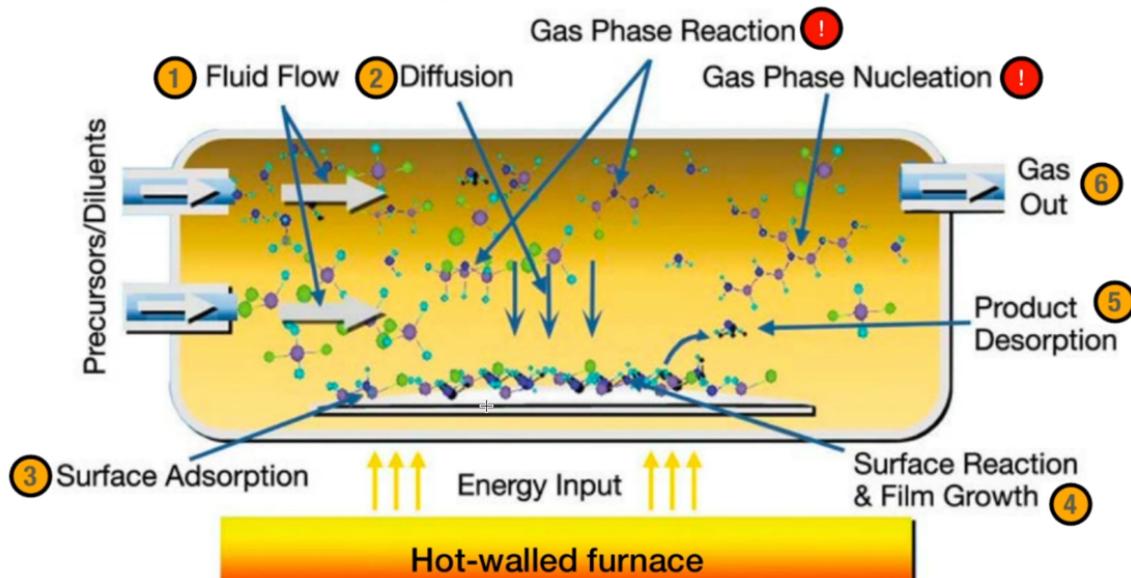


Figure 4: CVD Process Flow

1. Fluid Flow:

- Ensures the uniform distribution of reactant gases in the chamber.
- Laminar flow is preferred for precise deposition control.

2. Diffusion:

- **Gas-phase Diffusion:** Movement of gaseous precursors within the chamber to the substrate.
- **Surface Diffusion:** Migration of adsorbed species on the substrate surface, critical for uniform growth.

3. Energy Input:

- Energy (thermal, plasma, etc.) increases reaction rates and diffusion. Hot-wall furnaces provide uniform heating to enhance these processes.

4. Undesirable Gas-phase Nucleation:

- Formation of unwanted particles in the gas phase reduces coating quality. Minimizing gas-phase nucleation ensures uniform and defect-free deposition.

8.2.2 CVD Equipment

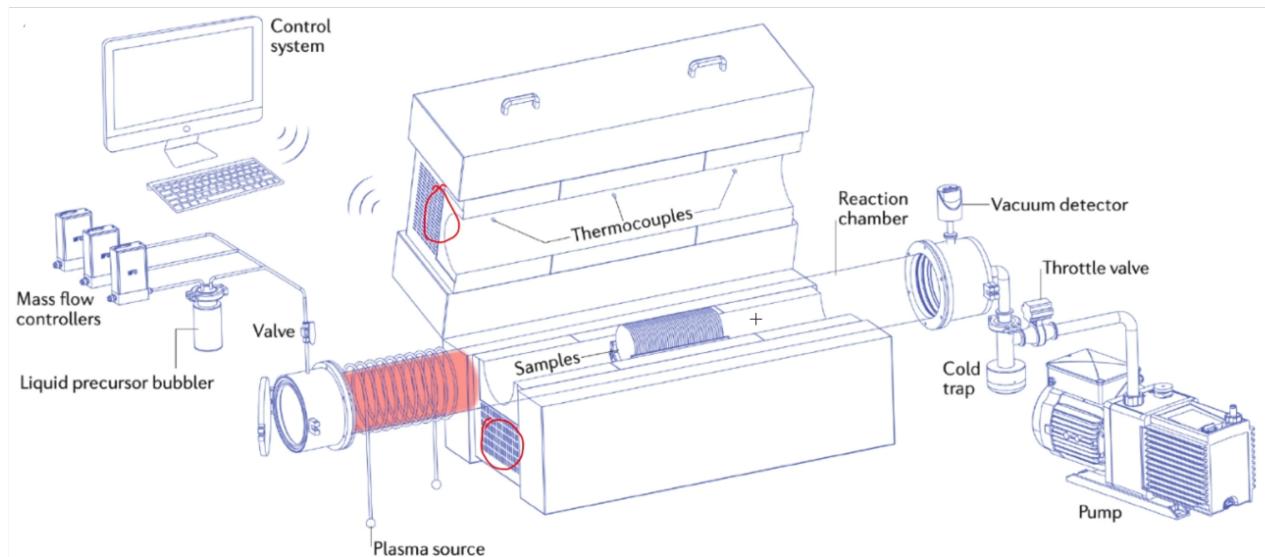


Figure 5: CVD Equipment

1. **Mass Flow Controllers (MFCs):** Regulate the flow rate of gaseous precursors with high precision.
2. **Liquid Precursor Bubbler:** Converts liquid precursors into vapors for the reaction process.
3. **Valves:** Control the flow and isolation of gases.
4. **Plasma Source:** Used in plasma-enhanced CVD (PECVD) to provide energy for reactions.
5. **Thermocouples:** Measure and control the temperature inside the chamber.
6. **Reaction Chamber:** The central area where deposition occurs, designed to maintain a controlled environment.
7. **Vacuum System:** Includes rotary pumps, vacuum gauges, and throttle valves to achieve and maintain low pressure.
8. **Cold Trap:** Captures unwanted by-products and particulates, protecting the vacuum system.

8.2.3 Types of CVD Processes

1. **Low-Pressure CVD (LPCVD):** Operates under low pressure, reducing gas-phase collisions and enhancing film uniformity.
2. **Plasma-Enhanced CVD (PECVD):** Utilizes plasma to reduce the thermal budget, enabling deposition at lower temperatures without damaging substrates.
3. **Pulsed CVD:** Delivers precursors in pulses, improving control over film composition and thickness.
4. **Applications in CNT and Pyrolytic Carbon:**
 - **CNT:** Facilitates carbon nanotube growth.
 - **Pyrolytic Carbon:** Produces coatings with high thermal and chemical resistance.

8.2.4 Graphene Synthesis via CVD

1. Process Steps:

- **Heating:** Substrate is heated to 1000°C to prepare for reaction.
- **Annealing:** Removes impurities and ensures a clean surface.
- **Growth:** Precursors decompose and carbon atoms adsorb on the substrate.
- **Cooling:** Controlled cooling solidifies graphene layers.

2. Control Parameters:

- **Temperature:** Higher temperatures enhance growth rates.
- **Pressure:** Uniform graphene is achieved at specific pressures (e.g., 0.6 Torr).
- **Cooling Rate:** Rapid cooling precipitates carbon, enabling controlled deposition.

3. Graphene Growth on Metals:

- Carbon dissolves into metals (e.g., Cu, Ni) at high temperatures and precipitates during cooling, forming graphene layers. Cu is preferred for single-layer growth due to limited carbon solubility.

4. **Uniform Growth:** Achieved by optimizing temperature, precursor flow rates, and cooling rates. Patterns can be pre-etched with photoresist to guide growth.

5. **Raman Spectroscopy:** Analyzes graphene quality, revealing SP2 bonding and layer uniformity.

8.2.5 CVD and SiO₂ Wafers

Deposition directly onto SiO₂ wafers is possible, enabling integration into electronic devices. Pre-patterning helps in localized growth and device fabrication.

8.2.6 Graphene Phase Diagram and Control

Growth increases with higher temperatures and precursor concentrations. To achieve specific morphologies, cooling parameters and substrate interactions are carefully controlled.

8.2.7 Shape and Nucleation Control

Increasing H₂ pressure and reducing grain sizes transition nucleation from random patterns to uniform hexagons.

8.2.8 Conclusion

CVD is a versatile technique with applications ranging from electronics to materials science. By controlling process parameters like temperature, pressure, and precursor flow, uniform and defect-free thin films can be achieved. The synthesis of graphene highlights the precision and adaptability of CVD, making it essential for advanced technological developments.

8.3 Practical Observations

In the CVD lab, we observed the following:

1. **CVD Chamber:** The chamber was controlled using a Raspberry Pi, ensuring precise monitoring and adjustments.
2. **Gas Inflows:** Mass Flow Controllers (MFCs) regulated the gas flow rates accurately.
3. **Temperature Control:** Thermocouples maintained the required temperature within the reaction chamber.
4. **Vacuum System:** Ensured low-pressure conditions, critical for uniform deposition.
5. **Cold Trap:** Collected by-products to protect the vacuum system.
6. **Other Equipment:** Included plasma sources and liquid precursor bubblers for specific deposition processes.

8.4 Learnings

- Understanding the importance of controlling parameters like temperature, pressure, and precursor flow for uniform deposition.
- Observing the practical integration of modern tools like Raspberry Pi for automation.
- Gaining insights into equipment functionality, such as MFCs, thermocouples, and cold traps.
- Realizing the significance of minimizing gas-phase nucleation to avoid defects.

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9 Lab Report: Photolithography Using Laser Writer

9.1 Aim

To create micro-patterns on a silicon wafer using a laser writer for the fabrication of Transfer Length Method (TLM) pads and Interdigitated Electrodes (IDE).

9.2 Objective

- To use photolithography to engrave specific designs onto the silicon wafer.
- To prepare patterns for calculating contact resistance (TLM) and gas detection (IDE).

9.3 Materials Required

1. Spin-coated silicon wafer
2. Oven or hot plate (set to 110 °C)
3. Spin coater and acetone solution (for cleaning)
4. Laser writer with lens 3 (Gallium Nitride based)
5. Vacuum pump
6. Mask design file (TLM and IDE patterns)
7. Developer solution
8. Deionized (DI) water
9. Nitrogen gas blower
10. Optical microscope

9.4 Steps to Follow

Pre-Writing Preparation

1. Bake the Wafer:

- Remove the spin-coated wafer from the spin coater and bake it at 110 °C for 1 minute.
- Clean the spin coater with an acetone solution after use.

9.4.1 Laser Writing Process

1. Setup the Laser Writer:

- Place the wafer inside the laser writer.
- Select lens 3, which supports up to 1-micron technology.

2. Stabilize the Wafer:

- Start the vacuum pump to secure the wafer and prevent movement during writing.

3. Upload the Mask Design:

- Upload the TLM and IDE mask design into the laser writer.
- **Note:** TLM is used for contact resistance calculation, and IDE is for gas detection.

4. Align the Wafer:

- Locate the center of the wafer by calculating the mean of its extremes using the arrow keys on the keyboard.

5. Writing Process:

- Start the writing process, which may take several minutes depending on the mask complexity.

9.4.2 Post-Writing Steps

1. Develop the Wafer:

- Submerge the wafer in the developer solution for 30 seconds.

2. Clean the Wafer:

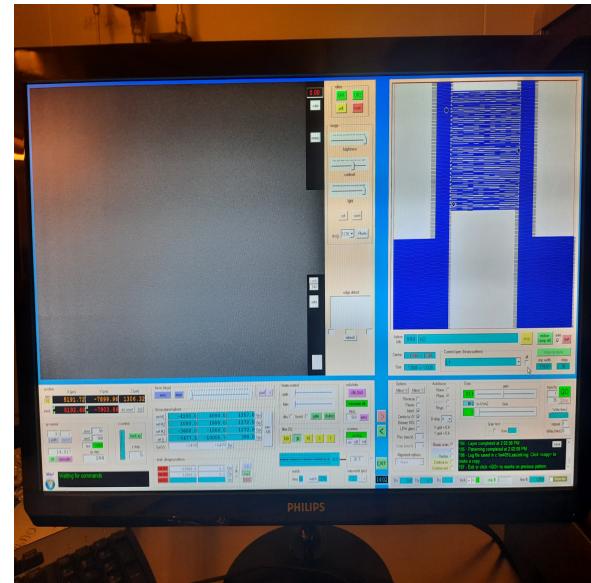
- Rinse the wafer with DI water and dry it using a nitrogen gas blower.

3. Inspect the Patterns:

- Use an optical microscope to verify the engraved microstructures on the wafer.



(a) Laser Writer



(b) Design of IDE pads

Figure 6: Laser writing setup

9.5 Conclusion

The photolithography process successfully engraves micro-patterns onto the silicon wafer, preparing it for specific applications like contact resistance measurement (TLM) and gas detection (IDE). Proper handling of equipment and precise alignment ensure the accuracy of the fabricated designs.

10 Lab Report: DC Sputtering Process

10.1 Introduction

This report details the DC sputtering process used for depositing chromium (Cr) metal onto a silicon (Si) substrate. The process was performed in a cleanroom environment using a specialized sputtering system. The procedure involves substrate preparation, vacuum chamber operation, and precise control of sputtering parameters to achieve uniform metal deposition.

10.2 Equipment and Materials

- Sputtering machine with load chamber and main chamber
- Vacuum pump system
- Chuck holder with magnetic control
- Silicon substrate (pre-processed using laser writer)
- Chromium target
- Argon gas supply
- Deionized (DI) water
- Acetone solution
- Nitrogen gas for drying

10.3 Process Parameters

- **Sputtering Type:** DC Sputtering
- **Target Material:** Chromium
- **Applied Voltage:** 150 Volts
- **Sputtering Time:** 150 seconds
- **Deposition Rate:** 4 Å/second
- **Operating Temperature:** 13K
- **Process Gas:** Argon

10.4 Detailed Procedure

10.4.1 1. Sample Preparation

- Mount the laser-processed silicon wafer onto the chuck.
- Secure the wafer with tape.
- Place the mounted wafer in the load chamber.

10.4.2 2. Chamber Preparation

- Evacuate the load chamber using the vacuum pump.
- Monitor pressure until it matches the main sputtering chamber.
- Open the gate valve between load and sputtering chambers.

10.4.3 3. Sample Transfer

- Transfer the substrate into the sputtering chamber using magnetic manipulation.
- Position the substrate precisely using chamber control valves.
- Retract the chuck holder.
- Seal the gate between chambers.

10.4.4 4. Sputtering Process

- Program the system UI with required parameters.
- Execute two-phase sputtering:
 - **Phase 1:** Surface striking (cleaning).
 - **Phase 2:** Chromium coating.
- Monitor the process indicated by blue argon plasma.

10.4.5 5. Sample Retrieval

- Equalize chamber pressures.
- Transfer sample back to load chamber.
- Remove from system.

10.4.6 6. Post-Processing

- Rinse wafer with DI water.
- Clean with acetone to remove excess chromium from photoresist.
- Dry using nitrogen gas.

10.5 Observations

- Blue plasma was observed during the sputtering process, indicating proper argon ionization.
- After cleaning with acetone, chromium coating remained only on the intended silicon surface areas.
- The process resulted in selective metal deposition as designed.



Figure 7: Sputtering machine

10.6 Conclusions

The DC sputtering process successfully deposited chromium onto the silicon substrate with selective patterning. The use of photoresist and subsequent cleaning enabled precise control over the metal deposition areas. The process parameters (150V, 150s) provided adequate conditions for uniform chromium coating at the specified deposition rate of 4 Å/second.

10.7 Safety Considerations

- Proper cleanroom protocols were followed throughout the process.
- Careful handling of vacuum systems was maintained.
- Appropriate safety measures were taken when working with acetone and other chemicals.
- Proper ventilation was ensured during the chemical cleaning process.

11 Lab Report: Fabrication of MEMS Structures using Silicon Wet Bulk Micromachining

11.1 Aim

This experiment aimed to study and perform wet bulk micromachining of silicon to fabricate microstructures, such as cantilevers, using anisotropic etching in a CMOS-compatible process.

11.2 Theory

Bulk micromachining is a microfabrication process used to create MEMS structures by selectively removing the bulk of the substrate. This experiment focuses on wet bulk micromachining, which involves chemical solutions to etch silicon. Two types of wet etching are commonly employed:

- **Isotropic etching:** The etch rate is uniform in all directions.
- **Anisotropic etching:** The etch rate varies based on the crystallographic orientation of the silicon. For example, the {111} planes etch slower than {100} and {110} planes.

Anisotropic etching is particularly significant for fabricating free-standing MEMS structures like cantilevers and diaphragms. TMAH (tetramethylammonium hydroxide) is used as the etchant due to its CMOS compatibility.

11.3 Materials and Equipment

- Silicon (Si) {100} wafer with a $1 \mu\text{m}$ thick silicon dioxide (SiO_2) masking layer
- Positive photoresist (AZ1512HS)
- Hexamethyldisilane (HMDS)
- Buffered HF solution ($\text{HF:NH}_4\text{F} = 1:7$)
- TMAH solution (25 wt. %)
- UV lithography setup (Mask aligner: MIDAS MDA-400M)
- Optical microscope (Olympus STM6)
- Spin coater
- Hot air oven
- Developer solution ($\text{NaOH:H}_2\text{O} = 1:3$)
- Acetone and deionized (DI) water

11.4 Experimental Procedure

11.4.1 Wet Etching of SiO_2 Layer

We began with a silicon {100} wafer coated with a $1 \mu\text{m}$ SiO_2 masking layer. The wafer was patterned using UV lithography as follows:

1. Spin coating of HMDS followed by positive photoresist (AZ1512HS) was performed at 3000 rpm for 30 seconds.
2. The wafer was pre-baked at 90°C for 30 minutes in a hot air oven.
3. A photomask containing the cantilever patterns was aligned, and UV exposure was carried out for 8 seconds.
4. The exposed wafer was developed in $\text{NaOH:H}_2\text{O}$ (1:3) for 2 minutes and rinsed with DI water.
5. Post-baking at 120°C for 30 minutes was performed.

The SiO_2 layer was selectively etched using a buffered HF solution. The etched wafer was rinsed thoroughly with DI water and inspected under a microscope to verify the patterns.

11.4.2 Anisotropic Etching with TMAH

We proceeded to fabricate cantilever structures through anisotropic etching:

1. The photoresist was removed using acetone, and the wafer was cleaned with DI water.
2. The wafer was diced into smaller chips for easier handling.
3. A 25 wt.% TMAH solution was heated to 70 °C, and its temperature was monitored continuously.
4. The chips were immersed in the TMAH bath. Periodic inspections were conducted at 30-minute intervals to monitor the etching progress.
5. The etching process was stopped once the cantilever structures were fully released.
6. The fabricated structures were cleaned with DI water and characterized using an optical microscope.

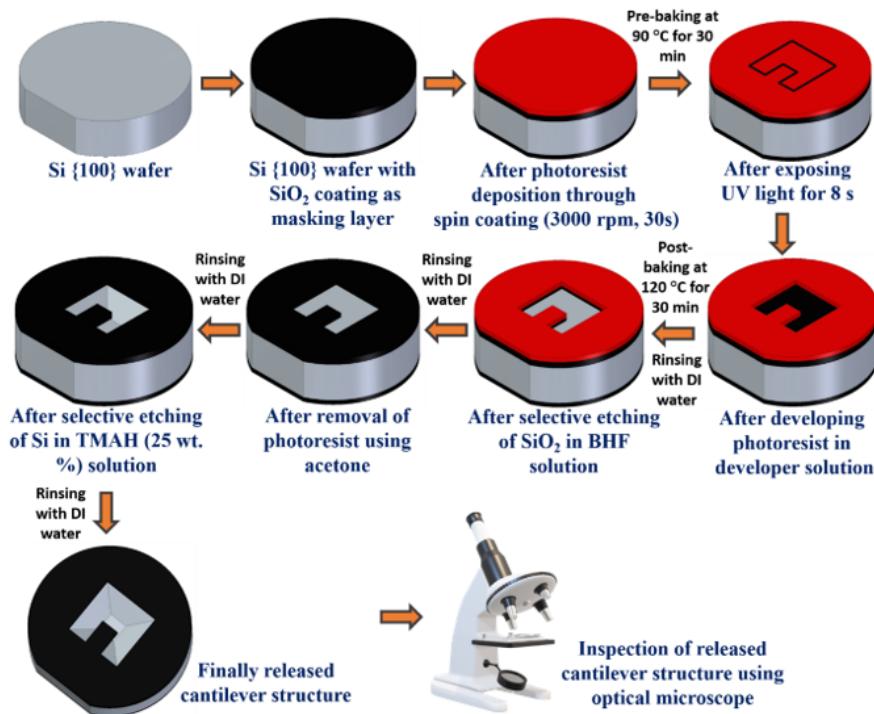


Figure 8: Schematic representation of the process steps to fabricate cantilever structures in Si {100} wafer.

11.5 Observations and Results

- The SiO₂ layer was effectively patterned and etched using buffered HF.
- TMAH etching successfully fabricated cantilever structures, as verified under the microscope.
- KOH was avoided due to its incompatibility with CMOS processes, emphasizing the importance of using TMAH for this application.
- Optical microscopy revealed well-defined cantilever structures.



(a) Etched Silicon Wafer



(b) Wet Etching Station where Wet Etching is done

Figure 9: Observations from the Lab

11.6 Conclusion

The experiment demonstrated the fabrication of MEMS structures using silicon wet bulk micromachining. Anisotropic etching with TMAH proved effective in releasing free-standing cantilever structures. This process showcases the precision and feasibility of MEMS fabrication using wet bulk micromachining.

12 Lab Report: Silicon Wafer Etching using Olympus LEXT

12.1 Meta Description

We know about the benefits of silicon wafer etching technique using the Olympus LEXT OLS5100 laser confocal microscope for micro-texturing of the silicon front surface to improve the performance of solar panels, and the potential gains it can offer solar parks across India.

12.2 Introduction

Silicon wafer etching is a crucial process to improve light trapping by modifying the surface reflectivity of silicon wafers, primarily for solar panel manufacturing. This process, known as micro-texturing, involves the use of alkaline solutions to form micro-sized pyramidal structures on the silicon surface. Parameters such as surface roughness and surface area are essential as they increase with etching time, helping to optimize the etching process for desired results.

12.3 Challenges in Conventional Techniques

Conventional techniques like SEM (Scanning Electron Microscopy) require cutting samples to observe the cross-section, making the process tedious and cost-ineffective.

12.4 Solution: Olympus LEXT OLS5100 Laser Confocal Microscope

The Olympus LEXT OLS5100 laser confocal microscope offers an easy and sophisticated alternative for analyzing silicon wafer etching.

12.4.1 Benefits

- **Submicron Level 3D Observation and Measurement:** Enables accurate observation of submicron unevenness on the silicon wafer's texture.
- **Surface Roughness Measurement:** Provides ISO-compliant measurements, transitioning from line profile to aerial observation for a new standard of roughness measurement.
- **Speed and Efficiency:** A non-contact, non-destructive technique that requires no sample preparation, allowing immediate measurement.

12.5 Functional Capabilities

- **Etched Silicon Wafer Imaging:** Captures height of individual peaks and calculates maximum peak values (Sp), surface roughness, surface area, and pyramid volume.
- **Volume and Surface Area Measurement:** Analyzes peak and valley volumes, enabling optimization for homogeneous peak distribution and minimal valley zones.
- **Peak Density and Direction Analysis:** Measures Spd (density of peaks per unit area), Spc (arithmetic mean of principal curvature of peaks), and Std (texture direction angle).
- **Periodicity Analysis:** The PSD parameter provides insights into the periodicity of pyramidal structures.

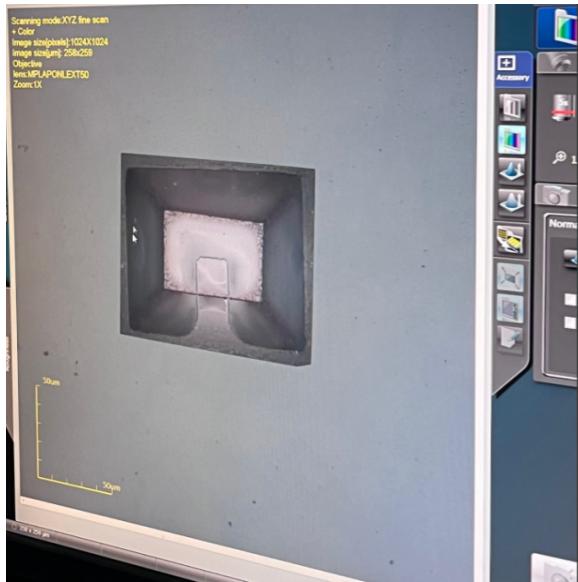
12.6 Advantages of the Olympus OLS5100

- Eliminates the need for destructive sample preparation.
- Ensures non-contact analysis, preventing contamination.
- Automates data collection and visualization with a smart experiment manager, reducing errors and simplifying workflows.
- Provides head map analysis, displaying all relevant data in a single sheet without the need for individual file handling.

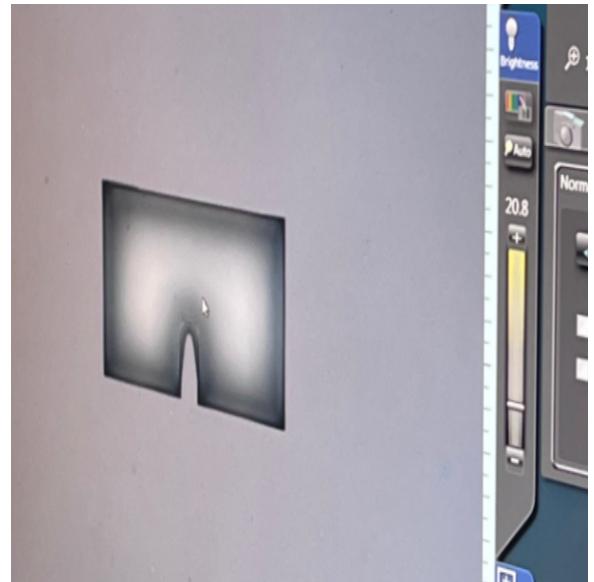
12.7 Observation

During the etching process, the following phenomena were observed:

- **Undercutting:** Significant undercutting at mask edges not aligned with 111 planes, especially in convex patterns.
- **Plane-Specific Etching:** 100 and 110 planes showed faster etching rates compared to the slower 111 planes.
- **Concave and Convex Cutting:** Concave mask patterns aligned well with 111 planes, whereas convex patterns exhibited prominent underetching effects.
- **Undercutting and Surface Morphology:** Prolonged etching revealed 111 facets on the sidewalls of fabricated structures, emphasizing orientation dependency.



(a) Perfectly Etched: We can see the transparent SiO₂ layer



(b) Under Etched structure

Figure 10: Observations from the Lab

12.8 Conclusion

The Olympus LEXT OLS5100 laser confocal microscope revolutionizes silicon wafer etching analysis by providing precise, non-destructive, and automated measurements. It plays a significant role in optimizing processes for solar panel manufacturing, contributing to improved performance and efficiency in solar energy applications.

13 Lab Report: Vibrometer Characterization

13.1 Objective

The purpose of this experiment was to characterize the vibration properties of a system using a Doppler vibrometer. This included measuring frequency and mode shapes, as well as damping and quality factors.

13.2 Introduction

A Doppler vibrometer (LDV) is a scientific instrument used to measure vibrations on a surface without physical contact. The LDV operates by detecting the Doppler effect of a reflected laser beam and is widely used in engineering and biomedical applications.

13.2.1 Applications of LDVs

- **Engineering:** Non-contact measurement of vibrations and sounds in industrial machinery, motors, and electronic equipment.
- **Biomedical:** Hearing research and other medical applications.

13.2.2 Specifications of the LDV System

- **Frequency measurement range:** 0.1 Hz to 250 kHz (analog), up to 5 MHz (digital).
- **Velocity measurement range:** Adjustable from 10 mm/s to 2 m/s based on resolution.
- **Resolution:** Velocity: $0.02 \mu\text{m}/\text{s}\sqrt{\text{Hz}}$, Displacement: 1 pm.
- **Demodulation system:** FPGA digital decoding system for real-time output.

13.3 Experimental Procedure

- The accelerometer was placed on the test surface, and the Doppler vibrometer was set up to measure the vibration characteristics.
- The system was excited, and the laser beam was focused on the vibrating surface to record the Doppler shift.
- The frequency spectrum of the vibrations was obtained, and the resonant peak was identified.
- High precision bandwidth (HPBW) was used to calculate the quality factor (Q).

13.4 Observations

- The magnitude versus frequency spectrum was analyzed.
- The resonant peak occurred at a frequency of 71.56 kHz.
- The half-power bandwidth (HPBW) was measured as 938 Hz.

13.5 Calculations

13.5.1 Quality Factor (Q)

The quality factor is calculated using the formula:

$$Q = \frac{f_0}{\text{HPBW}}$$

where:

- $f_0 = 71.56 \text{ kHz}$
- $\text{HPBW} = 938 \text{ Hz}$

Substituting the values:

$$Q = \frac{71,560}{938} \approx 76.26$$

13.6 Results

- **Resonant Frequency:** 71.56 kHz.
- **Half-Power Bandwidth:** 938 Hz.
- **Quality Factor:** 76.26.



Figure 11: Magnitude v/s Frequency Response of Accelerometer when place inside LDV

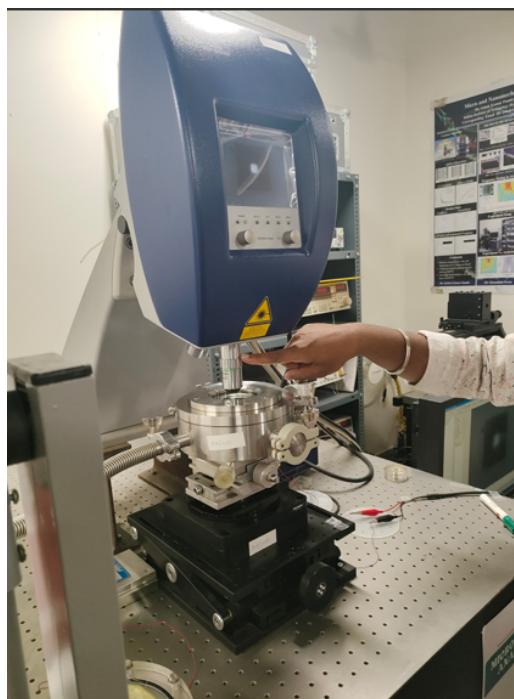


Figure 12: A Doppler vibrometer, also known as a laser Doppler vibrometer (LDV)

13.7 Conclusion

The experiment successfully characterized the vibration properties of the test system. The resonant peak was identified at 71.56 kHz, and the quality factor was calculated as approximately 76.26, indicating the sharpness of the resonance. The Doppler vibrometer proved to be an effective tool for non-contact vibration analysis, providing precise and reliable measurements.

14 Lab Report: Deep Reactive Ion Etching (DRIE) Process

14.1 Objective

To understand and perform the Deep Reactive Ion Etching (DRIE) process on a silicon wafer using the PlasmaPro® 100 Estrelas system, while learning the critical steps of wafer handling, etching, and chamber cleaning.

14.2 Equipment and Materials

- PlasmaPro® 100 Estrelas system
- Silicon wafer
- Process gases: SF₆, C₄F₈, O₂ (optional)
- Pumps: Scroll pump, Rotary pump, Turbo molecular pump
- Pressure measurement devices: Pirani gauge, Penning gauge

14.3 Experimental Procedure

14.3.1 Step 1: Wafer Loading

- Place the silicon wafer on the robotic arm, ensuring that the silicon side faces downward.

14.3.2 Step 2: Initial Evacuation

- Use the scroll pump to evacuate the load chamber until the pressure matches that of the main process chamber, monitored via the Pirani gauge, which operates based on the thermal conductivity of the gas.

14.3.3 Step 3: Transfer to Process Chamber

- Once comparable pressures are achieved, transfer the wafer into the process chamber.

14.3.4 Step 4: Wafer Clamping

- Use the electrostatic chuck (ESC) to securely clamp the wafer in place within the process chamber.

14.3.5 Step 5: Chamber Pressure Reduction

- Utilize the rotary pump to remove larger air molecules initially. Once a specific pressure is achieved, switch to the turbo molecular pump for higher vacuum levels. The Penning gauge, which operates based on ionization in a magnetic field, measures the high vacuum achieved.

14.3.6 Step 6: DRIE Process

The DRIE process alternates between two key steps:

1. Etching Step:

- SF₆ gas is introduced, producing fluorine radicals that chemically react with silicon to form volatile SiF₄, which is evacuated. Ion bombardment ensures vertical etching at the bottom of the features, maintaining high anisotropy.

2. Passivation Step:

- C₄F₈ gas is introduced to deposit a thin polymer layer on the sidewalls, protecting them from lateral etching.

These steps are repeated cyclically to achieve the desired etch depth and feature profile.

14.3.7 Step 7: Plasma Generation

- **RF Plasma:** An RF power source ionizes process gases, directing ions vertically toward the wafer surface for anisotropic etching.
- **ICP Plasma:** The inductively coupled plasma (ICP) source enhances plasma density and uniformity by inducing further gas ionization through an oscillating magnetic field.

14.3.8 Step 8: Wafer Unloading

- After the etching process is complete, follow the evacuation procedure to remove the etched wafer from the chamber safely.

14.3.9 Step 9: Chamber Cleaning

Plasma Cleaning:

- Oxygen plasma is used to break down organic residues, while fluorinated gases (e.g., SF₆ or CF₄) remove inorganic silicon-based residues.

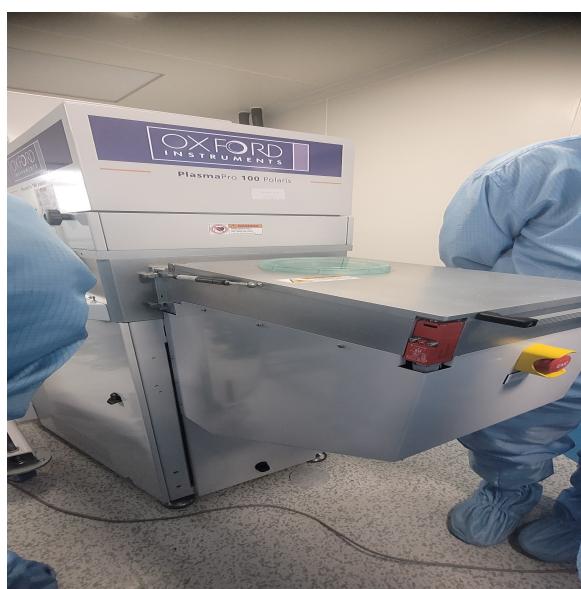
Cleaning Steps:

1. Introduce O₂ or cleaning gas to generate cleaning radicals.
2. Plasma is ignited, uniformly distributing reactive species throughout the chamber.
3. Evacuate volatile by-products and purge the chamber with inert gas (e.g., nitrogen) to reduce the concentration of byproducts to reduce the damage caused on the blades of the pumps.

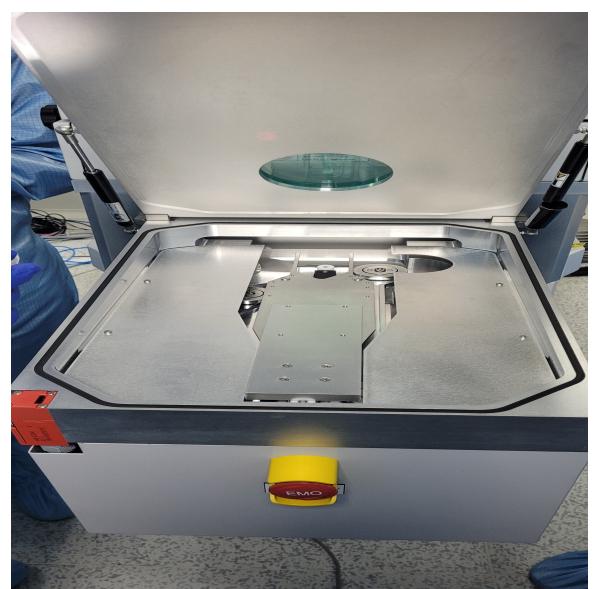
14.4 Observations

• Pressure measurements:

- Initial evacuation using the scroll pump: 10⁰ Torr (Pirani gauge).
- Final vacuum achieved with the turbo molecular pump: 10⁻⁶ Torr (Penning gauge).
- Yellowish color plasma is created.
- Uniform and anisotropic etching observed on the silicon wafer.
- Residual polymer buildup and silicon compounds were effectively removed during the cleaning process.



(a) Ion Etching Machine



(b) Robotic arm

Figure 13: Deep Reactive Ion Etching Machine

14.5 Conclusions

The DRIE process was successfully performed on the silicon wafer using the PlasmaPro® 100 Estrelas system. Key steps, including precise pressure control, plasma generation, and cyclic etching-passivation, enabled the fabrication of high-aspect-ratio structures. The cleaning procedure ensured the removal of contaminants, maintaining chamber performance for future runs. Understanding the operation of pressure gauges and pumps was critical to achieving and monitoring the vacuum conditions necessary for DRIE.

15 Lab Report: Capacitance-Voltage Relationship in MOS Capacitors

15.1 Objective

To study the capacitance-voltage (C-V) relationship in a Metal-Oxide-Semiconductor (MOS) capacitor under various biasing conditions and analyze the effects of potential defects.

15.2 Theory

Capacitance (C) is defined as the differential change in charge (dQ) with respect to voltage (dV):

$$C = \frac{dQ}{dV}$$

For MOS capacitors, the following assumptions are made:

1. No charge is trapped in the oxide layer ($Q_{ss} = 0$).
2. No charge is trapped at the oxide-semiconductor interface.

15.3 Operating Conditions

15.3.1 Accumulation Condition

- **Substrate:** p-type.
- **Bias:** Negative gate bias ($V_G < 0$).
- **Effect:** Electrons accumulate at the oxide-semiconductor interface. Only oxide capacitance (C_{ox}) is present.

$$C_{acc} = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

Observations:

- Positive charge ($+Q'$) on the metal plate.
- Negative charge ($-Q'$) accumulates in the semiconductor.

15.3.2 Depletion Condition

- **Substrate:** p-type.
- **Bias:** Slightly positive ($V_G > 0$).
- **Effect:** A depletion layer forms, causing capacitance to decrease due to the series combination of oxide and depletion capacitance.

$$\frac{1}{C_{dep}} = \frac{1}{C_{ox}} + \frac{1}{C_{depletion}}$$

As the depletion width increases, the capacitance decreases.

15.3.3 Inversion Condition

- **Substrate:** p-type.
- **Bias:** Highly positive ($V_G \gg 0$).
- **Effect:** Strong inversion occurs when the surface potential equals $2\phi_F$. An inversion layer forms, and the capacitance approaches C_{ox} .

15.4 Defects Analysis

In real MOS capacitors, **defects** can alter the C-V characteristics:

1. Charge Trapping in Oxide Layer:

- Caused by impurities or fabrication errors.
- Leads to shifts in the C-V curve.

2. Interface States:

- Localized states at the oxide-semiconductor interface.
- Affect the flat-band voltage and overall capacitance behavior.

3. Charge Distribution:

- Deviation from ideal charge distribution may occur.

These defects must be minimized to ensure accurate device performance.

15.5 Graphical Representation

The C-V curve reflects:

- **Accumulation:** High capacitance due to oxide-only behavior.
- **Depletion:** Gradual decline due to the widening depletion layer.
- **Inversion:** Stabilization at C_{\min} , dominated by oxide capacitance.

15.6 Frequency Effects

The frequency of the applied AC signal significantly influences the C-V characteristics of MOS capacitors:

1. High-Frequency Response:

- At high frequencies, the minority carriers cannot respond quickly to the AC signal.
- In the inversion condition, capacitance is limited to the oxide capacitance (C_{ox}).
- The C-V curve in inversion appears to plateau at a higher capacitance than in low-frequency measurements.

2. Low-Frequency Response:

- At low frequencies, minority carriers have sufficient time to respond.
- The depletion region alternates between strong inversion and depletion.
- Capacitance appears higher in inversion, as minority carriers contribute to the total charge.

Observations on Graphs:

- Low-frequency curves are closer to the theoretical C_{ox} .
- High-frequency curves stabilize at C_{\min} in inversion.

15.7 Thermal Oxide Effects

The thickness and quality of the thermally grown oxide layer influence the C-V relationship:

1. Oxide Thickness (t_{ox}):

- Thicker oxides result in lower capacitance due to the relation:

$$C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}}$$

- A thicker oxide shifts the entire curve downward.

2. Oxide Quality:

- Poorly grown oxide with defects (e.g., pinholes, impurities) introduces interface charges, shifting the flat-band voltage and distorting the curve.

Graph Effects:

- Thicker oxides reduce C_{acc} , C_{dep} , and C_{inv} , creating a compressed curve.
- Defects in thermal oxide cause irregularities or asymmetry in the curve.

15.8 Field Oxide Effects

Field oxides used for device isolation may cause:

1. Fringing Fields:

- Electric fields originating from the edges of the MOS capacitor can slightly distort the capacitance values, especially at the edges of the depletion and inversion regions.

2. Oxide Charges:

- Positive charges in the field oxide shift the flat-band voltage and alter the depletion region characteristics.

Graph Effects:

- Fringing fields may slightly elevate capacitance near the flat-band region.
- Oxide charges cause horizontal shifts in the C-V curve.

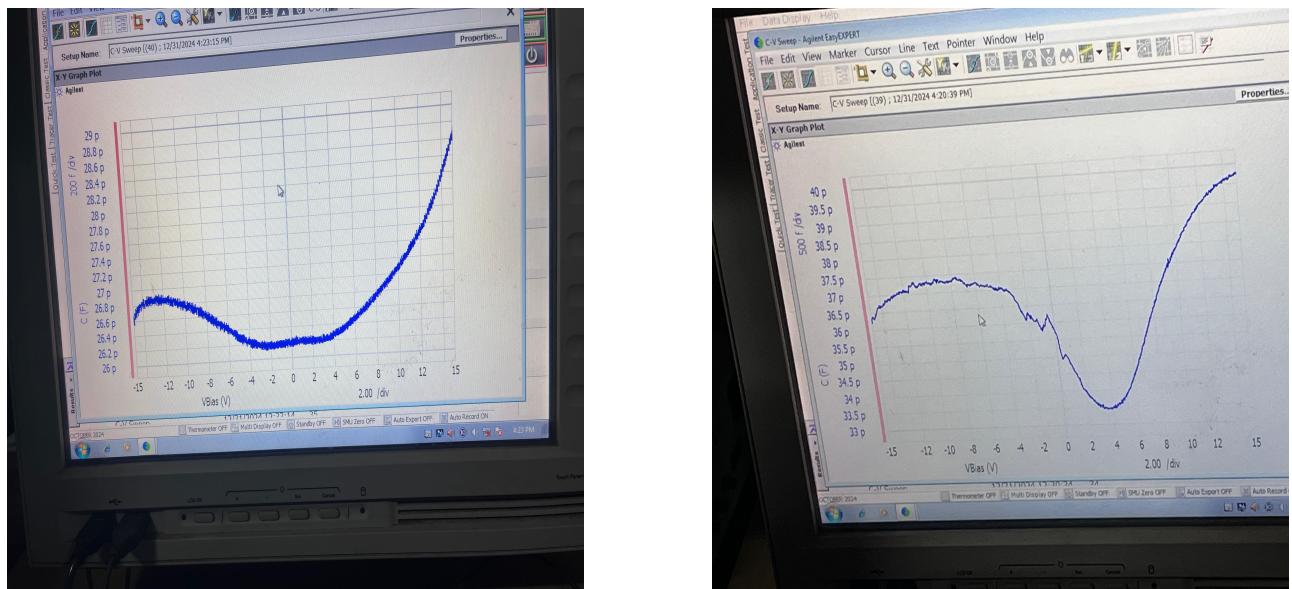


Figure 14: C-V Characteristics at different frequencies

15.9 Conclusion

The experiment highlights the ideal and non-ideal behaviour of MOS capacitors. Observations align with theoretical predictions, while potential defects such as trapped charges and interface states emphasize the need for optimized fabrication processes.