Advancements in Semiconductor Technologies

Insights from Taiwanese Experts

Naman Jain

Indian Institute of Information Technology Guwahati

Date: 18-12-2024 to 20-12-2024

Lecture Schedule

18th December 2024
Development & Future Trends of 3D-IC Packaging Technology
Duration: 1.5 hours (11:30 AM - 1 PM) and 1.5 hours (2:30 PM - 4 PM)
Speaker: Prof. Chang-Chun Lee, Department of Power Mechanical Engineering, NTHU

19th December 2024
Manufacturing Processes of Advanced Nano Devices
Duration: 3 hours (9:30 AM - 12:30 PM), 3 hours (2 PM - 5 PM), and 2 hours (11:30 AM - 1 PM)
Speaker: Prof. Tsung-Chieh Cheng, Department of Mechanical Engineering,
National Kaohsiung University of Science and Technology

20th December 2024
The Trends of Advanced Heterogeneous Integration Packaging
Duration: 3 hours (9:30 AM - 12:30 PM) and 1 hour (2 PM - 3 PM)
Speaker: Prof. Meng-Kai Shih, Department of Mechanical and Electromechanical Engineering,
National Sun Yat-sen University, Kaohsiung
The Development of Semiconductor Industry and Technology in Taiwan
Duration: 2 hours (3:30 PM - 5:30 PM)
Speaker: Dr. Yu-Hua Huang, Program Manager, TCSFT, NTHU
Highlights:
- Taiwan's contributions to global semiconductor technology
- Trends in semiconductor R&D and industrial growth

Prepared by: Naman Jain and Krushna Dinesh Rane

1 Future Trends of 3D-IC Packaging Technology

Introduction: The course began with an introduction to the concept of ***More Than Moore*** from a Taiwanese perspective. "More Than Moore" refers to innovations in semiconductor technology that extend beyond the traditional scaling of transistors as described by Moore's Law.

1.1 Course Outline

- **Development and Current Status of Fan-Out Packaging**
- **Development Trends and Key Technologies of 3D IC Packaging**
- **Development and Current Status of Heterogeneous IC Packaging and Technology**
- **Vehicle Design Cases for 3D Design**

1.2 Briefing on Scaling Trends

The briefing delved into the process of scaling semiconductor components:

- Dividing a unit area by half reduces the side lengths by a factor of $\sqrt{2}$.
- This iterative scaling process progresses as follows:

$$90 \text{ nm} \to 63 \text{ nm} \to 45.5 \text{ nm} \to 31.5 \text{ nm} \to 22.4 \text{ nm} \to 15.4 \text{ nm} \to 10.5 \text{ nm} \to 7 \text{ nm} \to 4.9 \text{ nm} \to 3.5 \text{ nm} \to 2 \text{ nm} \to 1 \text{ nm}.$$

1.3 Basics of Wafer-Level Packaging (WLP)

Wafer-level packaging (WLP) is a process in integrated circuit manufacturing where the packaging is done at the wafer level, prior to the wafer being diced into individual dies. This allows the entire wafer to be packaged as a whole before being divided into individual packaged chips.

Types of WLP:

1. **Fan-in WLP:** The package size matches the die size, with all connections located within the die area.
2. **Fan-out WLP:** This method expands the package area beyond the chip area, enabling integration of additional active and passive components to form *System in Package* (SiP).

1.3.1 Fan-in WLP Process

Key Technologies:

- **Redistribution Layer (RDL):** Converts peripheral welding areas to planar arrays on the chip surface.
- **Bumping:** Forms solder bumps on the wafer, with processes such as planting, ball mount, and encapsulation.

1.3.2 Fan-out WLP Process

Key Technologies:

- **Wafer Reconstruction:** Bonds the chip onto the wafer, enabling expansion of the package area.
- Incorporates active devices and passive components to create SiP.

1.4 Comparison of Fan-out and Fan-in Packaging

Aspect	Fan-out	Fan-in
Connection Distribution	Spreads connections outwards from the die, enabling a higher density of I/O pins.	Keeps most connections within the die boundary, limiting the number of available pins.
Package Size	Often leads to smaller and thinner packages due to the ability to distribute connections over a larger area.	Tends to be larger to accommodate the limited I/O pin density.
Application	Beneficial for high-performance devices requiring a large number of I/O connections, such as high-end processors or complex SoCs and AI chips.	Suitable for simpler designs with less demanding I/O needs.
Example	A chip with a small die area but needing many connections to external components, where the connections "fan out" from the die to a larger substrate, allowing for more pins within a smaller package footprint.	A chip with a larger die area where most connections are made within the die boundaries, limiting the number of external connections available.

1.5 TSV and Microbump Technology in IC Packaging

In IC packaging, **TSV** stands for *Through Silicon Via* and **microbumps** are tiny solder bumps. Together, they enable vertical connections between multiple chips in a 3D stacking arrangement, providing high-density integration within a single package. This allows for more complex circuitry in a smaller footprint. Essentially, TSVs act as vertical electrical pathways through the silicon substrate, while microbumps provide the electrical connections between stacked chips on top of the TSVs.

Key Points about TSVs and Microbumps:

- **Function:** TSVs are tiny holes drilled through a silicon wafer, creating vertical electrical pathways. Microbumps are small solder bumps that connect the top and bottom surfaces of stacked chips, enabling electrical signal transmission between them.
- **3D Integration:** This technology is crucial for advanced 3D integrated circuits (3D ICs) where multiple chips are stacked vertically.
- **Interposer:** Often, an interposer layer is used between stacked chips. It contains the TSVs and redistribution layers (RDLs) to route signals between different chips.
- **Manufacturing:** The fabrication process involves:
  1. Etching the TSVs into the silicon wafer.
  2. Depositing metal layers to fill the vias.
  3. Forming microbumps on chip surfaces through a specialized plating process.
- **Challenges:** Key concerns include:
  - Managing thermal stress due to different thermal expansion coefficients of materials the micro bumps may break due to stress , thats why there is development of Hybrid bumps.
  - Ensuring reliable electrical connections at the microbump interface.
  - Maintaining high density while minimizing parasitic capacitance.

1.5.1 Hybrid Bumps in IC Packaging

In IC packaging, **Hybrid Bumps** refer to a technique where, instead of traditional solder bumps, a combination of dielectric material and embedded copper pads is used to create direct copper-to-copper connections between dies. This method, often referred to as *hybrid bonding*, eliminates the use of bumps altogether. It allows for significantly finer pitch interconnects in advanced 3D packaging, enabling higher density and better electrical performance compared to standard bump-based connections. This approach provides a more efficient and effective way to achieve high-density integration in complex chip stacking arrangements.

1.6 CoWoS and InFO Technologies

1.6.1 CoWoS Technology

CoWoS (Chip-on-Wafer-on-Substrate) is a 2.5D packaging technology developed by TSMC that enables the integration of multiple chips (such as CPUs, GPUs, and memory) on a single package. The key component of CoWoS is an *interposer*, a silicon substrate with Through Silicon Vias (TSVs) for high-speed connections. This technology is ideal for high-performance and high-bandwidth applications.

1.6.2 TSMC's Integrated Fan-Out (InFO) Technology

In traditional chip packaging, individual chips are cut from a wafer and then connected to a substrate (like a printed circuit board) using wires or solder bumps. TSMC's **Integrated Fan-Out (InFO)** technology takes a different approach, offering advanced packaging solutions with several key features:

- **"Growing" the Package:** Instead of cutting the chips first, the packaging is built directly on the wafer. This involves creating a redistribution layer (RDL) on the wafer surface, which acts as an intermediary wiring layer.
- **Wider Connections:** The RDL enables more connections and wider spacing between them compared to traditional wire bonding. This process "fans out" the connections, giving the technology its name.
- **Cutting After Packaging:** Only after the packaging layers are built on the wafer are the individual chips separated.

1.6.3 Types of InFO

TSMC offers different variations of InFO technology to address diverse application needs:

- **InFO_PoP (Package-on-Package):** Used for stacking memory chips on top of a processor, this variation is commonly found in smartphones.
- **InFO_oS (on-Substrate):** Designed for larger packages and higher-performance applications, such as networking and high-performance computing.

1.6.4 Points Concluded

- Manufacturing individual chips on a silicon wafer is a complex, multi-step process, while dicing a wafer into individual chips is a relatively simple cutting process.
- **IC Packaging and Protection:** Packaging protects ICs from dust, contaminants, mechanical damage, and environmental factors like humidity. It also ensures proper power delivery, signal routing, and heat dissipation.
- **Packaging Without Clean Rooms:** When clean rooms are unavailable, specialized packaging techniques, including polymers or bonding methods, are used. For critical applications like medical electronics, materials such as gold or silver are preferred for their conductivity and biocompatibility.
- **Fabrication Challenges and Metamaterials:** Advanced packaging frameworks sometimes use metamaterials. However, designs with porous structures may not provide sufficient protection, posing challenges in certain applications.
- **Lead Frames and Solder Paste in SMT:** Lead frames provide electrical connections between the IC and the PCB. Solder paste is a key material in Surface Mount Technology (SMT) for mounting IC packages onto PCBs.
- **SMT Packaging Types:** SMT packages like Quad Flat Packages (QFP), Small Outline Packages (SOP), and Thin Small Outline Packages (TSOP) cater to various applications based on size, density, and performance requirements.
- **Ball Grid Array (BGA):** BGA packaging replaces traditional leads with a grid of solder balls, offering higher pin density and improved thermal and electrical performance, making it ideal for CPUs and GPUs.
- **Flip-Chip and Bumps:** Flip-chip packaging involves flipping the IC die upside down and using solder bumps for connections. Micro bumps provide high-density interconnects but face stress challenges, mitigated through hybrid bump designs.

- **Flip-Chip Ball Grid Array (FCBGA):** Combines flip-chip technology with BGA, mounting the die face-down onto a substrate, making it suitable for high-performance computing like servers and GPUs.
- **Substrates:** The base of IC packages, substrates can be made from polyester, ceramic, or organic materials, chosen based on application requirements like heat resistance or lightweight designs.

1.7 Advanced IC Packaging Techniques

1.7.1 Wafer-Level Packaging (WLP) and Chip-Scale Packaging (CSP)

- **WLP:** The IC is packaged directly at the wafer level before dicing individual dies.
- **CSP:** A type of package with an area less than 1.2 times the die size. While CSP provides compactness and performance, it doesn't necessarily use wafer-level processes.
- **Key Difference:**
  - **WLP** focuses on packaging at the wafer level.
  - **CSP** refers to a package close to the die's size, which may or may not use WLP techniques.

1.7.2 Panel-Level Packaging (PLP) vs. Wafer-Level Packaging (WLP)

- **WLP:** Utilizes circular wafers for packaging, constrained by wafer size.
- **PLP:** Uses rectangular panels, allowing larger batch processing and lower costs for mass production.

Aspect	**WLP**	**PLP**
Substrate Shape	Circular (wafer)	Rectangular (panel)
Chip Integration	Limited by wafer size	Greater capacity
Cost	Higher	Lower for large scale

Table 1: Comparison of WLP and PLP

1.7.3 Reliability Tests for Substrates

- **Thermal Cycle Test (TCT):** Simulates temperature variations to test durability under thermal stress.
- **Accelerated Lifetime Test:** Uses elevated temperatures or stress to identify failure points early in the lifecycle.

1.7.4 Underfilling in Flip Chips

- **Purpose:** Distributes mechanical stress and enhances reliability in flip-chip designs.
- **Function:** Compensates for increased stress from die shrinkage and higher functionality demands.

1.7.5 Single Chip Module (SCM) vs. Multi-Chip Module (MCM)

Aspect	**SCM**	**MCM**
Number of Chips	One chip	Multiple chips
Functionality	Limited to single IC	Combines several ICs
Application	Simple devices	Complex systems (e.g., servers)

Table 2: Comparison of SCM and MCM

1.7.6 Heterogeneous vs. Homogeneous Packaging

- **Homogeneous Packaging:** Combines chips with similar functionalities (e.g., memory modules).
- **Heterogeneous Packaging:** Integrates chips with different functionalities for advanced systems (e.g., processors with GPUs or sensors).

1.7.7 Fan-In and Fan-Out Packaging

- **Fan-In WLP:** Interconnections are within the chip area, limiting I/Os.
- **Fan-Out WLP (FOWLP):** Expands interconnects beyond the die using redistribution layers (RDLs).

1.7.8 Formation Approaches for FOWLP

- **Chip First, Die-Up:** Chips are placed face-up on a carrier.
- **Chip First, Die-Down:** Chips are placed face-down, followed by encapsulation.
- **Chip Last, RDL First:** RDLs are created before placing chips.

1.8 Extra Insights in Advanced Semiconductor Packaging

1.8.1 Two Logical Switches in Signal Routing

Signal routing in advanced semiconductor packaging often relies on logical switches to optimize functionality and efficiency:

1. **Logical Switch at the Chip Level:** Manages signal paths within the integrated circuit (IC) itself, ensuring efficient internal signal routing.
2. **Logical Switch in the Interposer/RDL:** Operates at the Redistribution Layer (RDL) or interposer to determine external signal routing.
    - Interposers act as intermediate layers connecting the silicon die to the substrate, enabling high-density interconnections.
    - **Through-Silicon Vias (TSVs):** Traditionally used in silicon interposers, TSVs support dense connections but introduce complexities and costs.
    - **Non-TSV Interposers (NTI):** Emerging as an alternative to TSVs, NTI provides high electrical performance through techniques such as chip-on-wafer (CoW) stacking, mold encapsulation, silicon removal, and chip module-on-substrate (CMoS) assembly.

1.8.2 NVIDIA's Role in Advanced AI and Packaging

NVIDIA continues to lead in AI advancements, leveraging cutting-edge semiconductor packaging and AI technologies:

- **NVIDIA NIM:** A suite of inference microservices aimed at accelerating the deployment of foundation models across diverse platforms.
- **Project Ceiba:** A collaboration with AWS to develop the world's fastest GPU-powered AI supercomputer. This system integrates GH200 NVL32 GPUs and Amazon EFA interconnects, hosted by AWS for NVIDIA's research and development initiatives.

These innovations provide scalable, efficient AI solutions, making advanced AI capabilities accessible and cost-effective.

1.9 Conclusion for Day 1

In this section 1, we explored advanced semiconductor packaging concepts, including WLP, PLP, and their comparisons, as well as reliability testing for substrates. We discussed techniques like underfilling flip chips, SCM versus MCM architectures, and homogeneous versus heterogeneous packaging. Signal routing strategies with logical switches at the chip and interposer levels were highlighted alongside the transition from TSV to NTI interposers. Finally, NVIDIA's contributions to AI computation and packaging innovations, such as NVIDIA NIM and Project Ceiba, underline the intersection of semiconductor technology with AI advancement. These developments signify the industry's ongoing drive toward more efficient, scalable, and cost-effective solutions.

1 Summarization of Day 2: Manufacturing Processes of Advanced Nano Devices

Speaker: Prof. Tsung-Chieh Cheng

1.1 Introduction

The session provided an insightful overview of the historical evolution of memory device manufacturing, processes involved in IC fabrication, and the trends in the semiconductor industry.

1.1.1 Semiconductor Trends

1. **Increase in Chip Performance:**
   - Smaller feature sizes, higher transistor density (Moore's law).
   - Improved energy efficiency and faster data transfer rates.
2. **Increase in Chip Reliability:** Advances in design and material quality.
3. **Reduction in Chip Price:** Higher yields and advanced manufacturing techniques.

1.1.2 Classification of Devices Based on Critical Dimension

- **Micrometer Devices (μm devices):** Critical dimension $> 100\,\text{nm}$.
- **Nanometer Devices (nm devices):** Critical dimension $\leq 100\,\text{nm}$.

1.1.3 Evolution of Wafer Size and IC Technology

1. **Wafer Size Evolution:**
   - 1965: The wafer size was 50 mm.
   - 2000: Increased to 300 mm, enabling more chips per wafer.
2. **Moore's Law:**
   - Initially predicted doubling of the transistor every 12 months, later adjusted to 18 months.
   - Continued relevance in driving performance and cost-efficiency until 2010.
3. **Critical Dimension Trends:**
   - Decreased from 350 nm to about $1 - 2\,\text{nm}$ by 2023.
   - Predicted to shrink further by 2034.
4. **Semiconductor Roadmap:**
   - The 20-year IMEC roadmap guides long-term advancements in semiconductor technologies.

1.2 Understanding FinFETs: Why FinFETs?

What is a FinFET? A Fin Field-Effect Transistor (FinFET) is a type of 3D transistor structure designed to address the challenges of traditional planar MOSFETs as device scaling reaches nanometer dimensions. It is named "FinFET" because the conducting channel, shaped like a fin, stands vertically on the silicon substrate.

Why FinFETs?

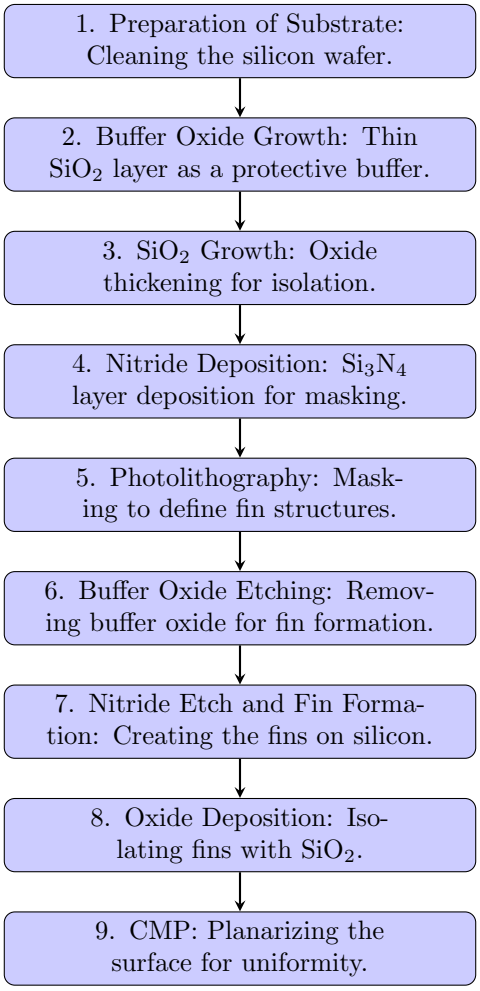
- **Reduced Current Leakage:**
  - In traditional planar transistors, as the channel length shortens, leakage currents and short-channel effects (SCE) increase significantly.
  - FinFETs mitigate this by wrapping the gate around the channel, providing better electrostatic control.
- **Improved Power Efficiency:**
  - Low leakage current reduces standby power consumption.
  - Better gate control improves switching efficiency, lowering dynamic power usage.
  - Faster switching speeds due to better electrostatic control.
  - FinFETs enable operation at lower voltages, enhancing speed and reducing power consumption.

1.2.1 Comparison of Planar MOSFETs and FinFETs

Aspect	Planar MOSFET	FinFET
Structure	Flat, 2D channel	3D channel wrapped around fin
Conduction Surface	Single surface	Multiple surfaces (3 sides of the fin)
Leakage Current	High at small nodes	Low due to better gate control
Short-Channel Effect (SCE)	Severe below 22nm	Minimized with multi-gate design
Power Efficiency	Higher leakage increases power consumption	Lower leakage reduces standby power
Scalability	Limited below 22nm	Effective for nodes below 16nm
Performance	Moderate switching speeds	Higher speed and lower power consumption

1.2.2 Fabrication Process Flow of a FinFet

(Explained using Video Illustration)



1.3 Key Factors for Semiconductor Industry Employees

- Yield Yield is a critical factor in semiconductor manufacturing, determining the quality and profitability of production.
  - Example calculations for 500 steps in the process:
    - $0.995^{500} \rightarrow 8.1\%$ yield
    - $0.99^{500} \rightarrow 0.65\%$ yield
    - $0.999^{500} \rightarrow 60.6\%$ yield
    - $0.9999^{500} \rightarrow 95\%$ yield
  - Higher yield reduces defects, ensuring better quality and lower production costs.
- Price of the Process The cost of each manufacturing step significantly impacts overall profitability and competitiveness in the semiconductor market.
- Limitation of Process Equipment Process equipment often imposes constraints on the scaling of process nodes, affecting advancements in miniaturization.
- High Competition Resistance Rapid technological advancements demand continuous innovation to maintain an edge in the highly competitive semiconductor industry.
- Carefulness and Patience The intricate and precise nature of semiconductor manufacturing requires a high level of attention to detail and patience.
- Teamwork Effective collaboration among various teams, including design, engineering, and production, is essential for successful outcomes.

1.3.1 Limitation of 2nm Technology

- 2nm technology is relatively easier to manufacture compared to smaller nodes like 1nm but suffers from low yield.
- High application costs limit its mass production, making more mature nodes like 16nm or 24nm more feasible for large-scale applications.

1.4 IC Fabrication Process

In IC fabrication, several key steps are meticulously executed to create integrated circuits. Each step is essential to ensure precision, performance, and reliability. Below is a fine-tuned outline of the major stages involved:

1.4.1 Silicon Production

- **Source of Silicon**: Silicon is derived from sand, primarily made up of silicon dioxide (SiO_2).
- **Types of Silicon**:
  - **Crystalline**: Long-range order of atoms.
  - **Polycrystalline**: Medium-range order, many grains with grain boundaries.
  - **Amorphous**: Random, non-structured arrangement of atoms.

1.4.2 Purification of Silicon

- **Metallurgical Grade Silicon** (98% pure) is produced through reduction:

$$SiO_2 + C \rightarrow Si + CO_2$$

- This is further purified to semiconductor grade silicon (99.9999%) using chemical processes like:

$$SiHCl_3 \rightarrow Si + 3HCl$$

- The purified silicon is used for growing single crystal silicon through methods like the **Czochralski Process**.

Crystal Growth using Czochralski Process : A single solid seed crystal is rotated and slowly extracted from molten silicon to create a single crystal with precise purity and dimensions.

1.4.3 Oxidation and Silicon Dioxide Formation

- Oxidation occurs in tube furnaces (vertical or horizontal).
- **Diel-Groove Model**:
  - Oxide growth slows as thickness increases.
  - Silicon atoms are consumed during the reaction, forming a layer of SiO_2.
  - Oxide expansion leads to a compressive strength of 2.2 times the oxide thickness.

1.4.4 Oxidation Techniques in IC Fabrication

Oxidation Technique	Details
Dry Oxidation	**Chemical Reaction**: Si (solid) + O_2 (gas) $\rightarrow$ SiO_2 (solid)
	Process: - Wafer is loaded into the chamber. - Initially, $\mathbf{N_2}$ gas is used. - **Oxygen** is introduced when the maximum temperature is reached. - After oxidation, $\mathbf{N_2}$ is reintroduced to stop the process.
	Characteristics: - Slow process, used for thin oxide layers (¡1000 angstroms). - Results in better electrical characteristics.
Wet Oxidation	**Chemical Reaction**: Si + $2H_2O$ $\rightarrow$ SiO_2 + $2H_2$ Si + $2N_2O$ $\rightarrow$ SiO_2 + $2N_2$
	Process: - Wafers are heated in an atmosphere containing O_2, H_2O, or N_2. - Faster growth rate compared to dry oxidation.
	Characteristics: - Faster oxidation but with slightly lower electrical performance compared to dry oxidation. - Includes methods like vaporization, bubbling, baking, and direct injections.

1.4.5 Silicon Dioxide (SiO_2)

- **Properties of SiO_2**:
  - Excellent electrical insulator (resistivity greater than 10^{16} ohm·cm).
  - Energy gap: ~ 9 eV.
  - High breakdown electric field (greater than 10 MV/cm).
  - Stable and reproducible interface with Si.
  - Good diffusion barrier for dopants and etching selectivity between Si and SiO_2.
- **Use of SiO_2 as a Dielectric in MOSFETs**

  Silicon dioxide (SiO_2) is widely used as a dielectric material in MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors). It acts as an insulating layer between metal layers, such as the gate and source/drain regions, and the silicon wafer. This isolation prevents unwanted electrical leakage and ensures the proper functioning of MOSFETs. In addition, SiO2 serves as a gate dielectric, providing a stable and controlled environment for the electric field to modulate the flow of charge carriers. It also plays a crucial role in capacitive coupling between the gate and the channel, contributing to the efficient operation of MOSFET devices.

2 Comprehensive Guide to the Lithographic Process

2.1 Introduction to Lithography Concepts

Lithography is a cornerstone in the field of microfabrication and semiconductor manufacturing, enabling the creation of intricate patterns necessary for modern technology. The key concepts include:

- **Pattern Process:** Methodologies used to produce precise and intricate designs on a wafer surface.

- **Photomasks and Reticles:** Specialized tools containing the design patterns, serving as templates for the lithographic process.
- **Critical Dimension (CD):** The smallest feature size that can be reliably and accurately reproduced during the process.
- **Light Spectrum and Resolution:** The wavelength of light used determines the resolution, which is the ability to distinguish two closely spaced features on a pattern.
- **Overlay Accuracy and Budget:** Precision in aligning successive layers of patterns and the cumulative tolerance limits for feature placement on the wafer.
- **Process Latitude:** Indicates the robustness of the lithographic process in consistently producing features that meet defined specifications.

2.2 Evolution of Lithography Technology

Lithography has evolved significantly, transitioning from traditional darkroom techniques to highly sophisticated methods:

- **Darkroom Techniques:** Involved basic camera film-based processes.
- **PCB Processes:** Intermediate step, employing simpler patterning techniques.
- **Modern Photolithography:** Utilizes advanced optical systems and precise chemical processes for microfabrication.

2.3 Detailed Steps in the Photolithographic Process

Photolithography involves a series of meticulously executed steps to achieve high-precision patterns on a substrate:

2.3.1 Substrate Surface Preparation

1. **Cleaning:** Removal of contaminants such as grease, dust, or organic residues using solvents like acetone and isopropyl alcohol (IPA).
2. **Dehydration:** Eliminating moisture from the wafer surface to ensure proper adhesion of subsequent layers.
3. **Priming:** Application of an adhesion promoter, typically Hexamethyldisilazane (HMDS), which reacts with the wafer surface to enhance the bonding of the photoresist layer.

2.3.2 Spin Coating of Photoresist

- **Process:** A liquid photoresist is applied to the substrate and spun at high speeds to create a uniform thin film.
- **Photoresist Composition:**
  - **Solvent:** Determines the flow properties of the resist.
  - **Resin:** Provides the mechanical structure and stability.
  - **Sensitizer:** The photosensitive component that reacts to light.
  - **Additives:** Tailored to control specific resist properties such as adhesion or etch resistance.
- **Spin Curve:** Essential for controlling mask thickness and ensuring uniformity across the wafer.

2.3.3 Pre-Exposure Bake (Soft Bake)

- **Purpose:** Removes excess solvent from the resist to stabilize the film.
- **Conditions:** Typically performed at 90C for 1 minute on a hot plate or 30 minutes in a convection oven.

2.3.4 Alignment and Exposure

- **Alignment:** The photomask or reticle is aligned precisely with the wafer.
- **Exposure:** The photoresist is exposed to light, transferring the pattern from the mask to the resist.

2.3.5 Post-Exposure Bake (PEB)

- **Purpose:** Minimizes standing wave effects in the resist and enhances photochemical reactions.
- **Additional Role:** Can thermally activate image reversal or improve the resist profile for further processing.

2.3.6 Development

- The exposed areas of the resist (for positive resists) or unexposed areas (for negative resists) are removed using a developer solution, revealing the pattern.

2.3.7 Post-Development Bake (Hard Bake)

- **Purpose:** Hardens the resist to improve its resistance to subsequent etching processes.
- **Precaution:** Temperatures exceeding 130C may cause the resist to flow, leading to distortion.

2.4 Importance of DUV Tuning in Exposure

Deep ultraviolet (DUV) tuning is a critical step that refines resist profiles and enhances the fidelity of transferred patterns, ensuring high precision and accuracy.

2.5 Comparison of Alignment Marks

Alignment Mark	**Design Features**	**Applications**	**Advantages**
Traditional Alignment Mark	Basic geometric shapes like circles or squares.	Suitable for single-layer alignment tasks.	Simplicity and ease of implementation.
XPA Alignment Mark	Contains multiple phases (Extended Phase Array).	Used in complex lithographic processes for multi-layer alignment and overlay.	High accuracy and precision in alignment.
Multi Grating Alignment Mark	Composed of multiple grating lines in various orientations (horizontal, vertical, diagonal).	Useful for high-resolution lithography with fine details.	Enhances alignment precision and overlay accuracy.

Table 4: Comparison of Alignment Marks in Lithography

2.6 Immersion Lithography

Immersion Lithography:

- Involves using a liquid (typically water or other fluids) between the lens and the wafer to achieve higher Numerical Aperture (NA) by reducing refraction losses.

Key Concepts:

- **Total Internal Refraction**: $\text{NA} = n_s \sin(\theta)$, where:
  - n_s is the refractive index of the immersion liquid.
  - θ is the angle of incidence.

2.6.1 Immersion Lithography Bath Types

Bath Type	Description	Advantages/Challenges
Large Volume of Fluid in Container (Bath Type)	Large volume of immersion fluid surrounding the wafer stage.	• Challenges: – Stage moving issues due to large fluid volume. – Slower filling and relaxation times. • Solution: Special stage design to handle fluid movement efficiently.
Shower Type	Small fluid volume sprayed or directed onto the wafer stage.	• Advantages: – Short time constants for filling and relaxation. – Compatible with conventional wafer alignment techniques. • Benefit: Ensures better control over the immersion process and quicker transitions between exposures.

Table 5: Comparison of Immersion Lithography Bath Types

Resist Types Comparison

	Positive Resist	Negative Resist	Bright Field Resist
Definition	Light-sensitive material that is exposed where exposed to light. Developing removes unexposed areas.	Light-sensitive material that is exposed where not exposed to light. Developing removes exposed areas.	Exposed areas become soluble in developer (light creates a positive image).
Sensitivity	Reacts to light exposure to form a latent image.	Reacts to light exposure to form a latent image.	More sensitive to light, reacts to brightness.
Pattern Transfer	Exposed areas become solubilized in developer.	Exposed areas become insolubilized in developer.	Allows high contrast image transfer.
Applications	Used for standard photolithography.	Used for applications requiring high resolution.	Used in microelectronics, MEMS, etc.
Contrast	Moderate to high contrast for clear image.	High contrast for fine details.	High contrast for clear, bright images.
Development	Areas exposed to light dissolve.	Areas not exposed to light dissolve.	Positive resist used with bright light exposure.

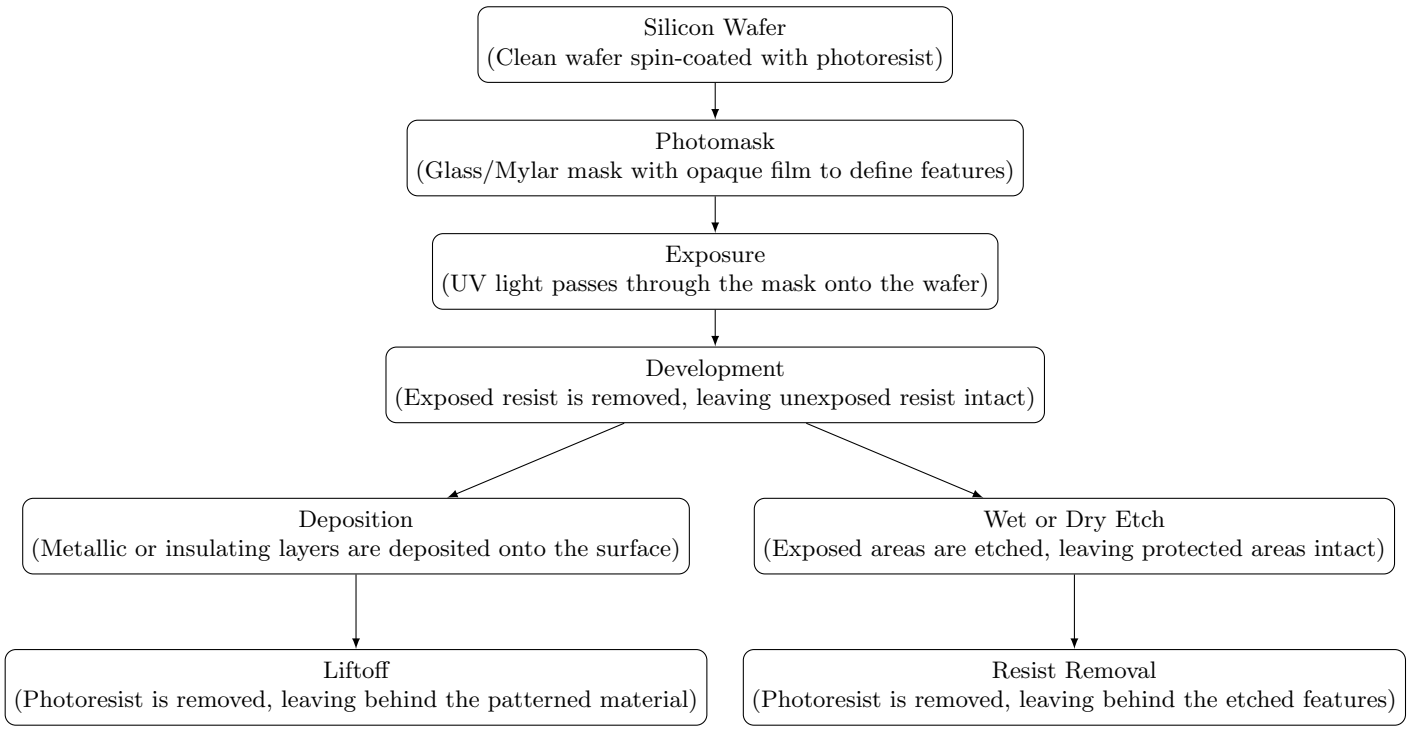
Table 6: Comparison of Resist Types

2.6.2 Comparative Analysis of Laser Lithography, Extreme Ultraviolet (EUV) Lithography, and Electron Beam (E-Beam) Lithography

Parameter	Laser Lithography	EUV Lithography	E-Beam Lithography
Resolution Limits	Utilizes DUV light at 193 nm wavelengths, achieving feature sizes down to approximately 20 nm through multiple patterning techniques.	Employs 13.5 nm wavelength light, enabling patterning of features as small as 7 nm and below, facilitating advanced node semiconductor fabrication.	Achieves resolutions below 10 nm due to the extremely short wavelengths of electrons, suitable for research and low-volume production requiring ultra-fine features.
Mask Patterns	Relies on photomasks containing the circuit patterns; mask fabrication is complex and costly, especially for advanced nodes.	Requires specialized masks with multilayer coatings to reflect EUV light; mask defects and contamination are significant concerns.	Operates maskless by directly writing patterns onto the resist, eliminating mask-related costs but resulting in slower throughput.
Substrate Preparation	Standard cleaning and priming procedures are sufficient; however, surface flatness becomes critical at smaller nodes.	Demands ultra-clean and extremely flat substrates to prevent defects, given the sensitivity of the process to surface imperfections.	Requires meticulous substrate preparation to avoid charging effects and ensure pattern fidelity, especially on insulating substrates.
Throughput	High throughput, capable of processing numerous wafers per hour, making it suitable for mass production.	Lower throughput compared to DUV lithography due to the complexity of the technology and current source power limitations.	Significantly lower throughput, as it writes patterns serially, making it impractical for high-volume manufacturing.
Yield	Mature technology with high yield rates; yield can decrease at advanced nodes due to process complexities.	Yield improvement is ongoing; challenges include defectivity and tool availability, impacting overall yield.	High precision leads to excellent pattern fidelity, but the slow writing process can introduce variability, affecting yield.
Mask Alignment	Advanced alignment systems ensure precise overlay of multiple layers, critical for complex integrated circuits.	Alignment precision is challenged by shorter wavelengths and thermal distortions; ongoing improvements aim to address these issues.	Direct writing eliminates mask alignment errors; however, stage positioning accuracy is crucial for pattern placement.
Equipment Complexity	Well-established equipment with a broad installation base; complexity increases with techniques like immersion and multiple patterning.	Highly complex systems requiring vacuum environments, specialized light sources, and reflective optics, leading to increased maintenance demands.	Complex electron optics and vacuum systems are necessary; however, the absence of masks simplifies certain aspects.
Cost	High initial capital expenditure with substantial ongoing costs for masks and maintenance, especially at advanced nodes.	Significantly higher costs due to complex equipment, mask fabrication, and operational expenses.	Lower capital costs without the need for masks but higher operational costs per wafer due to low throughput.
Applications	Predominantly used for mainstream semiconductor manufacturing up to the 7 nm node, with extensions through multiple patterning.	Essential for cutting-edge semiconductor devices at 7 nm and below, enabling further scaling of integrated circuits.	Ideal for prototyping, research, and low-volume production where ultra-high resolution is required.

Table 7: Comparison of Laser Lithography, EUV Lithography, and E-Beam Lithography

2.6.3 Photolithography Flowchart



3 Thin Film Deposition

Thin film deposition is the process of creating a thin layer of material (typically on the order of nanometers to micrometers) onto a substrate.

3.1 Comparison of PVD and CVD

Aspect	**PVD**	**CVD**
Mechanism	Physical processes like evaporation or sputtering.	Relies on chemical reactions of gaseous precursors.
Process Conditions	Vacuum or low-pressure environment.	Operates at various pressures, often high temperatures.
Temperature	Generally lower than CVD.	Higher temperatures are often required.
Material Flexibility	Limited to materials that can be evaporated or sputtered.	More materials can be deposited due to chemical flexibility.
Surface Coverage	May have shadowing effects, uneven coverage.	Provides better step coverage and conformality.
Equipment Cost	Typically less expensive.	More expensive due to complex equipment.
Advantages	• Cleaner process with minimal chemical waste. • Produces dense and pure films. • Better for high melting-point materials. • Simpler setup and relatively faster process.	• High uniformity and excellent conformal coatings. • Can deposit a wide range of materials. • Scalability for industrial applications. • Often used for depositing complex compounds.
Time Required	Depends on the deposition rate, typically faster.	Takes more time due to precursor reactions and higher temperatures.

Table 8: Comparison of PVD and CVD

3.2 What is Plasma

Plasma is often referred to as the fourth state of matter. It consists of ionized gases containing free electrons, ions, and neutral atoms or molecules. Plasma exhibits unique electrical and chemical properties, making it a crucial medium for thin film deposition, etching, and surface treatment.

3.2.1 What Is Plasma Physics Good For?

Plasma physics enables various applications in industrial, scientific, and medical fields, including:

- Enhancing reaction rates in plasma-enhanced chemical vapor deposition (PECVD).
- Enabling sputtering for thin film deposition in electronics and optics.
- Facilitating etching processes in semiconductor fabrication.

3.2.2 Cold Plasma vs. Hot Plasma

- **Cold Plasma**: The electron temperature is much higher than the ion temperature. Used in thin-film deposition and etching.
- **Hot Plasma**: Both ions and electrons are at high temperatures, commonly found in fusion reactors.

3.2.3 Plasma Reactions

- **Ionization**: $A \rightarrow A^+ + e^-$
- **Dissociation**: $AB + e^- \rightarrow A + B + e^-$
- **Excitation**: $A + e^- \rightarrow A^* + e^-$
- **Relaxation**: $A^* \rightarrow A + h\nu$ (photon emission)

The **dissociation step** is critical for deposition as it breaks down precursor molecules.

3.2.4 DC Plasma vs. RF Plasma Sputtering

Aspect	**DC Plasma**	**RF Plasma**
Working	Direct current ionizes the gas.	Alternating current ionizes the gas.
Preferred Use	For conductive materials.	For both conductive and dielectric materials.
Deposition	Positive ions accumulate on the cathode, causing deposition.	Alternating potential allows deposition on both electrodes.
Applications	Sputtering and etching of metals.	Sputtering and deposition of dielectrics and metals.
Limitation	Cannot sustain plasma for thick dielectric layers.	Better for thick dielectric films.

Table 9: Comparison of DC and RF Plasma

3.3 RF Sputtering Principles

3.3.1 RF Sputtering Method

In the RF sputtering method, the cathode and anode are connected in series with a blocking capacitor (C) (Figure 3). This capacitor is part of an impedance matching network that optimizes power transfer from the RF source to the plasma. All Vac Coat RF power supplies include an RF matching network to precisely tune the RF power, either manually or automatically.

The RF voltage is an alternating voltage expressed by Equation (1):

$$V_{\mathrm{RF}}(t) = V_{\mathrm{RF}} \sin(\omega t) \tag{1}$$

3.3.2 RF Sputtering Circuit

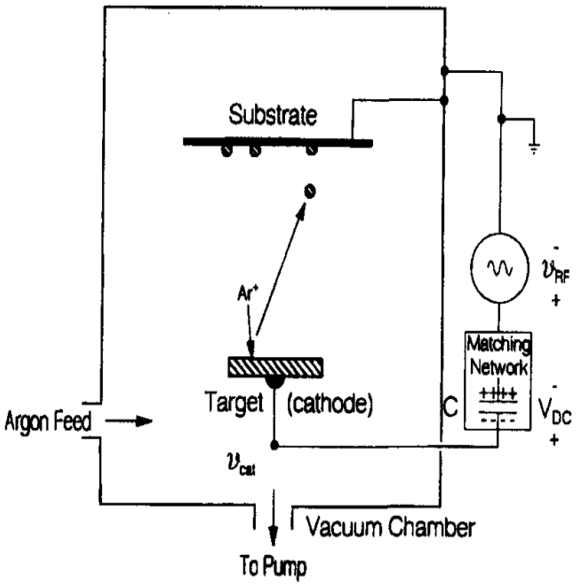
A schematic of the RF sputtering circuit is shown in Figure 3. If V_{RF} is set to about 500 V (Figure 4-a) without a blocking capacitor, the target current will exhibit the behavior shown in Figure 4-b. Since the plasma potential is close to ground, the current density oscillates between J_{ion} and $-qz$, depending on the sign of V_{RF}. As a result, the net current is not zero.

When a blocking capacitor is used and a self-bias DC voltage is applied, the cathode voltage is expressed by Equation (2) (Figure 4-c):

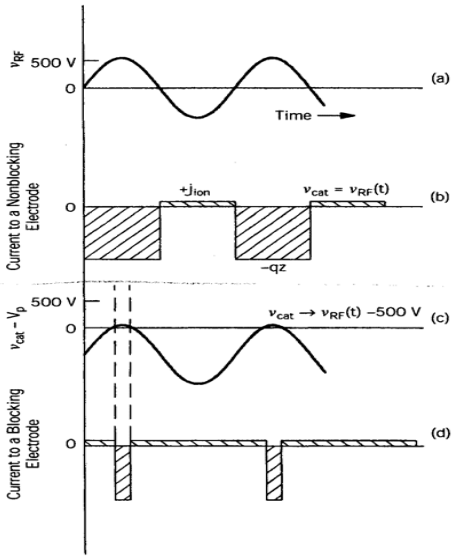
$$V_{\mathrm{cath}}(t) = V_{\mathrm{RF}}(t) - V_{\mathrm{DC}} \tag{2}$$

3.3.3 Electrode Voltage and Current Curves in an RF Circuit

The electrode voltage and current curves for an RF circuit demonstrate the importance of the blocking capacitor in ensuring net-zero current. Figure 4 illustrates the voltage and current characteristics for different configurations.



(a) RF Sputtering Circuit.



(b) Electrode Voltage and Current Curves in a RF Circuit.

Figure 1: Side-by-side comparison of RF Sputtering Circuit and its electrode characteristics.

3.3.4 Target Potential in RF Sputtering

In RF sputtering, the target potential is generally lower than the plasma potential. To achieve zero net current over an RF cycle, the electrode potential must remain negative for most of the cycle. When the cathode potential becomes positive, electrons bombard the target, charging it negatively. Due to their higher mobility and faster speed compared to argon ions, the time for electron bombardment must be reduced.

To ensure charge neutrality, the duration of target bombardment by argon ions is increased to neutralize the collected charge on the target surface. This balance is illustrated by setting the area under the electrode current curve, representing the average current, equal to zero.

3.3.5 Why 13.56 MHz is Used?

The frequency of 13.56 MHz is chosen for RF sputtering to avoid interference with telecommunication services. It is part of the ISM band, recommended by the ITU Radio Regulations (2012), with a bandwidth of 14 kHz.

Additionally, this frequency is low enough to allow sufficient time for momentum transfer between argon ions and the target. At higher frequencies, argon ions become immobilized, and electrons play a dominant role in sputtering, resembling an electron-beam evaporation process.

3.3.6 A Common Problem in RF Sputtering

One of the challenges in RF sputtering is the deposition of insulating (non-conductive) target materials. These materials, being poor conductors of heat and electricity, require a thin conductive backing plate to prevent thermal shock and charge accumulation.

The dielectric target surface must completely cover the conductive backing plate. If the metal backing plate is exposed to the electric field, the capacitance is short-circuited, leading to significant issues. This is a critical problem during plasma treatment, cleaning, or coating of dielectric surfaces.

3.4 CVD and Types of CVD

CVD is a process where one or more volatile precursors react and deposit thin films on a heated substrate through chemical reactions. The process is driven by the diffusive transport of gaseous species to the surface and numerous intermolecular collisions.

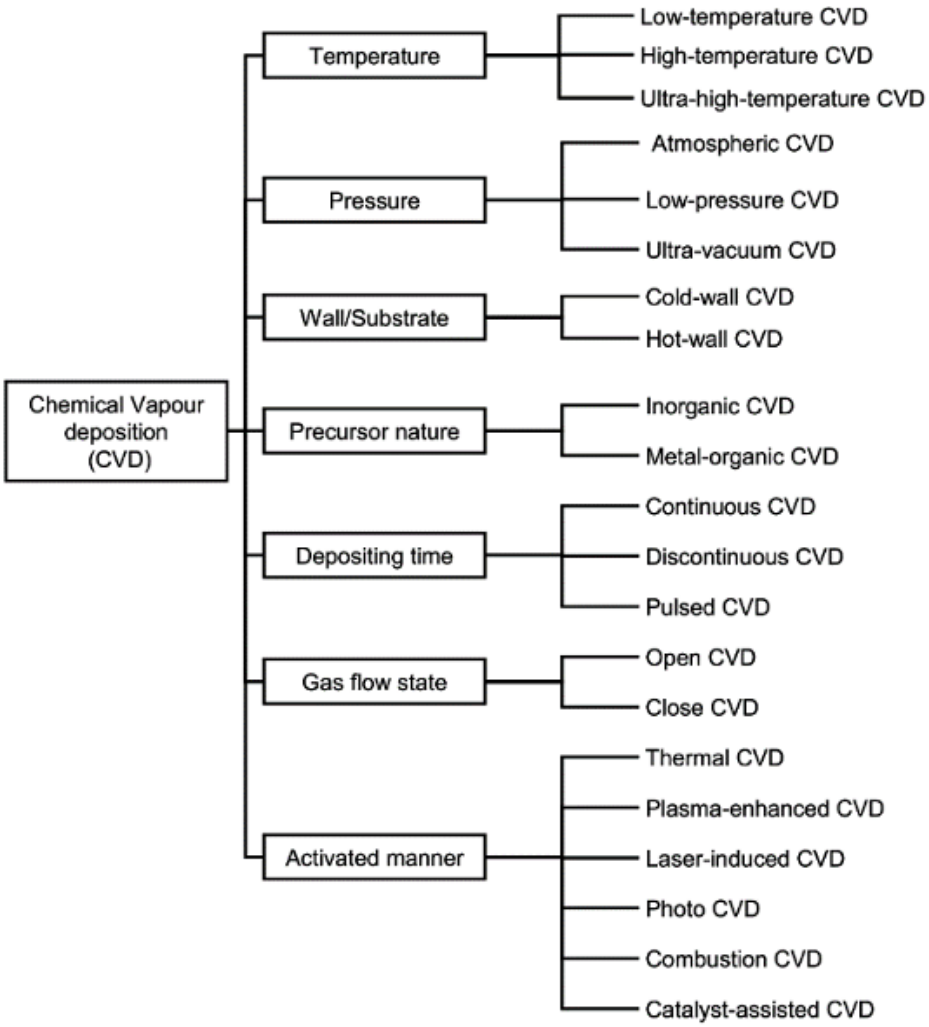


Figure 2: Types of CVD

3.4.1 Mechanism of CVD (Chemical Vapor Deposition)

CVD involves the chemical reaction of volatile precursors to deposit a thin film onto a substrate. The key steps in CVD include:

1. **Transport:** The precursor gases are transported to the reaction chamber, often involving diffusive and convective movements.
2. **Reaction:** On the heated substrate, the gases decompose or react, forming a thin solid film.
3. **Surface Reactions:** Adsorption, surface reaction, and migration occur on the substrate surface.
4. **Island Formation:** Small, distinct regions (islands) of the film grow and coalesce to form a continuous layer.
5. **Byproduct Transport:** Byproducts of the reaction are transported away, often in the bulk gas phase.

3.5 Fluid Mechanics in CVD

CVD involves different transport phenomena for the precursor species:

1. **Viscous Flow:** The movement of gases through channels or across surfaces.
2. **Diffusion:** Random movement of particles driven by concentration gradients.

3. **Convection:** Bulk movement of gases due to pressure or temperature gradients.
4. **Thermal Conductivity:** Heat transfer at the substrate interface, influencing the deposition rate and uniformity.

3.6 Growth Mechanism of CVD

The CVD growth can be categorized into different controls:

- Feed Rate Limited Growth
  - When feed rate is low and both transport and diffusion are fast, this allows for lower precursor vapor pressure.
  - If the feed rate is slow, transport-limited deposition occurs.
- Kinetic Control
  - Surface reactions are slow, limiting the growth rate.
- Diffusion Control
  - When diffusion limitations occur due to high molecular collisions or poor precursor transport.
- Desorption Control
  - Early surface reactions hinder deposition due to limited precursor availability at the surface.

3.7 Graphical Representation of CVD Growth Mechanisms

Graph Explanation: The CVD growth curve typically shows:

- An initial rapid increase in deposition rate.
- A leveling-off phase as transport becomes limiting.
- As feed rates decrease, diffusion or surface reaction mechanisms dominate, controlling the deposition rate.
- Under ideal conditions, a steady state with minimal variations in thickness and uniformity.
- Imperfections can lead to variations in film quality.
- Feed rate limited growth if both mass transport and diffusion are fast compared to feed. Often with low vapor pressure precursors.

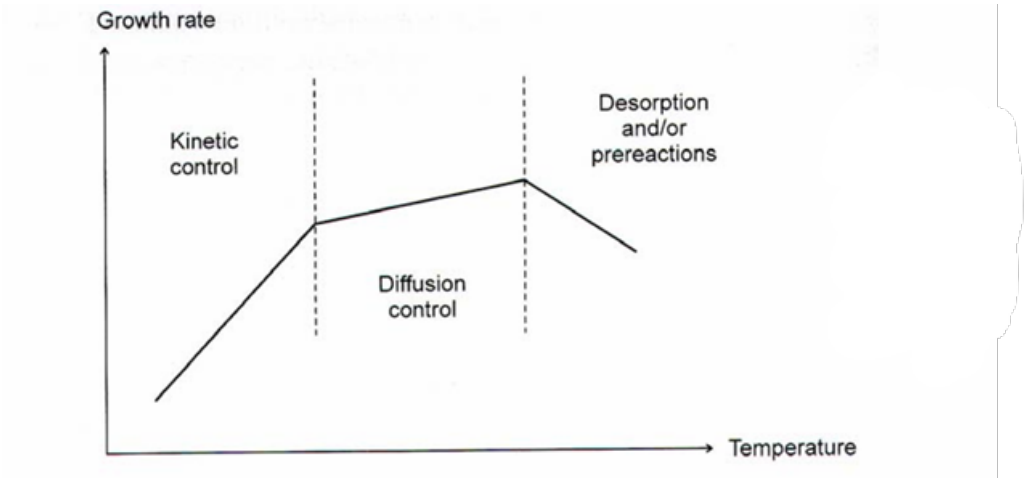


Figure 3: Dependence of the film growth rate on the substrate temperature.

3.8 Epitaxy

Epitaxy refers to the process of growing a crystalline layer of one material on the surface of another crystalline material. The growing layer has the same crystallographic orientation as the substrate. This process is commonly used in semiconductor manufacturing to create highly controlled, uniform layers of materials, essential for devices such as transistors, LEDs, and sensors.

3.8.1 Types of Epitaxy

- **Homoepitaxy:** Growth of a layer on a substrate of the same material.
- **Heteroepitaxy:** Growth of a layer on a substrate of a different material.

3.8.2 Molecular Beam Epitaxy (MBE)

- MBE involves the evaporation of elemental sources that are independently controlled to form molecular or atomic beams.
- These beams are then directed towards a substrate in a high-vacuum environment, typically under ultra-high vacuum (UHV) conditions (10^{-10} bar).
- The process occurs in a controlled atmosphere, eliminating contaminants that could degrade film quality.
- The substrate is maintained at elevated temperatures, ensuring the growth of high-quality, epitaxial layers.

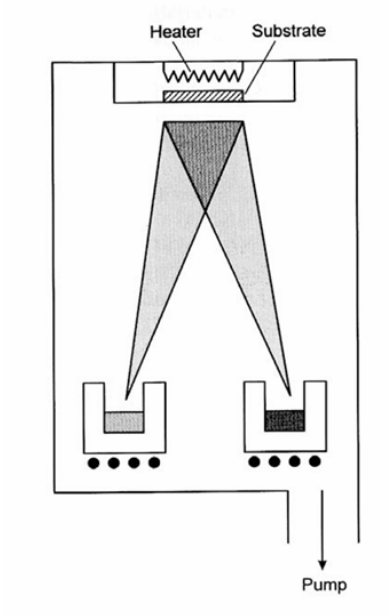


Figure 4: Molecular Beam Epitaxy (MBE)

3.9 Introduction to GAA and FinFET Technologies

3.9.1 FinFET Technology

FinFET (Fin Field-Effect Transistor) is a type of multi-gate transistor, where the gate surrounds the channel on three sides (two sides and the top). This structure improves the control over the channel, mitigating short-channel effects and enhancing performance at smaller nodes. FinFETs have become the standard for sub-22 nm nodes due to their better scalability, higher drive current, and lower leakage compared to traditional planar transistors.

3.9.2 GAAFET Technology

GAAFET (Gate-All-Around FET) is an evolution of FinFET technology. In GAAFETs, the gate fully surrounds the channel on all four sides, providing even more control over the channel. This design allows for superior electrostatic control and significantly reduces short-channel effects, enabling reliable operation at even smaller nodes (below 5 nm). GAAFETs promise improvements in performance, power consumption, and scalability compared to FinFETs, making them suitable for advanced semiconductor nodes like 3 nm and beyond.

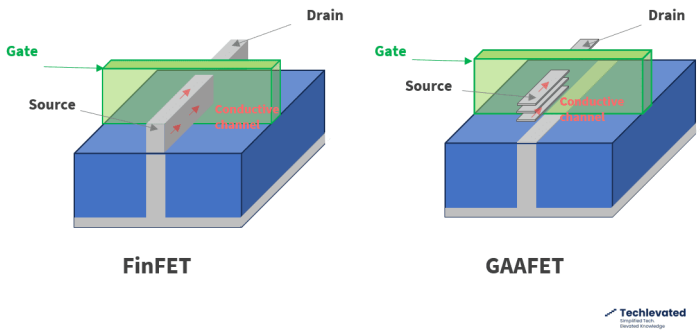


Figure 5: FinFet and GAA

3.9.3 Comparison between FinFET and GAAFET Technologies

Parameter	FinFET	GAAFET
Structure	Features a gate that surrounds three sides of a vertical fin-shaped channel.	Incorporates a gate that completely encircles the channel, providing superior electrostatic control.
Frequency Switching	Capable of high-frequency operation, but performance may degrade at smaller nodes due to increased leakage and reduced gate control.	Maintains high-frequency performance even at reduced dimensions, owing to superior gate control and reduced leakage currents.
Parameter	**FinFET**	**GAAFET**
Structure	Gate surrounds 3 sides of a fin-shaped channel.	Gate fully surrounds the channel (4 sides).
Channel Geometry	Fin height: 50-60 nm, Fin width: 5-7 nm.	Nanosheet width: 15-30 nm, Nanosheet thickness: 5-10 nm.
Drive Current	1.3 mA/m (at 7 nm node).	1.6 mA/m (at 7 nm node).
Power Consumption	Higher due to leakage currents, 1.0-1.2 W for advanced nodes.	Up to 45% reduction in power, 0.6-0.8 W for advanced nodes.
Performance Gain	Baseline performance at sub-7 nm nodes.	23% higher performance at 3 nm compared to FinFET.
Switching Frequency	Capable of 3-5 GHz operation.	Operates at similar or higher frequencies, with better energy efficiency.
Scalability	Limited below 5 nm due to short-channel effects and leakage.	Scalable below 5 nm with robust control over short-channel effects.
Short-Channel Effects	Noticeable degradation at 5 nm and smaller nodes.	Minimized, enabling effective operation at 3 nm and beyond.
Power Efficiency	30-40% efficiency improvement compared to planar transistors.	45% efficiency improvement compared to FinFETs at advanced nodes.
Performance Metrics	Standard for 7 nm and above nodes.	Achieves 16% area reduction, with better performance at similar or lower power consumption.
Fabrication Complexity	Moderate, relies on well-established processes for vertical fins.	Slightly more complex due to horizontal nanosheet stacking, but compatible with existing FinFET tools.

Table 10: Comparison of FinFET and GAAFET Technologies

Day 2 Summary of Semiconductor Manufacturing

- IC fabrication involves wafer preparation, fabrication, testing, assembly, and final testing.
- Key trends in semiconductor manufacturing include increased performance, reduced chip prices, and smaller feature sizes (from 350nm to 1-2nm).
- Devices are classified as micrometer (¿100nm) and nanometer (100nm) devices.
- Technological advancements are guided by Moore's Law, with wafer sizes increasing from 50mm to 300mm over time.
- FinFETs are 3D transistors that overcome the limitations of planar MOSFETs at the nanoscale.
- The advantages of FinFETs include reduced current leakage, improved power efficiency, and faster switching speeds.
- The FinFET fabrication process includes substrate preparation, fin formation, and chemical-mechanical planarization (CMP).
- Yield, price, equipment limitations, and competition are crucial factors in semiconductor manufacturing for cost-effectiveness and innovation.
- Precision, patience, and teamwork are key for success in the semiconductor industry.
- 2nm technology faces yield challenges, making larger nodes more practical for mass production.
- Silicon is purified from sand and grown into single crystals through the Czochralski process for semiconductor use.
- Oxidation forms SiO2, which acts as an insulator and dielectric material in MOSFETs.
- Dry oxidation provides better electrical characteristics compared to wet oxidation.

- Lithography is a critical process that involves patterning, photomasks, light spectrum control, and resolution management.
- The lithography process has evolved from traditional methods to advanced techniques such as immersion lithography, which uses liquid between the lens and wafer to improve resolution.
- Lithography technologies such as DUV, EUV, and E-beam lithography are compared based on parameters like resolution, mask patterns, cost, and applications.
- Thin film deposition techniques, such as PVD and CVD, are compared based on process conditions, temperature, surface coverage, and material flexibility.
- Plasma, as the fourth state of matter, is used in processes like PECVD, sputtering, and etching, with DC and RF plasma variations providing different characteristics.

Conclusion

The second day covered essential aspects of semiconductor manufacturing, focusing on the stages from wafer production to advanced lithographic techniques. FinFETs significantly improve transistor performance, while immersion and EUV lithography enhance miniaturization capabilities. Yield, precision, and cost-effectiveness remain vital, and emerging technologies such as GAAFETs and improved deposition methods are driving future innovation. These advancements ensure the semiconductor industry can continue meeting the increasing demands of modern electronics.

1 Summarization of Day 3: The Trends of Advanced Heterogeneous Integration Packaging and The Development of Semiconductor Industry and Technology in Taiwan

Speaker: Prof. Meng-Kai Shih and Dr. Yu-Hua Huang

1.1 Trends in Advanced Packaging Technology Development

Advanced packaging technologies are evolving to meet increasing demands for performance, miniaturization, and integration. Key trends include the development of heterogeneous integration, 3D packaging, and system-on-package designs.

- Driving Forces for Heterogeneous Integration Packaging Technology Heterogeneous integration is driven by the need for higher performance, reduced power consumption, and multifunctionality in compact form factors. This approach enables integration of diverse components like processors, memory, and sensors on a single platform.
- Analysis of Packaging Characteristics (I): Heat Dissipation Heat dissipation is critical to prevent overheating and maintain system reliability. Packaging design must consider materials and structures to efficiently transfer heat away from components.
- Analysis of Packaging Characteristics (II): Stress Analysis Stress analysis ensures mechanical stability and durability. Packaging must withstand thermal and mechanical stresses during operation to avoid failures such as cracking or delamination.
- Reliability Testing and Analysis Reliability testing assesses packaging performance under various conditions, including thermal cycling, mechanical stress, and environmental exposure. These tests validate long-term operational stability.

1.2 What's a Package and Why Do We Need It?

A package provides electrical, thermal, and mechanical support for electronic components. Its primary functions include:

- **Signal Distribution and Connection:** Ensuring reliable electrical connectivity and managing signal integrity through topological and electromagnetic considerations.
- **Power Distribution and Connection:** Addressing electromagnetic, structural, and material aspects to supply power effectively.
- **Heat Dissipation:** Managing thermal performance using appropriate structural and material solutions.
- **Protection of Components and Interconnections:** Safeguarding components from mechanical, chemical, and electromagnetic damage.

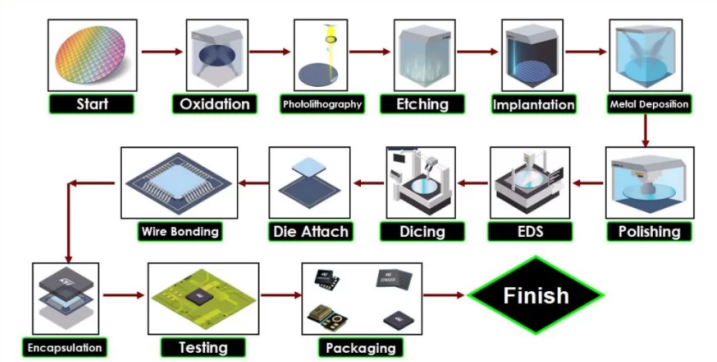


Figure 6: IC Fabrication Flow

1.3 Wafer Level Chip Scale Package (WLCSP)

Wafer Level Chip Scale Package (WLCSP) is an advanced packaging technology that integrates semiconductor devices directly on a wafer, providing a compact and highly efficient solution for modern electronic systems. This approach eliminates the need for traditional packaging substrates, reducing size and increasing performance. WLCSP incorporates multiple techniques such as FlipChip BGA, FI-WLP (Fan-In Wafer-Level Package), and SESUB (Semiconductor Embedded in Substrate) to provide versatile and high-density packaging solutions.

1.3.1 Overview of WLCSP

WLCSP directly attaches semiconductor die to a wafer surface, eliminating the need for intermediate packaging layers. The resulting package is typically smaller and lighter, which is essential for applications requiring compactness and portability, such as smartphones, wearables, and automotive systems. Additionally, this method enhances electrical and thermal performance, crucial for high-speed data transmission and efficient power management.

1.3.2 Advantages of WLCSP

- **Miniaturization**: WLCSP offers extreme miniaturization, allowing for more components in a smaller area, which is essential for modern IoT and mobile devices.
- **Form Factor**: Due to its compact design, WLCSP significantly reduces the footprint and weight, contributing to the development of slimmer and lighter electronic products.
- **Performance**:
  - **Thermal Performance**: Efficient heat dissipation is achieved by placing the die directly on the substrate, minimizing thermal resistance.
  - **Electrical Performance**: Optimized electrical performance through direct connections between the die and I/O pads, improving signal integrity and reducing latency.
- **Cost Effectiveness**: WLCSP reduces manufacturing costs by eliminating the need for additional substrate materials and simplifying assembly processes.

1.3.3 Challenges of WLCSP

- **I/O Limitation**: Due to the compact nature of WLCSP, the number of I/O pins is limited, typically capped at around 50 I/Os, which can be a bottleneck for high-performance applications requiring extensive connectivity.
- **BLRT Reliability**: Backside Laminate Reliability Test (BLRT) is a crucial consideration for ensuring long-term reliability, particularly for thermomechanical stress.
- **Integration Complexity**: Combining WLCSP with other packaging technologies such as Flip Chip Hybrid and SESUB adds complexity to the manufacturing and design process.
- **SESUB Challenges**: Semiconductor Embedded in Substrate faces challenges such as maintaining high accuracy in embedding, which is essential for reliable performance over time.

1.3.4 Use Cases of WLCSP

- Mobile Devices: Smartphones and wearables benefit from reduced size and improved performance.
- Automotive Systems: High integration in automotive electronics for navigation, safety, and control systems.
- Consumer Electronics: Devices requiring compact and efficient electronic integration, such as smart watches and medical devices.

1.4 Integrated Circuit (IC) Fabrication Technologies

Integrated Circuit (IC) fabrication technologies have evolved significantly to enhance performance, reduce power consumption, and minimize form factors. The primary methodologies include 2D, 2.5D, and 3D IC fabrication, each with distinct characteristics.

1.4.1 2D IC Fabrication

In traditional 2D ICs, all components reside on a single planar substrate. This approach is straightforward and cost-effective but faces limitations in performance and miniaturization due to longer interconnects and increased signal delays.

1.4.2 2.5D IC Fabrication

2.5D IC technology places multiple dies side by side on an interposer, typically made of silicon. This configuration shortens interconnect lengths compared to 2D ICs, enhancing performance and enabling heterogeneous integration of different technologies within a single package.

1.4.3 3D IC Fabrication

3D ICs involve stacking multiple dies vertically, interconnected through technologies like Through-Silicon Vias (TSVs). This architecture significantly reduces interconnect lengths, leading to improved performance and reduced power consumption. However, 3D ICs present challenges in heat dissipation and manufacturing complexity.

1.4.4 Comparison of IC Fabrication Technologies

Parameter	2D ICs	2.5D ICs	3D ICs
Die Arrangement	Single die on a planar substrate	Multiple dies placed side by side on an interposer	Multiple dies stacked vertically
Interconnect Length	Longest interconnects	Shorter interconnects than 2D	Shortest interconnects
Performance	Limited by longer interconnects	Improved over 2D due to reduced interconnect lengths	Superior due to minimal interconnect lengths
Power Efficiency	Lower due to longer interconnects	Better than 2D	Highest, owing to reduced interconnect lengths
Thermal Management	Easier to manage	Better than 3D due to planar arrangement	Challenging due to vertical stacking
Manufacturing Complexity	Simplest fabrication process	More complex than 2D; requires precise interposer alignment	Most complex; involves TSVs and alignment of multiple layers
Heterogeneous Integration	Limited	Supports integration of different technologies within a single package	Supports integration but with increased complexity

1.4.5 Leading-Edge Technologies by Intel and IBM

- **Intel's EMIB (Embedded Multi-die Interconnect Bridge)**
  Intel utilizes EMIB in its 2.5D packaging, allowing high-density interconnections between heterogeneous dies without a full silicon interposer. This approach enhances performance and flexibility in integrating various components.
- **Intel's Foveros Technology**
  Foveros represents Intel's advancement in 3D IC technology, enabling vertical stacking of logic chips. This innovation allows for increased functionality within a smaller footprint, improving performance and power efficiency.
- **IBM's 3D Integration Research**
  IBM has been at the forefront of 3D IC research, focusing on stacking multiple layers of active devices to enhance performance and reduce power consumption. Their work addresses challenges in thermal management and manufacturing processes associated with 3D integration.

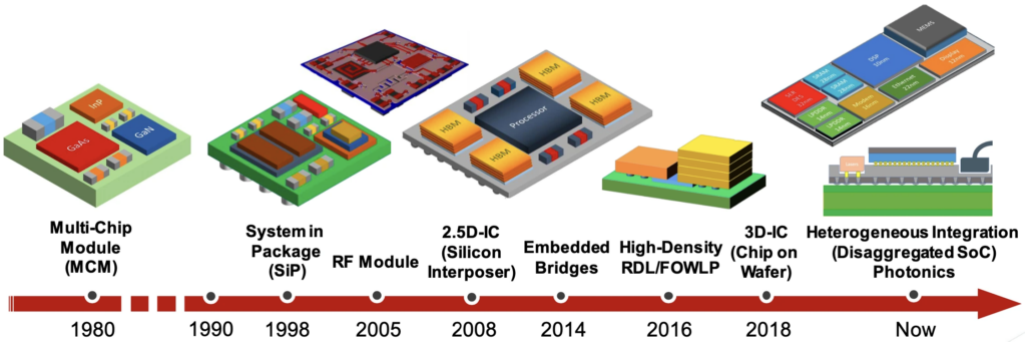


Figure 7: Evolution of IC Packaging

In summary, while 2D IC fabrication is straightforward, it faces limitations in performance scaling. 2.5D and 3D IC technologies offer pathways to overcome these challenges, with leading companies like Intel and IBM developing innovative solutions to harness the benefits of these advanced packaging techniques.

1.5 Advanced Semiconductor Packaging: 2.5D Interposer vs. EMIB

In advanced semiconductor packaging, both 2.5D Interposer and Embedded Multi-die Interconnect Bridge (EMIB) technologies enable high-density integration of multiple dies within a single package. While they share the objective of enhancing performance and reducing form factors, they differ in design, implementation, and trade-offs.

1.5.1 2.5D Interposer

In 2.5D packaging, multiple dies are placed side by side on a silicon interposer, which serves as a high-density interconnect substrate. The interposer incorporates Through-Silicon Vias (TSVs) to facilitate communication between the dies and the package substrate. This interposer acts as a bridge between the chips and the board, providing increased I/O and bandwidth.

1.5.2 Embedded Multi-die Interconnect Bridge (EMIB)

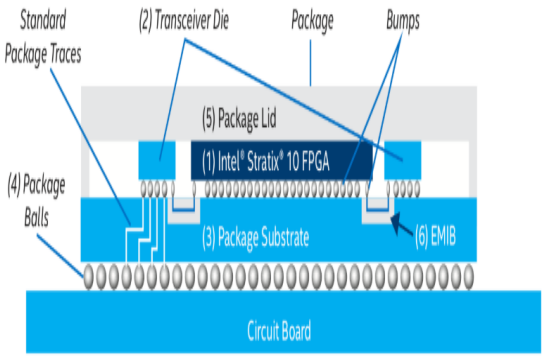
Developed by Intel, EMIB embeds small silicon bridges within the package's organic substrate to connect adjacent dies. Unlike the large interposer in 2.5D designs, EMIB places these silicon bridges only where high-density connections are necessary, eliminating the need for a full interposer. This approach reduces cost and complexity while maintaining high interconnect density.

1.5.3 Comparison of 2.5D Interposer and EMIB

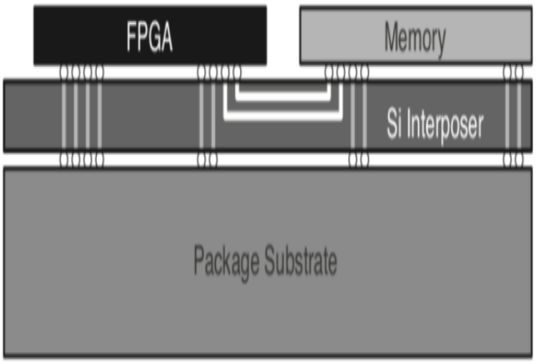
Parameter	2.5D Interposer	EMIB
Structure	Large silicon interposer beneath all dies, incorporating TSVs	Small silicon bridges embedded within the organic substrate, placed only where needed
Interconnect Density	High-density connections across the entire interposer	High-density connections localized to specific areas between dies
Manufacturing Complexity	Requires fabrication and alignment of a large interposer with TSVs	Involves embedding multiple small silicon bridges within the substrate
Cost	Higher, due to the large silicon interposer and TSV fabrication	Lower, as it eliminates the need for a full interposer
Thermal Management	Challenges due to the large interposer potentially impeding heat dissipation	Improved, as the absence of a full interposer allows for better thermal management
Scalability	Limited by the size of the interposer and TSV complexity	More scalable, as additional bridges can be embedded as needed without a full interposer
Applications	Suitable for high-performance computing requiring extensive inter-die communication	Ideal for designs needing high-density interconnects in specific areas, offering flexibility and cost benefits

1.5.4 Leading-Edge Technologies by Intel and IBM

- **Intel's EMIB**
  Intel's EMIB technology integrates small silicon bridges within the package substrate to connect multiple dies. This method provides high-density interconnects without the need for a full silicon interposer, reducing cost and complexity.
- **IBM's Bridge Technologies**
  IBM has developed its own bridge technologies, such as the Direct Bonded Heterogeneous Integration (DBHi), which differ from Intel's EMIB in aspects like bump structures and assembly processes. For instance, IBM's approach may utilize standard flip-chip assembly methods, offering distinct advantages in certain applications.



(a) EMIB implementation (silicon bridge). Source: Intel



(b) FPGA + HBM in 2.5D package with interposer. Source: Xilinx

Figure 8: Intel's EMIB package and Xilinx Package with Interposer

While both 2.5D Interposer and EMIB technologies aim to enhance multi-die integration, they differ significantly in design, cost, thermal management, and scalability. Intel and IBM continue to innovate in this space, developing solutions tailored to specific performance and application requirements.

1.6 Thermal Management in Semiconductor Packaging

Thermal management is crucial in semiconductor packaging to ensure device reliability and performance. As power densities increase, effective heat dissipation becomes essential to prevent issues like thermal runaway and high leakage power.

1.6.1 Thermal Stress in Packaging

Thermal stress arises from temperature variations causing expansion or contraction in materials with differing coefficients of thermal expansion (CTE). In semiconductor packages, mismatched CTEs between the silicon die, packaging materials, and the printed circuit board (PCB) can lead to mechanical stress, potentially causing delamination, cracking, or solder joint failures.

1.6.2 Fan-Out Wafer-Level Packaging (FOWLP)

Fan-Out Wafer-Level Packaging (FOWLP) is an advanced technology that redistributes I/O pads beyond the chip footprint, enabling more external connections without increasing the die size. This design enhances thermal performance by:

- Providing better heat dissipation pathways,
- Reducing thermal resistance,
- Mitigating hotspots.

By improving heat spreading, FOWLP addresses thermal runaway, where increased temperatures lead to higher leakage currents, creating a detrimental feedback loop.

1.6.3 Levels of Thermal Management

1. **Die Level:** Thermal management involves optimizing transistor layouts, using materials with high thermal conductivity, and implementing on-die cooling solutions to dissipate heat efficiently.
2. **Package Level:** Techniques like heat spreaders, thermal interface materials (TIMs), and heatsinks are used to transfer heat from the die to the external environment. Advanced methods, such as FOWLP, further enhance thermal performance.

3. **Board Level:** Thermal vias, heat pipes, and high-conductivity PCB materials manage heat dissipation from the package to the PCB, ensuring efficient heat spreading.
4. **System Level:** System-level management involves cooling systems such as fans, liquid cooling, and airflow designs to maintain optimal operating temperatures across the entire device.

1.6.4 Hotspots and High Leakage Power

Hotspots are localized areas on the die with significantly higher temperatures due to concentrated power density. These hotspots can exacerbate leakage currents, leading to increased power consumption and thermal runaway. Effective strategies, such as power distribution optimization and advanced cooling solutions, are essential to mitigate these issues.

1.6.5 Thermal Runaway

Thermal runaway is a condition where increasing temperature leads to higher leakage currents, generating more heat and further elevating temperatures in a self-reinforcing cycle. Robust thermal management solutions at all levels are essential to prevent this phenomenon.

1.6.6 Modes of Heat Transfer

Thermal management relies on three primary modes of heat transfer:

- **Conduction**
  Heat transfer through a solid material occurs via conduction, governed by Fourier's Law:

$$q = -k \cdot A \cdot \frac{dT}{dx}$$

  where:
  - q: Heat transfer rate (W),
  - k: Thermal conductivity of the material (W/m·K),
  - A: Cross-sectional area perpendicular to heat flow (m^2),
  - $\frac{dT}{dx}$: Temperature gradient (K/m).

- **Convection**
  Heat transfer between a solid surface and a fluid in motion is described by Newton's Law of Cooling:

$$q = h \cdot A \cdot (T_s - T_\infty)$$

  where:
  - q: Heat transfer rate (W),
  - h: Convective heat transfer coefficient ($W/m^2 \cdot K$),
  - A: Surface area (m^2),
  - T_s: Surface temperature (K),
  - T_∞: Fluid temperature away from the surface (K).

- **Radiation**
  Heat transfer through electromagnetic waves is given by the Stefan-Boltzmann Law:

$$q = \epsilon \cdot \sigma \cdot A \cdot (T^4 - T_{\text{sur}}^4)$$

  where:
  - q: Heat transfer rate (W),
  - ϵ: Emissivity of the surface (dimensionless),
  - σ: Stefan-Boltzmann constant (5.67×10^{-8} $W/m^2 \cdot K$),
  - A: Surface area (m^2),
  - T: Absolute temperature of the surface (K),
  - T_{sur}: Absolute temperature of the surrounding environment (K).

1.7 Passive and Active Heatsinks in Thermal Management

Efficient thermal management in semiconductor packaging requires the use of heatsinks to improve heat dissipation. Below is an overview of passive and active heatsinks, their characteristics, applications, and roles in mitigating thermal stress and preventing thermal runaway.

1.7.1 Passive Heatsinks (HS)

- Passive heatsinks rely on natural heat dissipation through conduction, convection, and radiation without requiring additional energy input.
- Typically made of high thermal conductivity materials, such as aluminum or copper.
- Heat is transferred from the heat source (e.g., silicon die) to the heatsink, which dissipates it into the surrounding environment.

1.7.2 Active Heatsinks (HS)

- Active heatsinks integrate additional cooling mechanisms, such as fans or liquid cooling, to enhance heat dissipation.
- Forced airflow or liquid circulation significantly increases the thermal transfer rate.

1.7.3 Key Differences Between Passive and Active Heatsinks

Parameter	**Passive Heatsinks**	**Active Heatsinks**
Cooling Mechanism	Natural convection	Forced convection or liquid cooling
Components	Metal fins	Metal fins + fans/pumps
Efficiency	Lower cooling capacity	Higher cooling capacity
Power Requirement	None	Requires external power
Maintenance	No maintenance required	Requires maintenance (e.g., fan cleaning)
Applications	Low to medium power devices	High-power or high-performance devices

1.7.4 Implementation of Passive and Active Heatsinks in Thermal Management Levels

1. **Die Level:** Advanced TIMs (thermal interface materials) optimize heat transfer between the die and the heatsink.
2. **Package Level:**
   - Passive heatsinks are often paired with vapor chambers to distribute heat evenly.
   - Active heatsinks with fans can be attached directly to the package for more efficient heat removal.
3. **Board Level:** Heatpipes or embedded cooling structures (e.g., copper layers in PCBs) can work alongside passive/active heatsinks.
4. **System Level:** Active cooling systems like liquid cooling loops or fan arrays augment the heatsink's performance, especially in server systems or gaming rigs.

1.7.5 Thermal Runaway Mitigation with Heatsinks

- **Passive Heatsinks:** Sufficient to handle moderate thermal loads, preventing the initial onset of thermal runaway.
- **Active Heatsinks:** Essential in high-power systems where passive solutions fail, effectively breaking the thermal runaway cycle.

1.7.6 Combining Passive and Active Solutions

In many systems, a hybrid approach is used:

- Passive heatsinks handle base thermal dissipation.
- Active components like fans boost cooling during peak thermal loads.

This synergy ensures both efficiency and performance, especially in variable workloads.

1.8 Comprehensive Thermal and Mechanical Stress Management

The following tables provide a detailed overview of key concepts, sources, and test types related to thermal and mechanical stress management in semiconductor packaging.

- **Stress vs. Strength Overview**

Category	**Definition**
Stress	External forces or conditions causing potential damage to an object.
Strength	Ability of the material or object to resist damage from stress.
Failure Condition	Occurs when Stress > Strength.

- **Sources of Stress and Strength**

Source	Examples
Manufacturing	Wafer grinding, sawing, die attach, wire bonding, molding.
Package-Level	Thermal stress, reliability testing, shipping, SMT.
PCB-Level	Reliability testing, shipping, assembly.
Material	Elasticity, ductility, toughness.
Design	Stress-distribution optimization, geometry adjustments.
Manufacturing	Process quality control.

- **Reliability Testing and Mechanical Testing**

Test Type	Purpose	Parameters
Thermal Cycling	Simulates temperature variations.	-40°C to 125°C, 50 min/cycle.
Cycling Bend	Tests mechanical flexibility.	Deflection: 1–3 mm, Frequency: 1–10 Hz.
Drop Test	Tests mechanical impact.	Acceleration: 1500 G, Pulse: Half-sine, Velocity change: 4.67 m/s.
Vibration Test	Simulates vibration during shipping.	Frequency span: 1–10 Hz.
Lead Pull Test	Tests solder joint strength.	Based on customer-specific configurations.

- **JEDEC vs. Free Drop Comparison**

Aspect	JEDEC Drop Test	Free Drop Condition
Test Setup	Standardized setup for predictable results.	Real-world scenarios with random forces.
Stress Variability	Lower variability in stress conditions.	Higher variability due to random impacts.
Parameters	Predefined acceleration, duration, and waveform.	Depends on drop height, surface, and object.

- **Failure Scenarios and Stress Mitigation**

Stage	Stress Sources	Possible Failure
Wafer	Grinding, sawing, die attach.	Cracks, delamination.
Package	Thermal stress, reliability tests.	Solder joint cracks, warping.
PCB	Vibration, assembling.	Solder pad detachment, broken traces.
Product	Recycling, environmental exposure.	Overall system failure, physical damage.

2 Semiconductor Outlook for 2025: Hsinchu Science Park (HSP)

2.1 Hsinchu Science Park Overview

- Established in 1980 to enhance Taiwan's high-tech industries.
- Primary focus: Semiconductor, computer, telecommunications, LCD panels, optoelectronics.
- HSP hosts leading semiconductor companies: TSMC, UMC, and supported by ITRI.
- Collaboration with academic institutions: NTHU, NYCU.
- Home to five national research laboratories, including the National Synchrotron Radiation Center.

2.2 Advantages of HSP

- Geographical proximity fostering academia-industry collaboration.
- Innovation ecosystem combining education, research centers, and top-tier foundries.
- Leading position in the semiconductor industry with continued innovation and expansion in 2025.

2.3 Growth Drivers of the Semiconductor Industry

The semiconductor industry is experiencing significant growth driven by several key factors:

- **AI Driving Semiconductor Growth:** The increasing use of aluminum (Al) applications is becoming a major driver for semiconductor industry expansion, expected to continue driving growth in the next five years.
- **Regionalization of Global Supply Chain:** Countries are focusing on developing domestic semiconductor industries and promoting regional supply chains to enhance self-reliance and reduce dependency on global networks.
- **Increased Demand for Advanced Processes:** The rise of artificial intelligence (AI) is fueling demand for advanced semiconductor processes, including memory technologies and advanced packaging, which are essential for improved performance and efficiency.
- **Diverse Applications of Advanced Packaging:** The adoption of 2.5D and 3D packaging technologies is revolutionizing high-end computing by enhancing chip performance, minimizing packaging area, reducing power consumption, and fostering cross-industry collaboration in a competitive market environment.

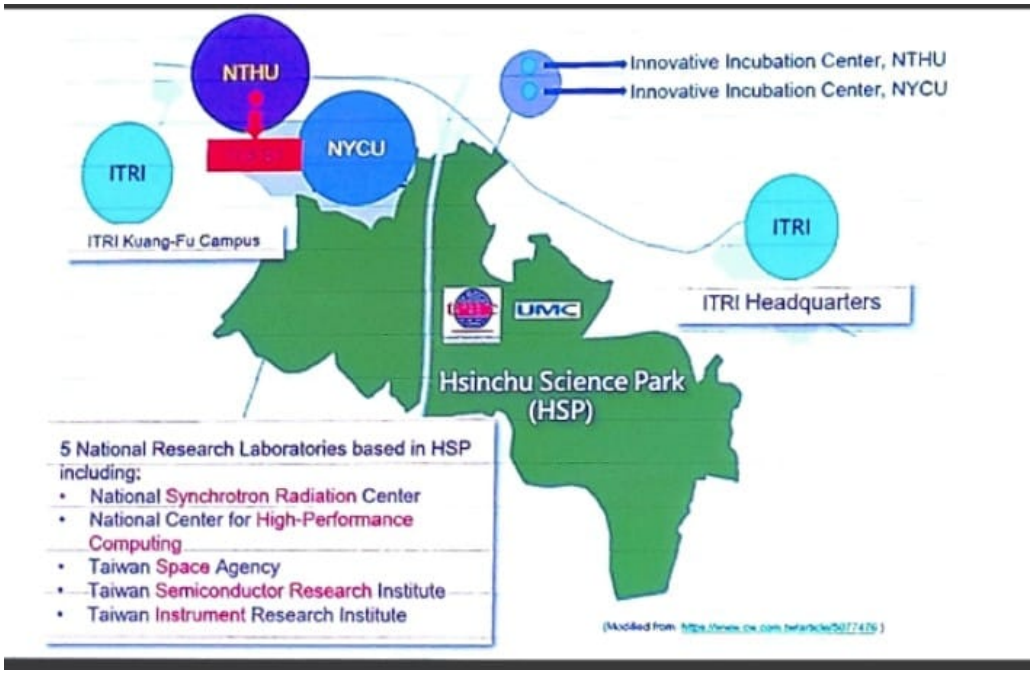


Figure 9: Advantages of Geographical Location

Conclusive Learnings from Day 3

1. **Trends in Advanced Packaging Technology Development** Advanced packaging technologies are evolving to meet the demand for higher performance, miniaturization, and integration. Key trends include heterogeneous integration, 3D packaging, and system-on-package designs. These innovations enable the integration of diverse components like processors, memory, and sensors into compact, high-performance platforms.
2. **Driving Forces for Heterogeneous Integration** The demand for multifunctionality, reduced power consumption, and compact form factors drives heterogeneous integration. This approach integrates various components into a single platform, enhancing system efficiency and functionality.
3. **Thermal and Mechanical Stress Management** Thermal management is critical for maintaining reliability and performance. Effective packaging designs address heat dissipation through materials and structures, ensuring system stability and reducing risks like cracking or delamination. Reliability testing under various conditions validates long-term operational stability.
4. **Wafer Level Chip Scale Package (WLCSP)** WLCSP offers extreme miniaturization and integrates semiconductor devices directly onto a wafer, eliminating traditional substrates. This reduces size, increases performance, and enhances both thermal and electrical performance, making it ideal for mobile, automotive, and IoT applications.
5. **Integrated Circuit Fabrication Technologies** The evolution from 2D to 3D IC technologies has improved performance, reduced power consumption, and minimized form factors. 2.5D and 3D ICs provide pathways for enhanced multi-die integration, addressing challenges such as heat dissipation and manufacturing complexity.
6. **Advanced Semiconductor Packaging: 2.5D vs. EMIB** Both 2.5D Interposer and EMIB enable high-density integration, but differ in design, cost, and thermal management. EMIB offers localized high-density connections with reduced manufacturing complexity compared to traditional 2.5D approaches.

7. **Thermal Management Techniques** Effective thermal management is achieved through passive and active heatsinks, and advanced packaging technologies like Fan-Out Wafer-Level Packaging (FOWLP) that enhance heat dissipation. Thermal stress management, along with strategies like thermal cycling and vibration tests, ensures reliability in semiconductor packaging.
8. **Semiconductor Outlook for 2025: Hsinchu Science Park** Hsinchu Science Park continues to lead Taiwan's semiconductor industry with a focus on innovation, collaboration between academia and industry, and advancements in technology such as AI-driven semiconductor processes and regional supply chain development.

3 Used Abbreviations

The following table lists the abbreviations used in this report along with their respective full forms and relevance:

Abbreviation	**Full Form**	**Relevance**
UBM	Under Bump Metallization	Essential for flip-chip packaging, enabling connections between IC and PCB
TSV	Through-Silicon Via	Key technology in 3D IC stacking
KGD	Known Good Die	Ensures quality control in die-level semiconductor manufacturing
CoWOS	Chip-on-Wafer-on-Substrate	Advanced packaging technology for high-performance computing
inFO	Integrated Fan-Out	High-density, low-profile packaging solution
TSOP	Thin Small Outline Package	Compact packaging for memory devices
BGA	Ball Grid Array	Common IC packaging for enhanced connection reliability
SMT	Surface-Mount Technology	Enables miniaturization in electronics assembly
DRAM	Dynamic Random-Access Memory	Widely used volatile memory in computing
SMRA	Semiconductor Manufacturing Resource Allocation	Optimizes resource use in fabs
FC-BGA	Flip Chip Ball Grid Array	High-performance IC packaging technique
HEPA Filters	High-Efficiency Particulate Air Filters	Critical for maintaining cleanroom standards in fabs
EMIB	Embedded Multi-Die Interconnect Bridge	Advanced interconnect technology for heterogeneous integration
CMP	Chemical Mechanical Planarization	Process for achieving flat wafer surfaces
DIBL	Drain-Induced Barrier Lowering	Important parameter in transistor scaling
SESUB	Semiconductive Embedded Substrate	Innovative IC packaging method for miniaturization
MEMS	Micro-Electro-Mechanical Systems	Key in sensors and actuators for IoT
BLRT	Below-Lithography Resolution Technology	Addresses challenges in advanced lithography nodes