IIT Guwahati - Department of Computer Science & Engineering

CS 223- Computer Organization & Architecture – End Semester Examination (13.06.2020)

Duration: 90 minutes **Paper Code: 7CM28**

A. Consider a 5x5 mesh NoC that uses input buffered routers. All routers employ XY routing. At a given clock cycle, router 17, receives 5 packets whose details (P-ID, Src, Dest) are given in the table. The priority value of a packet is the number of hops the packet has to traverse to reach its destination from the current router. This priority value is used to resolve conflicts during output port allocation. Larger priority value has higher priority. Draw a table similar to one given below that contain various information regarding input port and output port assigned to each packet. Fill up the missing entries in the table.

P-ID	Src	Dest	Priority value	Possible Input Port (N/S/E/W/L)	Desired Output Port (N/S/E/W/L)	Output allocation (Buff/N/S/E/W/L)	Remarks
P1	15	19					
P2	18	0					
P3	17	20					
P4	22	12					
P5	2	22					

B. Consider a TCMP system with a 4x4 mesh NoC where each tile consists of a superscalar processor, a private L1 cache and a shared distributed L2 cache. Let T0, T1, T2... ,T15 corresponds to the tiles where T0 is the bottom left tile and T15 is the top right tile. The total on-chip L2 cache is 4MB. The direct mapped L1 cache per tile is 16KB in size and is having a block size of 32B. L2 cache uses 128B block and is 16-way associative. Each L2 cache on chip has all the 16 ways of the sets assigned to it. The L2 cache is shared and distributed across all tiles. The L2 cache memory per tile division is such that total sets in L2 cache are uniformly partitioned across all tiles in sequential fashion. The TCMP uses 32-bit words. Consider a 3-cycle NoC router and a 1-cycle link for the NoC that uses XY routing. Packet injection and ejection require 1 cycle each, and hit/miss logic in L2 cache requires 3 cycles. Inter-router link-bandwidth is 64 bits. The system uses 4GB physical memory. Tile T4 encountered an L1 cache misses for the memory address M1=0x42046800.

(a) How many bits will be there in the tag field of the L2 cache block?
(b) How many words can be kept in an L1 cache block?
(c) List the path of routers through which cache miss request generated for M1 will travel.
(d) What is the latency of the cache miss request packet generated for M1?