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Code: 7CM28

Q1)

20	21	22	23	24
15	16	17	18	19
10	11	12	13	14
5	6	7	8	9
0	1	2	3	4

PId	Src	Dest	Priority value	Input port	Output Port (Desired)	output allocation	Remark
P1	15	19	4	W	E	E	
P2	18	0	6	E	W	W	atlast
P3	17	20	3	L	W	Buffer	
P4	22	12	2	N	S	S	
P5	2	22	4	S	N	N	

↳ Since P2, P3, have desired output to be W hence their allocation is done using priority values.

↳ Since P2 has max priority value hence higher priority. Hence rest of them have to be in buffer.

Remarks: P1 get E because of no conflict

→ P2 get W because of higher priority than P3.

↳ P3 will get buffer due to lower priority than P2.

↳ P4 will get S because of no conflict.

↳ P5 will get N because of no conflict.

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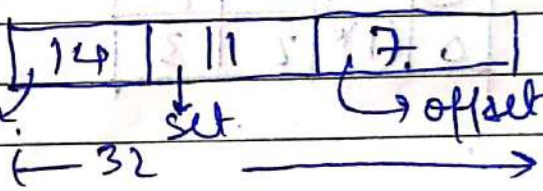
Q2) Soln: For L2: total size = 4MB = 2^{32}
Block size = 128 = 2^7 bytes
↳ 16 set associative = 2^4 associative.

No. of sets = $\frac{2^{22}}{2^7 \times 2^4} = 2^{11}$.

Hence req^n no. of set bits = 11.
∴ Physical address ⇒ Physical memory size = 4GB = 2^{32} B
Hence, physical address will be of 32.

(a) L2 cache block:

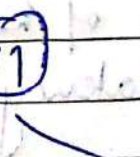


↳ Block offset will be of 7 bits because Block size = 2^7 = 128 bytes.

No. of bits in tag field = 14 Ans.

(b) L1 cache block:
Since block size = 32 Bytes = 2^8 bits.
and each word size = 32 bits = 2^5 bits.
⇒ No of words in each block = $\frac{2^8}{2^5}$ = 8 words. Ans.

(c) MI → 0x42046800
Out of 11 bits of set index



↳ because there are 16 tiles = 2^4 tiles.

this will show the tile no.

↳ set no.

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0x 42046800 → 0100 0010 0000 0100 0110 1000 0000

↳ M bits → tag.

↳ 11 bits will represent set index.

11 bit set index → 0 0 0 1 | 1 0 1 0 0 0 0

↳ set no.

↳ HL4 no

↳ Hence, L1 miss will be at Tile (T1) ($(0001)_2 = 1$)

12	13	14	15
8	9	10	11
(4)	5	6	7
0	(1)	2	3

So, cache miss for M1 will travel: T4 → T5 → T1 (2 hops) [due to XY routing].

(d) Total latency =>

∴ 1 hop includes (3 cycle NoC router + 1 cycle link)

= 4 cycles in total

∴ injection and ejection total requires 2 cycles (1+1)

↳ There will be injection at source and ejection at destination.

and there is a hit/miss logic in L2 = 3 cycles.

No. of hops: 4 → 5 → 1 = 2 hops

Total latency = 6×4×(no. of hops) + 2 + 3

= 6×4×2 + 2 + 3

= 6×8 + 2 + 3 = 53 cycles // Ans

↳ Here 6 because no. of flits = Size of L1 / Bandwidth = 32/8 = 4 + 2 = 6.

↳ for head and tail