Emulating MOS 6502 for Vintage Computing

MAJOR PROJECT REPORT

SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF

BACHELOR OF TECHNOLOGY

(Computer Science and Engineering)

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Abstract

The MOS 6502 microprocessor, renowned for its pivotal role in the evolution of vintage computing systems, continues to captivate enthusiasts and researchers alike. As hardware becomes increasingly scarce, emulation emerges as a crucial avenue for preserving and studying these iconic systems. This project presents a comprehensive approach to emulating the MOS 6502, delving into the intricacies of its architecture and the challenges associated with faithful reproduction in a digital environment.

Our emulation strategy encompasses the accurate representation of the 6502's instruction set, memory management, and peripheral interactions. We explore the nuances of the original hardware, addressing subtle timing variations and undocumented behaviours that contribute to the unique character of the 6502-based systems. Leveraging advancements in modern computing, we discuss optimization techniques and parallelization to enhance emulation performance without compromising accuracy.

To facilitate broad accessibility and collaboration, we introduce an open-source emulation framework tailored for MOS 6502-based systems. The framework provides a modular and extensible architecture, allowing enthusiasts to contribute and adapt the emulation to various vintage computing platforms. Emphasis is placed on documentation and user-friendly interfaces to encourage wider adoption and participation in the preservation efforts.

We explore the potential applications of MOS 6502 emulation beyond preservation, such as educational tools, game development, and the exploration of historical software. By providing a versatile and accurate emulation environment, we aim to bridge the gap between contemporary computing and the rich legacy of vintage systems, fostering a renewed appreciation for the MOS 6502 and its impact on the evolution of computer technology.

Furthermore, we also explore collaborative efforts within the community, such as debugging tools and online repositories, that contribute to the collective knowledge and appreciation of MOS 6502-based systems. By intertwining technical precision with a broader cultural perspective, this project seeks to underscore the multifaceted importance of MOS 6502 emulation in preserving not just the hardware but the spirit of vintage computing for years to come.

ACKNOWLEDGEMENT

We are highly grateful to the Dr. Sehijpal Singh, Principal, Guru Nanak Dev Engineering College (GNDEC), Ludhiana, for providing this opportunity to carry out the major project work at Emulating MOS 6502 for Vintage Computing.

The constant guidance and encouragement received from Dr. Kiran Jyoti, HOD CSE Department, GNDEC Ludhiana has been of great help in carrying out the project work and is acknowledged with reverential thanks.

We would like to express a deep sense of gratitude and thanks profusely to Dr. Parminder Singh, without his wise counsel and able guidance, it would have been impossible to complete the project in this manner.

We express gratitude to other faculty members of computer science and engineering department of GNDEC for their intellectual support throughout the course of this work.

Finally, we are indebted to all whosoever have contributed to this report work.

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1. Introduction

1.1 Introduction to the Project

The project titled "Emulating MOS 6502 for Vintage Computing" is a unique and ambitious endeavour that combines the emulation of the MOS 6502 microprocessor with the functionality of a Nintendo Entertainment System (NES) emulator. The MOS 6502 microprocessor played a pivotal role in the microcomputer revolution of the late 1970s and early 1980s. Its presence in legendary systems like the Apple II and the Commodore 64 makes it a symbol of an era when personal computing was in its infancy.

This project aims to create a versatile software platform that not only accurately emulates the behaviour of the MOS 6502 processor for executing 8-bit assembly programs but also extends its capabilities to emulate NES games, providing an all-encompassing learning and nostalgic gaming experience.

The MOS 6502 microprocessor stands as a symbol of early computing history, embodying the fundamental aspects of microprocessor architecture. This project seeks to pay homage to this historical significance by meticulously emulating its operation. By doing so, the project invites users to explore the intricacies of instruction sets, memory organization, and program execution flow that define the essence of 8-bit computing technology. From addressing modes to memory management, the project aims to bring these fundamental concepts to life.

Furthermore, this project goes beyond a traditional microprocessor emulator by integrating the functionality of an NES emulator. The NES, known for its iconic games and impact on popular culture, provides an additional layer of engagement and interactivity. By combining the MOS 6502 emulation with NES game emulation, the project caters to both learners seeking a comprehensive understanding of microprocessors and enthusiasts eager to relive classic gaming experiences. Beyond the software development aspect, this project has the potential to foster a community of enthusiasts, educators, and learners who share a passion for vintage computing and gaming. Such communities often become hubs of knowledge sharing and collaborative exploration.

In the context of computer science education, this project holds immense educational value. It offers students an opportunity to explore low-level programming concepts, microprocessor architecture, and the mechanics of game emulation in a controlled environment. This project represents a holistic approach to merging technology, history, education, and entertainment, encapsulating the spirit of vintage computing for a new era of learners and enthusiasts.

1.2 Project Category

The project falls under the category of "Computer Architecture and Emulation." Specifically, it combines elements of hardware emulation and preservation within the broader domain of retro computing. This interdisciplinary project involves aspects of computer engineering, software development, and historical preservation. Emulating the MOS 6502 processor involves creating a virtualized environment that accurately reproduces the behaviour of the original hardware, enabling the execution of vintage software and the recreation of computing experiences from the past.

1.3 Problem Formulation

The endeavour to emulate MOS 6502 for vintage computing is prompted by the growing need to bridge the widening gap between the rich heritage of early computing systems and contemporary technology. As the original MOS 6502 hardware becomes increasingly scarce, the risk of losing access to the software and experiences unique to this era rises. By undertaking this emulation project, we aspire to create a versatile and open-source framework that not only preserves the functionality of the MOS 6502 but also facilitates a seamless transition for enthusiasts and researchers into the digital realm. This emulation solution aims to serve as a valuable resource for educational purposes, allowing new generations to gain insights into the foundational technologies that shaped the computing landscape. Moreover, the project aligns with the broader mission of preserving the cultural and historical significance embedded in vintage computing, ensuring that the MOS 6502 legacy remains vibrant and accessible for years to come.

Furthermore, the emulation of MOS 6502 for vintage computing not only addresses the immediate challenge of hardware scarcity but also opens avenues for collaborative exploration and innovation within the retro computing community. In doing so, we seek to ignite a renewed interest in the MOS 6502 and vintage computing, ensuring that the legacy of these foundational technologies remains relevant and accessible in our rapidly evolving digital landscape.

1.4 Identification of the Need

The imperative to develop an emulation framework for the MOS 6502 in vintage computing arises from several pressing needs within the computing community. Firstly, the original MOS 6502 hardware, which played a pivotal role in the advent of personal computing, is rapidly becoming scarce and difficult to obtain. This scarcity poses a significant obstacle for enthusiasts, historians, and educators who wish to explore and understand the early days of computing.

Secondly, there is a growing demand to preserve and make accessible the extensive catalogue of software and applications designed for the MOS 6502 architecture. Without a reliable emulation solution, there is a risk of losing access to valuable cultural and historical artifacts that are integral to the development of computing technology. Thirdly, the emulation project serves as a proactive measure to bridge the generational gap, offering a means for contemporary audiences to experience and appreciate the computing environments that laid the foundation for the modern digital landscape. In essence, the development of an MOS 6502 emulator addresses the urgent need to ensure the continued availability, study, and appreciation of vintage computing systems.

1.5 Existing System

The existing system for emulating MOS 6502 in the context of vintage computing is limited and fragmented. Enthusiasts and researchers relying on original MOS 6502 hardware face the challenge of increasing scarcity and potential hardware failures, hindering their ability to sustain and explore vintage computing environments. While some generic emulators exist, they often lack the specificity and accuracy required to faithfully reproduce the intricate behaviors of the MOS 6502 processor and its associated systems.

Additionally, the lack of a standardized and open-source emulation framework dedicated to MOS 6502 specifically hampers collaborative efforts, leaving a void in the preservation and exploration of this iconic computing era. The existing landscape underscores the necessity for a comprehensive and specialized emulation solution that caters specifically to the nuances of the MOS 6502 architecture, addressing the challenges posed by hardware scarcity and providing a robust platform for the study and enjoyment of vintage computing.

Moreover, the existing system lacks a unified and user-friendly environment for enthusiasts, educators, and developers to engage with the MOS 6502 emulation community. Documentation is often incomplete or dispersed, hindering the ease of use and adoption of current emulation tools.

By creating an open-source framework dedicated to MOS 6502 emulation, we aim to provide a centralized platform that encourages active participation, accelerates the development of new features, and fosters a collaborative environment where knowledge-sharing and innovation can flourish. This approach will not only enhance the accuracy and reliability of MOS 6502 emulation but also democratize access to vintage computing experiences, ensuring the continued relevance and vibrancy of this critical era in the history of computer technology.

1.6 Objectives of the Project

The following objectives have been achieved for accomplishment of this project:

- To develop a user-friendly emulator for the MOS 6502 processor, ensuring compatibility with a wide range of software and systems.
- To implement tools for real time debugging of assembly programs.
- To expand the emulator's capabilities to run Nintendo NES games, broadening its utility and appeal.

1.7 Proposed System

The proposed system for emulating MOS 6502 in vintage computing represents a comprehensive and specialized framework designed to address the limitations of the existing landscape. This proposed emulation system aims to offer a highly accurate and modular solution, specifically tailored to the intricacies of the MOS 6502 architecture.

Leveraging advancements in emulation technology, the system will prioritize authenticity, ensuring faithful reproduction of the original hardware's behavior, including subtle timing variations and undocumented features. To enhance accessibility and collaboration, the proposed system will be open source, inviting contributions from the community to refine and expand the emulation capabilities. The framework will include thorough documentation and user-friendly interfaces, facilitating a seamless experience for enthusiasts, researchers, and educators seeking to explore and understand vintage computing environments.

Moreover, the system will promote extensibility, enabling users to adapt the emulation for various vintage computing platforms and encouraging the development of additional features, tools, and peripherals. Through these innovations, the proposed system aims to establish a unified and vibrant ecosystem that not only preserves the legacy of the MOS 6502 but also propels the exploration and enjoyment of vintage computing into the future.

1.8 Unique Features of the System

The project will have the following features:

- **User-Friendly Interface:** The emulator prioritizes user-friendliness, offering an intuitive and accessible interface for enthusiasts, researchers, and educators. The graphical user interface (GUI) is designed to streamline the emulation process, making it easy for users to set up, configure, and run MOS 6502-based software with minimal technical barriers.
- **Compatibility Across Systems:** A key feature is the emphasis on ensuring broad compatibility. The emulator is engineered to work seamlessly across a diverse range of vintage computing systems that utilized the MOS 6502 processor. This compatibility ensures that users can explore and experience the unique characteristics of various platforms, fostering a more comprehensive understanding of the MOS 6502's impact on vintage computing.
- **Real-Time Debugging Tools:** To facilitate the exploration of assembly programs, the emulator incorporates real-time debugging tools. Users can step through code execution, set breakpoints, inspect registers and memory, and gain valuable insights into the inner workings of MOS 6502 programs. This feature caters to researchers and developers, providing a powerful toolset for in-depth analysis and debugging.
- **NES Game Compatibility:** A distinctive aspect of the emulator is its extended capability to run Nintendo NES games. This expansion broadens the utility and appeal of the emulator beyond traditional MOS 6502 software, attracting a wider audience interested in the iconic NES gaming experience. The inclusion of NES game compatibility adds a nostalgic and entertainment dimension to the project, making it a versatile platform for both educational and recreational purposes.

2. Requirement Analysis and System Specification

2.1 Feasibility Study

- **Technical Feasibility:**

  Emulating the MOS 6502 is technically feasible, involving a solid understanding of the 6502 architecture, choice between software or hardware emulation, consideration of performance requirements, accurate memory mapping, emulation of peripherals, development of testing and debugging tools, reliance on documentation, engagement with the retro computing community, attention to legal considerations, and allocation of adequate resources.

- **Economic Feasibility:**

  The cost-effectiveness depends on factors like existing hardware, software, and community support. Emulating on modern, widely-used platforms minimizes development costs. However, for commercial endeavors, the feasibility may be impacted by potential copyright issues, legal considerations, and the niche market for vintage computing. A thorough analysis of development costs, potential user base, and legal constraints is essential for determining economic feasibility.

- **Operational Feasibility:**

  Operational feasibility involves assessing whether the emulation project can be smoothly integrated and sustained within the intended environment. Key considerations include compatibility with existing systems, ease of use, potential impact on user workflows, and adaptability to evolving technologies.

- **Behavioural Feasibility:**

  Behavioural feasibility for emulating the MOS 6502 involves evaluating how well the emulation aligns with user needs and expectations. Key considerations include user acceptance, the ability of the emulation to replicate the behaviour of the original system accurately, and the overall user experience. Assessing whether the emulated system meets user requirements, provides a seamless transition for users accustomed to the original system, and aligns with their preferences is essential for determining behavioural feasibility.

2.2 Software Requirement Specification Document

- **Data Requirements**

  The system will require the following data inputs:

  - 6502 Architecture Documentation
  - Memory Mapping Information
  - Peripheral Specifications
  - Instruction Set reference
  - Cycle time information
  - Debugging Tools

- **Functional Requirements**

  The system will have the following functional requirements:

  - Emulate the complete MOS 6502 instruction set, including addressing modes and operation codes.
  - Replicate the memory structure of the original system, supporting RAM, ROM, and memory-mapped peripherals.
  - Emulate any peripherals (e.g., disk drives, graphics chips) associated with the vintage system to enable proper software interaction.
  - Implement cycle-accurate timing for precise emulation of the original 6502's timing characteristics.
  - Ensure accurate handling of flags in the processor status register (PSR), including zero, carry, and overflow flags.
  - Support all addressing modes employed by the MOS 6502, such as immediate, zero page, and absolute.
  - Design a user-friendly interface for easy interaction, software loading, and configuration.

- **Performance Requirements**

  The system must meet the following performance requirements:

  - Achieve real-time performance to ensure responsiveness and accurate timing in emulation.
  - Ensure broad compatibility with original software, maintaining a balance between accuracy and efficiency.

- Optimize resource utilization (CPU, memory) to run efficiently on a variety of modern hardware configurations.
- Ensure stable and reliable performance, avoiding crashes, freezes, or unexpected behaviour during emulation.

- **Dependability Requirements**

The system must meet the following dependability requirements:

- Ensure the emulator consistently performs as expected without frequent crashes or errors.
- Maintain high availability, allowing users to access and use the emulator reliably when needed.
- Provide a consistent emulation environment to ensure that software behaves predictably across different instances of the emulator.

- **Maintainability Requirements**

The system must meet the following maintainability requirements:

- Design the emulator with a modular architecture, allowing easy isolation and modification of components for maintenance purposes.
- Implement a version control system to track changes, manage updates, and facilitate rollbacks if necessary.
- Include clear and well-documented code comments to enhance code readability and understanding, aiding future developers in maintenance tasks.
- Design the emulator to be easily adaptable to new hardware platforms or operating systems, promoting long-term maintainability.
- Maintain comprehensive and up-to-date documentation for both users and developers, aiding in understanding, troubleshooting, and updates.

- **Security Requirements**

The system must meet the following security requirements:

- Implement access controls to restrict unauthorized access to sensitive features or configuration settings within the emulator.
- Ensure secure communication between the emulator and external systems, especially if it involves data transfer or network interactions.
- Utilize encryption mechanisms for sensitive data, both during storage and transmission, to protect against unauthorized access.

- Regularly monitor for and address potential security vulnerabilities, applying patches or updates promptly.

- **Look and Feel Requirements**

The system must meet the following look and feel requirements:

- Emulate the look and feel of the original vintage system's user interface, capturing the nostalgic experience for users.
- Provide user controls that mimic the feel of the original system, ensuring an intuitive and familiar interaction for users.
- Replicate the graphical elements and display characteristics of the vintage system to maintain an authentic visual experience.

2.3 SDLC model

i). **Planning and Requirement Analysis:** In the planning and requirement analysis phase of emulating the MOS 6502 for the SDLC model, it is essential to define the project scope by specifying the targeted features and limitations of the emulation. This comprehensive planning and requirement analysis will provide a solid foundation for the subsequent stages of the SDLC, ensuring a systematic and well-informed approach to the emulation project.

ii). **Defining Requirements:** In emulating the MOS 6502 for the Software Development Life Cycle (SDLC) model, defining requirements involves a meticulous analysis of the architecture, specifying emulation goals, and considering compatibility factors. The requirements encompass a comprehensive understanding of the MOS 6502's instruction set, memory organization, and addressing modes.

iii). **Designing the Product Architecture:** The product architecture design should be centered around creating an efficient and accurate representation of the vintage computing environment. The architecture needs to encompass key components such as the instruction decoder, memory management, and emulation of peripheral devices. A modular and extensible design is crucial to accommodate potential future enhancements and optimizations. The architecture should also consider factors like performance, compatibility, and ease of debugging. Implementing an accurate instruction set interpreter or dynamic recompilation approach, depending on the project's goals, is fundamental.

iv). **Building or Developing the Product:** During the development phase of emulating MOS 6502 within the chosen SDLC model, the focus is on translating the planned architecture and requirements into a functional emulator. The development process, whether following a Waterfall, Iterative, Agile, or Prototyping model, involves iterative cycles of implementation, testing, and refinement until a robust and feature-complete MOS 6502 emulator is achieved.

v). **Testing the Product:** Testing the emulation of the MOS 6502 in the Software Development Life Cycle (SDLC) model involves a comprehensive approach to ensure the accuracy, reliability, and compatibility of the emulator. Unit testing focuses on verifying individual components such as instruction decoding and memory management, ensuring they function as intended.

Integration testing examines the interaction between these components to identify and address any issues that may arise during emulation. Functional testing validates the emulator against the expected behaviour of the MOS 6502 architecture, emphasizing the correct execution of instructions and accurate memory handling. Compatibility testing is crucial to ensure the emulator works with a variety of vintage software and peripherals.

vi). **Deployment in the Market and Maintenance:** For the deployment phase of emulating MOS 6502 within the SDLC model, carefully package the emulator and associated components for distribution. Create user documentation that explains installation procedures, system requirements, and basic usage. Utilize version control systems to manage releases and ensure that the deployment process is streamlined and reproducible. After deployment, shift focus to maintenance, addressing bug fixes, enhancing features based on user feedback, and ensuring compatibility with evolving systems.

3. System Design

3.1 Design Approach

The design approach for Emulating MOS 6502 for Vintage Computing, with each hardware component emulated as a C++ class, follows a modular and object-oriented paradigm to achieve accuracy, flexibility, and ease of maintenance. The primary components, such as the bus, mapper, CPU, PPU, and cartridge, are encapsulated within their respective classes, each responsible for handling specific functionalities.

3.2 Detail Design

The project involves emulation of MOS 6502 CPU and the various parts of a Nintendo Entertainment System. These components can be seen in the Figure 1

I. Modules and their functionalities:

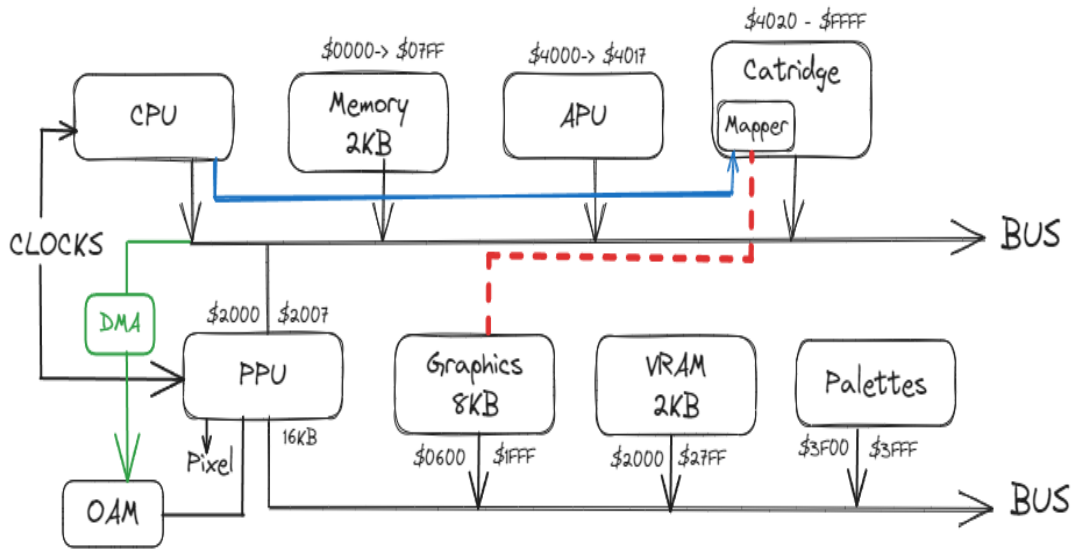


Figure 1 Various Modules of An NES System

i). CPU:

6502 CPU Emulator: Emulates the MOS Technology 6502 CPU, the processor used in the NES.

ii). Memory Management:

Memory Mapper: Manages the NES's memory mapping, handling the mapping of ROM and RAM to appropriate addresses.

iii). Picture Processing Unit (PPU) Emulation:

Picture Processing Unit (PPU) Emulator: Emulates the NES's GPU responsible for rendering graphics, sprites, and backgrounds.

iv). Audio Processing Unit (APU) Emulation:

Audio Emulator: Emulates the NES's APU responsible for generating sound and music.

v). Input Handling:

Controller Input Emulator: Simulates the NES controllers, mapping user input to the corresponding actions in the emulated game.

vi). Cartridge Emulation:

Mapper: Emulates the cartridge's mapper chip, which controls the bank switching and memory mapping of the game cartridge.

vii). Timing and Synchronization:

Clock and Timing: Manages the timing and synchronization of the emulator to ensure that instructions, graphics, and audio are processed at the correct rate.

viii). User Interface (UI):

Graphical User Interface (GUI): Provides a user interface for loading ROMs, configuring settings, and interacting with the emulator.

ix). Debugger and Logging:

Debugger: Allows developers to inspect the internal state of the emulator, set breakpoints, and analyse the execution of code.

Logging Module: Logs information about the emulator's operation for debugging purposes.

x). Save States:

Save State Manager: Enables the creation and loading of save states, allowing users to save their progress in a game and resume from a specific point.

xi). Configuration and Settings:

Configuration Manager: Manages settings and configurations, allowing users to customize the emulator's behaviour.

xii). Frontend and Backend:

- **Frontend:** The user-facing part of the emulator, including the GUI and user interactions.
- **Backend:** The core emulation logic and modules that handle the actual processing of instructions, graphics, and audio.

These modules collectively work together to recreate the functionality of the NES on a modern computing system, allowing users to play classic NES games on their computers or other devices. Developing an NES emulator is a complex task that requires a deep understanding of the NES hardware and programming.

II. CPU Emulation Design of MOS 6502 CPU:

The 6502 microprocessor is a relatively simple 8-bit CPU with only a few internal registers capable of addressing at most 64Kb of memory via its 16-bit address bus. The processor is little endian and expects addresses to be stored in memory least significant byte first.

The first 256-byte page of memory ($0000-$00FF) is referred to as 'Zero Page' and is the focus of several special addressing modes that result in shorter (and quicker) instructions or allow indirect access to the memory. The second page of memory ($0100-$01FF) is reserved for the system stack and which cannot be relocated.

The only other reserved locations in the memory map are the very last 6 bytes of memory $FFFA to $FFFF which must be programmed with the addresses of the non-maskable interrupt handler ($FFFA/B), the power on reset location ($FFFC/D) and the BRK/interrupt request handler ($FFFE/F) respectively.

The 6502 does not have any special support of hardware devices so they must be mapped to regions of memory to exchange data with the hardware latches.

III. Registers:

The 6502 has only a small number of registers compared to another processor of the same era. This makes it especially challenging to program as algorithms must make efficient use of both registers and memory.

i). Program Counter

The program counter is a 16 bit register which points to the next instruction to be executed. The value of program counter is modified automatically as instructions are executed. The value of the program counter can be modified by executing a jump, a relative branch or a subroutine call to another memory address or by returning from a subroutine or interrupt.

ii). Stack Pointer

The processor supports a 256 byte stack located between $0100 and $01FF. The stack pointer is an 8 bit register and holds the low 8 bits of the next free location on the stack. The location of the stack is fixed and cannot be moved. Pushing bytes to the stack causes the stack pointer to be decremented. Conversely pulling bytes causes it to be incremented.

The CPU does not detect if the stack is overflowed by excessive pushing or pulling operations and will most likely result in the program crashing.

iii). Accumulator

The 8-bit accumulator is used all arithmetic and logical operations (with the exception of increments and decrements). The contents of the accumulator can be stored and retrieved either from memory or the stack.

Most complex operations will need to use the accumulator for arithmetic and efficient optimisation of its use is a key feature of time critical routines.

iv). Index Register X

The 8-bit index register is most commonly used to hold counters or offsets for accessing memory. The value of the X register can be loaded and saved in memory, compared with values held in memory or incremented and decremented.

The X register has one special function. It can be used to get a copy of the stack pointer or change its value.

v). Index Register Y

The Y register is similar to the X register in that it is available for holding counter or offsets memory access and supports the same set of memory load, save and compare operations as wells as increments and decrements. It has no special functions.

vi). Processor Status

As instructions are executed a set of processor flags are set or clear to record the results of the operation. This flags and some additional control flags are held in a special status register. Each flag has a single bit within the register. Instructions exist to test the values of the various bits, to set or clear some of them and to push or pull the entire set to or from the stack.

- **Carry Flag:** The carry flag is set if the last operation caused an overflow from bit 7 of the result or an underflow from bit 0. This condition is set during arithmetic, comparison and during logical shifts. It can be explicitly set using the 'Set Carry Flag' (SEC) instruction and cleared with 'Clear Carry Flag' (CLC).
- **Zero Flag:** The zero flag is set if the result of the last operation as was zero.
- **Interrupt Disable:** The interrupt disable flag is set if the program has executed a 'Set Interrupt Disable' (SEI) instruction. While this flag is set the processor will not respond to interrupts from devices until it is cleared by a 'Clear Interrupt Disable' (CLI) instruction.
- **Decimal Mode:** While the decimal mode flag is set the processor will obey the rules of Binary Coded Decimal (BCD) arithmetic during addition and subtraction. The flag can be explicitly set using 'Set Decimal Flag' (SED) and cleared with 'Clear Decimal Flag' (CLD).
- **Break Command:** The break command bit is set when a BRK instruction has been executed and an interrupt has been generated to process it.
- **Overflow Flag:** The overflow flag is set during arithmetic operations if the result has yielded an invalid 2's complement result (e.g. adding to positive numbers and ending up with a negative result: 64 + 64 => -128). It is determined by looking at the carry between bits 6 and 7 and between bit 7 and the carry flag.
- **Negative Flag:** The negative flag is set if the result of the last operation had bit 7 set to a one.

IV. The Instruction Set:

The 6502 has a relatively basic set of instructions, many having similar functions (e.g. memory access, arithmetic, etc.). The following sections list the complete set of 56 instructions in functional groups.

i). Load/Store Operations

These instructions transfer a single byte between memory and one of the registers. Load operations set the negative (N) and zero (Z) flags depending on the value of transferred. Store operations do not affect the flag settings. Table 1 shows all the various load instructions.

Table 1 Various Load/Store Instructions

Instruction	Description	Flags Affected
LDA	Load Accumulator	N, Z
LDX	Load X Register	N, Z
LDY	Load Y Register	N, Z
STA	Store Accumulator	
STX	Store X Register	
STY	Store Y Register	

ii). Register Transfers

The contents of the X and Y registers can be moved to or from the accumulator, setting the negative (N) and zero (Z) flags as appropriate. Table 2 shows all the various register transfer instructions.

Table 2 Register Transfer Instructions

Instruction	Description	Flags Affected
TAX	Transfer accumulator to X	N, Z
TAY	Transfer accumulator to Y	N, Z
TXA	Transfer X to accumulator	N, Z
TYA	Transfer Y to accumulator	N, Z

iii). Stack Operations

The 6502 microprocessor supports a 256-byte stack fixed between memory locations $0100 and $01FF. A special 8-bit register, S, is used to keep track of the next free byte of stack space. Pushing a byte on to the stack causes the value to be stored at the current free location (e.g. $0100,S) and then the stack pointer is post decremented. Pull operations reverse this procedure.

The stack register can only be accessed by transferring its value to or from the X register. Its value is automatically modified by push/pull instructions, subroutine calls and returns, interrupts and returns from interrupts. Table 3 shows all the various stack instructions.

Table 3 Stack Instructions

Instruction	Description	Flags Affected
TSX	Transfer stack pointer to X	N, Z
TXS	Transfer X to stack pointer	
PHA	Push accumulator on stack	
PHP	Push processor status on stack	
PLA	Pull accumulator from stack	N, Z
PLP	Pull processor status from stack	All

iv). Logical

The following instructions perform logical operations on the contents of the accumulator and another value held in memory. The BIT instruction performs a logical AND to test the presence of bits in the memory value to set the flags but does not keep the result. Table 4 shows all the various logical instructions.

Table 4 Logical Instructions

Instruction	Description	Flags Affected
AND	Logical AND	N,Z
EOR	Exclusive OR	N,Z
ORA	Logical Inclusive OR	N,Z
BIT	Bit Test	N,V,Z

v). Arithmetic

The arithmetic operations perform addition and subtraction on the contents of the accumulator. The compare operations allow the comparison of the accumulator and X or Y with memory values. Table 5 shows various arithmetic instructions.

Table 5 Arithmetic Instructions

Instruction	Description	Flags Affected
ADC	Add with Carry	N,V,Z,C
SBC	Subtract with Carry	N,V,Z,C
CMP	Compare accumulator	N,Z,C
CPX	Compare X register	N,Z,C
CPY	Compare Y register	N,Z,C

vi). Increments & Decrements

Increment or decrement a memory location or one of the X or Y registers by one setting the negative (N) and zero (Z) flags as appropriate. Table 6 shows all the various increment and decrement instructions.

Table 6 Increment and Decrement Instructions

Instruction	Description	Flags Affected
INC	Increment a memory location	N,Z
INX	Increment the X register	N,Z
INY	Increment the Y register	N,Z
DEC	Decrement a memory location	N,Z
DEX	Decrement the X register	N,Z
DEY	Decrement the Y register	N,Z

vii). Shifts

Shift instructions cause the bits within either a memory location or the accumulator to be shifted by one bit position. The rotate instructions use the contents if the carry flag (C) to fill the vacant position generated by the shift and to catch the overflowing bit. The arithmetic and logical shifts shift in an appropriate 0 or 1 bit as appropriate but catch the overflow bit in the carry flag (C). Table 7 shows the various shift instructions.

Table 7 Shift Instructions

Instruction	Description	Flags Affected
ASL	Arithmetic Shift Left	N,Z,C
LSR	Logical Shift Right	N,Z,C
ROL	Rotate Left	N,Z,C
ROR	Rotate Right	N,Z,C

viii). Jumps & Calls

The following instructions modify the program counter causing a break to normal sequential execution. The JSR instruction pushes the old PC onto the stack before changing it to the new location allowing a subsequent RTS to return execution to the instruction after the call. Table 8 shows various jump and call instructions.

Table 8 Jump and Call Instructions

Instruction	Description
JMP	Jump to another location
JSR	Jump to a subroutine
RTS	Return from subroutine

ix). Branches

Branch instructions break the normal sequential flow of execution by changing the program counter if a specified condition is met. All the conditions are based on examining a single bit within the processor status. Table 9 shows various branching instructions.

Table 9 Branch Instructions

Instruction	Description
BCC	Branch if carry flag clear
BCS	Branch if carry flag set
BEQ	Branch if zero flag set
BMI	Branch if negative flag set
BNE	Branch if zero flag clear
BPL	Branch if negative flag clear
BVC	Branch if overflow flag clear
BVS	Branch if overflow flag set

Branch instructions use relative address to identify the target instruction if they are executed. As relative addresses are stored using a signed 8-bit byte the target instruction must be within 126 bytes before the branch or 128 bytes after the branch.

x). Status Flag Changes

The following instructions change the values of specific status flags.

Table 10 Status Instructions

Instruction	Description	Flags Affected
CLC	Clear carry flag	C
CLD	Clear decimal mode flag	D
CLI	Clear interrupt disable flag	I
CLV	Clear overflow flag	V
SEC	Set carry flag	C
SED	Set decimal mode flag	D
SEI	Set interrupt disable flag	I

xi). System Functions

The remaining instructions perform useful but rarely used functions.

Table 11 System Related Instructions

Instruction	Description	Flags Affected
BRK	Force an interrupt	B
NOP	No Operation	
RTI	Return from Interrupt	All

V. Addressing Modes:

The 6502 processor provides several ways in which memory locations can be addressed. Some instructions support several different modes while others may only support one. In addition, the two index registers cannot always be used interchangeably. This lack of orthogonality in the instruction set is one of the features that makes the 6502 trickier to program well.

i). Implicit

For many 6502 instructions the source and destination of the information to be manipulated is implied directly by the function of the instruction itself and no further operand needs to be specified. Operations like 'Clear Carry Flag' (CLC) and 'Return from Subroutine' (RTS) are implicit.

ii). Accumulator

Some instructions have an option to operate directly upon the accumulator. The programmer specifies this by using a special operand value, 'A'. For example:

```
LSR A           ;Logical shift right one bit
ROR A           ;Rotate right one bit
```

Figure 2 Example of An Instrction that applies operation on the accumulator

iii). Immediate

Immediate addressing allows the programmer to directly specify an 8 bit constant within the instruction. It is indicated by a '#' symbol followed by a numeric expression. For example:

```
LDA #10         ;Load 10 ($0A) into the accumulator
LDX #LO LABEL   ;Load the LSB of a 16 bit address into X
LDY #HI LABEL   ;Load the MSB of a 16 bit address into Y
```

Figure 3 Example of An Instruction that uses Immediate Addressing

iv). Zero Page

An instruction using zero page addressing mode has only an 8-bit address operand. This limits it to addressing only the first 256 bytes of memory (e.g., $0000 to $00FF) where the most significant byte of the address is always zero. In zero-page mode only the least significant byte of the address is held in the instruction making it shorter by one byte (important for space saving) and one less memory fetch during execution (important for speed).

An assembler will automatically select zero page addressing mode if the operand evaluates to a zero-page address and the instruction supports the mode (not all do).

```
LDA $00         ;Load accumulator from $00
ASL ANSWER      ;Shift labelled location ANSWER left
```

Figure 4 Example of An Instruction Using Zero Page Addressing

v). Zero Page, X

The address to be accessed by an instruction using indexed zero-page addressing is calculated by taking the 8-bit zero-page address from the instruction and adding the current value of the X register to it. For example, if the X register contains $0F and the instruction LDA $80, X is executed then the accumulator will be loaded from $008F (e.g., $80 + $0F => $8F).

NB: The address calculation wraps around if the sum of the base address and the register exceed $FF. If we repeat the last example but with $FF in the X register, then the accumulator will be loaded from $007F (e.g., $80 + $FF => $7F) and not $017F.

```
STY $10,X        ;Save the Y register at location on zero page
AND TEMP,X       ;Logical AND accumulator with a zero page value
```

Figure 5 Example of An Instruction Using Zero Page X Addressing

vi). Zero Page, Y

The address to be accessed by an instruction using indexed zero-page addressing is calculated by taking the 8-bit zero-page address from the instruction and adding the current value of the Y register to it. This mode can only be used with the LDX and STX instructions.

```
LDX $10,Y        ;Load the X register from a location on zero page
STX TEMP,Y       ;Store the X register in a location on zero page
```

Figure 6 Example of An Instruction Using Zero Page Y Addressing

vii). Relative

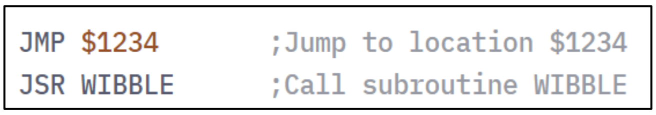
Relative addressing mode is used by branch instructions (e.g. BEQ, BNE, etc.) which contain a signed 8 bit relative offset (e.g. -128 to +127) which is added to program counter if the condition is true. As the program counter itself is incremented during instruction execution by two the effective address range for the target instruction must be with -126 to +129 bytes of the branch.

```
BEQ LABEL        ;Branch if zero flag set to LABEL
BNE *+4          ;Skip over the following 2 byte instruction
```

Figure 7 Example of An Instruction Using Relative Addressing

viii). Absolute

Instructions using absolute addressing contain a full 16-bit address to identify the target location.

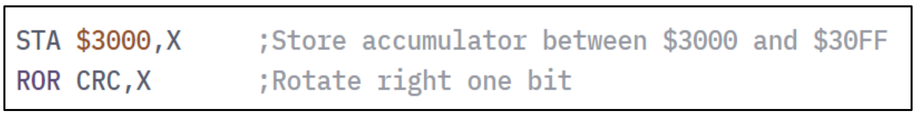


```
JMP $1234         ;Jump to location $1234
JSR WIBBLE        ;Call subroutine WIBBLE
```

Figure 8 Example of An Instruction Using Absolute Addressing

ix). Absolute, X

The address to be accessed by an instruction using X register indexed absolute addressing is computed by taking the 16-bit address from the instruction and added the contents of the X register. For example, if X contains $92 then an STA $2000, X instruction will store the accumulator at $2092 (e.g., $2000 + $92).

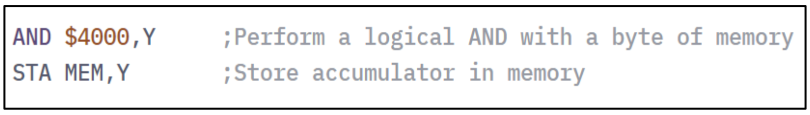


```
STA $3000,X       ;Store accumulator between $3000 and $30FF
ROR CRC,X         ;Rotate right one bit
```

Figure 9 Example of An Instruction Using Absolute X Addressing

x). Absolute, Y

The Y register indexed absolute addressing mode is the same as the previous mode only with the contents of the Y register added to the 16-bit address from the instruction.



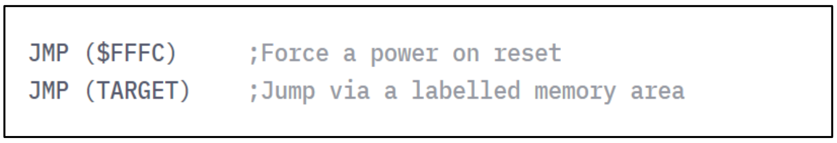
```
AND $4000,Y       ;Perform a logical AND with a byte of memory
STA MEM,Y         ;Store accumulator in memory
```

Figure 10 Example of An Instruction Using Absolute Y Addressing

xi). Indirect

JMP is the only 6502 instructions to support indirection. The instruction contains a 16-bit address which identifies the location of the least significant byte of another 16-bit memory address which is the real target of the instruction.

For example, if location $0120 contains $FC and location $0121 contains $BA then the instruction JMP ($0120) will cause the next instruction execution to occur at $BAFC (e.g., the contents of $0120 and $0121).

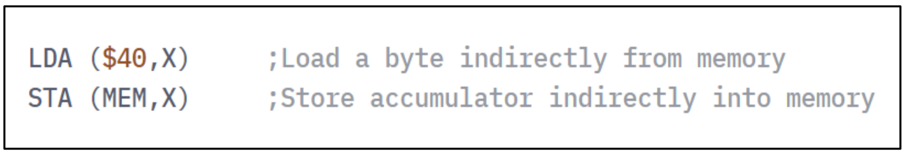


```
JMP ($FFFC)     ;Force a power on reset
JMP (TARGET)    ;Jump via a labelled memory area
```

Figure 11 Example of An Instruction Using Indirect Addressing

xii). Indexed Indirect

Indexed indirect addressing is normally used in conjunction with a table of address held on zero page. The address of the table is taken from the instruction and the X register added to it (with zero page wrap around) to give the location of the least significant byte of the target address.

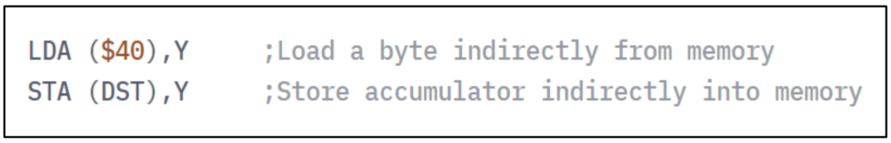


```
LDA ($40,X)     ;Load a byte indirectly from memory
STA (MEM,X)     ;Store accumulator indirectly into memory
```

Figure 12 Example of An Instruction Using Indexed Indirect Addressing

xiii). Indirect Indexed

Indirect indexed addressing is the most common indirection mode used on the 6502. In instruction contains the zero-page location of the least significant byte of 16-bit address. The Y register is dynamically added to this value to generate the actual target address for operation.



```
LDA ($40),Y     ;Load a byte indirectly from memory
STA (DST),Y     ;Store accumulator indirectly into memory
```

Figure 13 Example of An Instruction Using Indirect Indexed Addressing

III. BUS Design of MOS 6502 CPU:

In the context of the Nintendo Entertainment System (NES) emulator, the Bus component plays a crucial role as the central communication and data transfer hub within the simulated hardware architecture. The primary responsibility of the Bus is to facilitate interaction between the major components of the NES, including the CPU (Central Processing Unit), PPU (Picture Processing Unit), and the Cartridge containing the game data.

The Bus manages memory access by providing a unified interface for reading and writing data across different address ranges. It oversees the interaction between the CPU and system RAM, ensuring that reads and writes to specific memory locations are appropriately handled. Additionally, it handles communication with the PPU, allowing the CPU to manipulate and retrieve data from the graphics subsystem.

One of the critical tasks performed by the Bus is the initiation and management of DMA (Direct Memory Access) transfers. When a DMA transfer is triggered, the Bus coordinates the movement of data from the CPU's memory space to the PPU's OAM (Object Attribute Memory), facilitating efficient sprite rendering for graphics display.

Moreover, the Bus acts as a connector for the Cartridge, which contains the game program and additional data. It enables the CPU to read instructions and data from the Cartridge and allows the Cartridge to influence or intercept specific bus transactions. This flexibility is crucial for accommodating various cartridge types and potential future enhancements or custom hardware additions to the NES emulation.

The clocking mechanism implemented in the Bus ensures the synchronization of the CPU and PPU clocks, providing a unified timing source for the entire system. This coordination is essential for maintaining the correct timing relationships between different hardware components, enabling accurate emulation of the NES.

In summary, the Bus in the NES emulator serves as the backbone for communication, memory management, and timing synchronization among the key components of the system, contributing to the overall accuracy and functionality of the NES emulation.

The following figure represents how the Bus is used to connect all the over components of the NES emulator with each other.

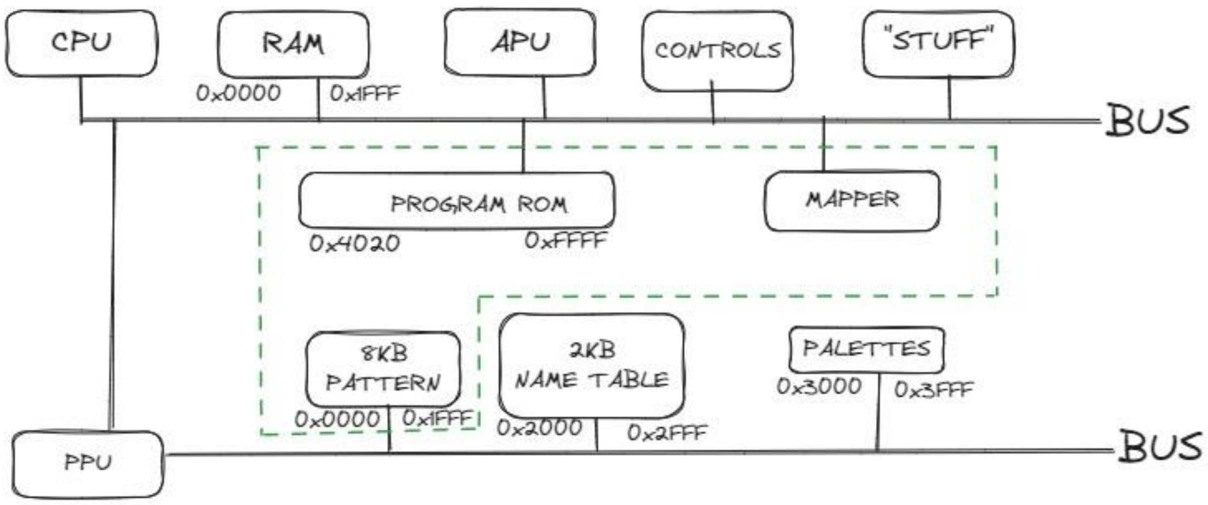


Figure 14 Connection of Bus with other components of NES Emulator

i). Responsibilities:

- **Communication Hub:** The Bus class acts as a communication hub between the CPU, PPU, Cartridge, and other components.
- **Memory Management:** Handles memory reads and writes, including system RAM, PPU registers, cartridge data, and controllers.
- **Clock Management:** Manages the system clock and ensures synchronization between the CPU and PPU.

ii). Memory Mapping:

- **Address Ranges:** Different address ranges are assigned to various components, such as system RAM, PPU registers, and controllers.
- **Mirroring:** Memory mirroring is handled to simplify memory access.

iii). DMA Transfer:

- **Initiation:** DMA transfers are initiated by writing to the 0x4014 address.
- **Timing:** DMA timing is crucial, involving dummy cycles and accurate synchronization with the PPU and CPU clocks.

iv). Clocking Mechanism:

- **CPU Clocking:** The CPU is clocked every three cycles, and it handles regular instructions or DMA transfers as needed.
- **PPU Clocking:** The PPU is clocked on every call to the clock method.

v). System Interface:

- **Cartridge Connection:** The insertCartridge method connects the cartridge to the bus, allowing the cartridge to provide data and control certain operations.

vi). Reset Mechanism:

- **Resetting Components:** The reset method resets various components, including the cartridge, CPU, and PPU, to their initial states.

```
#pragma once
#include <cstdint>
#include <array>
#include "olc6502.h"
#include "olc2C02.h"
#include "Cartridge.h"


class Bus
{
public:
        Bus();
        ~Bus();


public: // Devices on Main Bus
```

```
	// The 6502 derived processor
	olc6502 cpu;
	// The 2C02 Picture Processing Unit
	olc2C02 ppu;
	// The Cartridge or "GamePak"
	std::shared_ptr<Cartridge> cart;
	// 2KB of RAM
	uint8_t cpuRam[2048];
	// Controllers
	uint8_t controller[2];

public: // Main Bus Read & Write
	void    cpuWrite(uint16_t addr, uint8_t data);
	uint8_t cpuRead(uint16_t addr, bool bReadOnly = false);

private:
	// A count of how many clocks have passed


	uint32_t nSystemClockCounter = 0;
	// Internal cache of controller state


	uint8_t controller_state[2];

private:
	// A simple form of Direct Memory Access is used to swiftly
```

```
        // transfer data from CPU bus memory into the OAM memory. It would
        // take too long to sensibly do this manually using a CPU loop, so
        // the program prepares a page of memory with the sprite info required
        // for the next frame and initiates a DMA transfer. This suspends the
        // CPU momentarily while the PPU gets sent data at PPU clock speeds.
        // Note here, that dma_page and dma_addr form a 16-bit address in
        // the CPU bus address space
        uint8_t dma_page = 0x00;
        uint8_t dma_addr = 0x00;
        uint8_t dma_data = 0x00;

        // DMA transfers need to be timed accurately. In principle it takes
        // 512 cycles to read and write the 256 bytes of the OAM memory, a
        // read followed by a write. However, the CPU needs to be on an "even"
        // clock cycle, so a dummy cycle of idleness may be required
        bool dma_dummy = true;

        // Finally a flag to indicate that a DMA transfer is happening
        bool dma_transfer = false;

public: // System Interface
        // Connects a cartridge object to the internal buses
        void insertCartridge(const std::shared_ptr<Cartridge>& cartridge);
        // Resets the system
        void reset();
        // Clocks the system - a single whole systme tick
        void clock();
};
```

IV. Cartridge Design of MOS 6502 CPU:

In the context of the Nintendo Entertainment System (NES) emulation, the cartridge plays a pivotal role as the primary storage medium for the game program and associated data. The responsibilities of the cartridge in an NES emulator are multifaceted and include memory management, facilitating communication between the CPU and other system components, and ensuring accurate representation of the game's content.

First and foremost, the cartridge serves as a container for two main types of read-only memory (ROM): Program ROM (PRG) and Character ROM (CHR). The PRG ROM holds the executable code and game logic, while the CHR ROM stores graphics and sprite data used by the Picture Processing Unit (PPU). The cartridge is responsible for loading these ROM sections into the appropriate memory regions when requested by the CPU or PPU.

Memory management is a critical aspect of the cartridge's role. It must handle memory mapping, where specific addresses accessed by the CPU or PPU correspond to different regions within the PRG and CHR ROM. Cartridges often employ bank switching mechanisms to extend the effective memory space and enable larger games to fit into the NES's limited addressable memory.

Additionally, the cartridge facilitates communication between the CPU, PPU, and other components via read and write operations. It responds to requests from the CPU for code execution and data retrieval, ensuring that the correct information is provided based on the accessed memory address. Similarly, the PPU communicates with the cartridge to fetch graphics data required for rendering sprites and backgrounds.

The cartridge also manages additional features specific to certain games or hardware configurations. Some cartridges may include battery-backed RAM for saving game progress, sophisticated mappers to support advanced bank switching, or additional hardware to enhance the NES system's capabilities.

Furthermore, the cartridge plays a crucial role in system initialization and resets. It ensures that the game begins in a consistent state and that any necessary setup procedures are executed. This includes resetting internal registers, initializing memory banks, and preparing the system for a new gameplay session.

In summary, the cartridge in an NES emulator is responsible for providing the necessary ROM data, managing memory access through sophisticated mapping mechanisms, facilitating communication between the CPU and PPU, and ensuring that the emulator accurately emulates the behaviour of the original NES hardware. Its multifunctional nature makes it a central component in recreating the gaming experience of NES titles within a software emulation environment.

The following diagram shows the interaction between the bus and how the mapper is used for communication between the components.

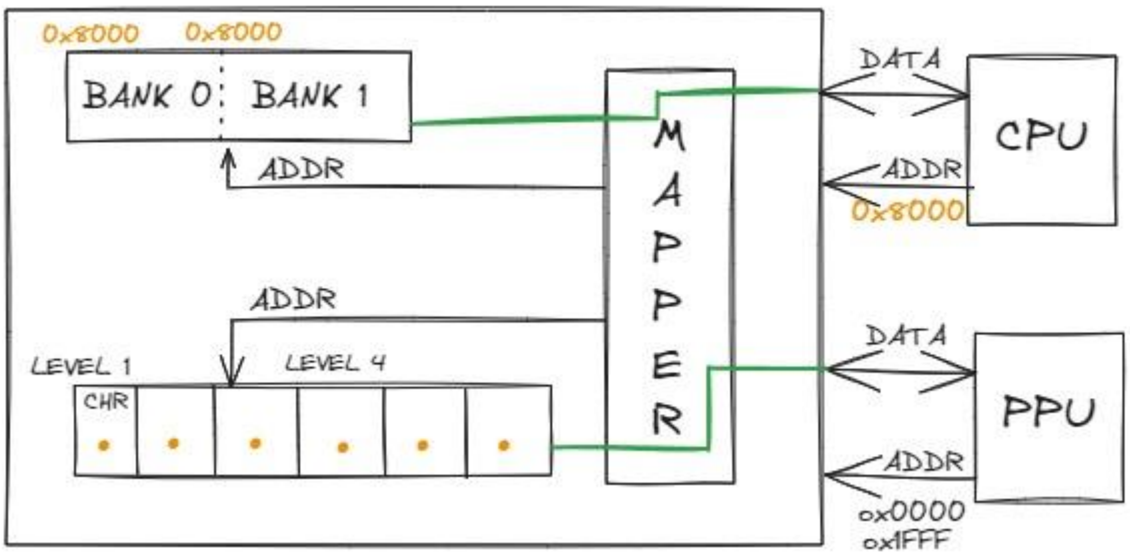


Figure 15 Interaction between Bus and Mapper for communication between components

i). **ROM Loading:** The Cartridge class is responsible for loading ROM data from a specified file path, including both PRG ROM (program data) and CHR ROM (graphics data).

ii). **CPU and PPU Interfaces:** The class provides interfaces for the CPU and PPU components to read and write data to the cartridge memory. These methods handle memory mapping based on the cartridge's specifications, including bank switching and mirroring.

iii). **Memory Mapping Functions:** The cartridge implements memory mapping functions to determine the correct memory locations for reads and writes. This involves translating CPU and PPU addresses into specific regions of the ROM, considering features such as bank switching and mirroring.

iv). **Reset and Initialization:** The reset method resets the cartridge state if needed. This may involve resetting bank switching, mirroring, or other internal cartridge parameters.

```
#pragma once

#include <cstdint>

#include <string>

#include <fstream>

#include <vector>

#include "Mapper_000.h"

//#include "Mapper_002.h"

//#include "Mapper_003.h"

//#include "Mapper_066.h"


class Cartridge

{

public:

	Cartridge(const std::string& sFileName);

	~Cartridge();


public:

	bool ImageValid();

	enum MIRROR

	{

		HORIZONTAL,

		VERTICAL,

		ONESCREEN_LO,

		ONESCREEN_HI,

	} mirror = HORIZONTAL;
private:
	bool bImageValid = false;

	uint8_t nMapperID = 0;
	uint8_t nPRGBanks = 0;
	uint8_t nCHRBanks = 0;

	std::vector<uint8_t> vPRGMemory;
	std::vector<uint8_t> vCHRMemory;

	std::shared_ptr<Mapper> pMapper;

public:
	// Communication with Main Bus
	bool cpuRead(uint16_t addr, uint8_t &data);
	bool cpuWrite(uint16_t addr, uint8_t data);

	// Communication with PPU Bus
	bool ppuRead(uint16_t addr, uint8_t &data);
	bool ppuWrite(uint16_t addr, uint8_t data);
	// Permits system rest of mapper to know state
	void reset();
};
```

V. PPU Design of MOS 6502 CPU:

The Picture Processing Unit (PPU) in the Nintendo Entertainment System (NES) serves as the graphics processing component responsible for rendering visuals on the screen. Its primary responsibility lies in the generation of 2D graphics by combining background layers, sprites, and palettes to create the overall game display. The PPU operates independently of the Central Processing Unit (CPU) and has its own memory, addressing scheme, and clocking mechanism.

The PPU is tasked with fetching graphical data from the connected cartridge, interpreting this data, and converting it into pixel information for display on the screen. It manages two main types of memory: Pattern Table, storing tile patterns for backgrounds and sprites, and Name Table, organizing the arrangement of tiles to compose the visible scene. The PPU reads data from these tables, applies palettes, and renders the composite image, which is then sent to the display.

One of the critical functions of the PPU is sprite rendering, where it retrieves sprite data from memory based on the game's requirements. The PPU also handles sprite evaluation, determining which sprites should be displayed on each scanline, considering factors like sprite priority and transparency. Additionally, the PPU supports scrolling and mirroring effects, allowing for dynamic and visually appealing backgrounds.

The PPU operates in sync with the CPU, and their coordination is vital for smooth emulation. The CPU communicates with the PPU by reading and writing to specific memory-mapped registers, instructing the PPU on how to render graphics and manage the display. The PPU, in turn, generates non-maskable interrupts (NMIs) to alert the CPU when specific rendering stages are complete, ensuring precise synchronization.

Moreover, the PPU contributes to the overall visual aesthetic through its support for a limited but effective color palette. The NES PPU is capable of displaying up to 64 unique colors simultaneously, using a combination of background, sprite, and universal palettes.

In essence, the PPU's responsibilities encompass fetching and interpreting graphical data, managing the arrangement of tiles and sprites, rendering the final image for display, handling scrolling effects, supporting sprite evaluation, and ensuring synchronization with the CPU to create a cohesive and visually appealing gaming experience on the NES platform. Its role is fundamental to the emulation of NES games, as it replicates the original hardware's ability to produce graphics with the distinctive retro charm associated with the NES era.

The Picture Processing Unit (PPU) in the Nintendo Entertainment System (NES) is a specialized chip responsible for generating graphics and rendering images on the screen. It consists of several key components that work together to produce the visual output for NES games. Here are the various components of the PPU:

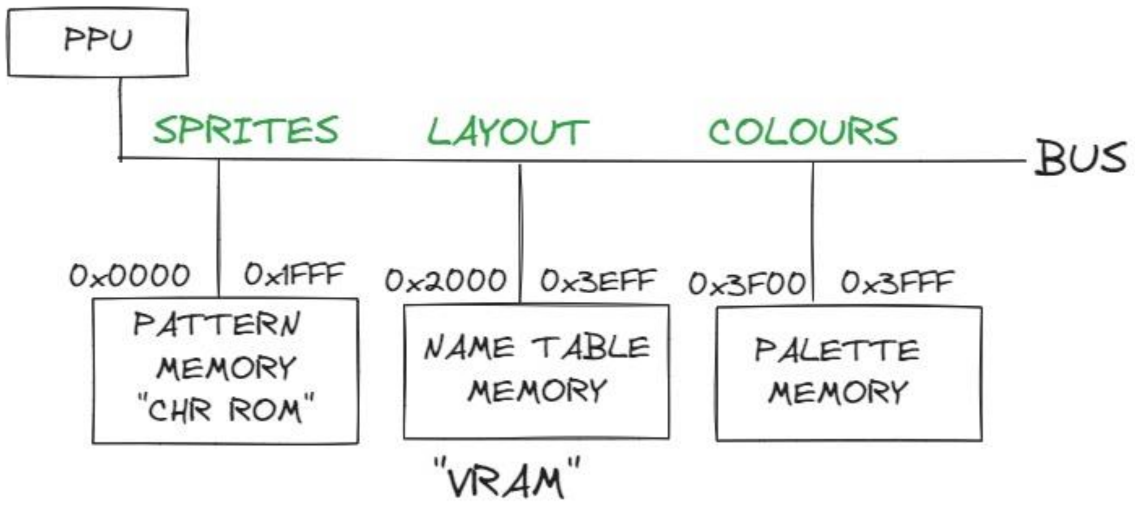


Figure 16 Components of PPU

i). Pattern Memory (CHR ROM)

Pattern memory in the context of the NES PPU (Picture Processing Unit) is a critical component responsible for storing the graphical patterns that make up sprites and backgrounds in NES games. Understanding pattern memory is key to grasping how the PPU renders images on the screen.

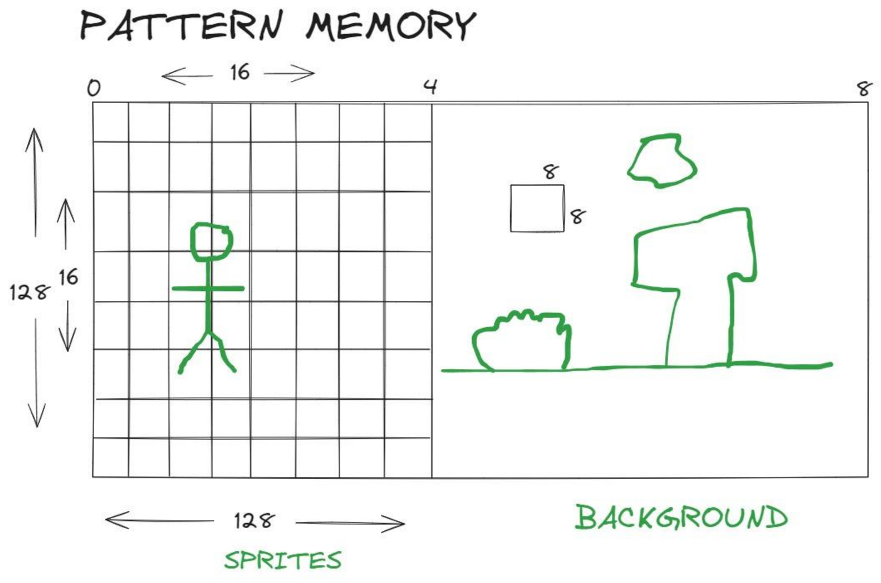


Figure 17 Representation of Pattern Memory

Here's a more detailed explanation of pattern memory:

a). Size and Organization:

- Pattern memory is organized as a collection of 8x8 pixel tiles. Each tile is a small, reusable graphic element that can be combined to create larger images.
- In the NES, each tile consists of 64 pixels arranged in an 8x8 grid. Each pixel is represented by a binary value (0 or 1), determining whether the pixel is transparent (0) or opaque (1).

b). Role in Sprite and Background Rendering:

- For sprites: Pattern memory holds the unique graphical patterns of individual sprites. Each sprite in a game is represented by a specific tile pattern in pattern memory. The PPU fetches these patterns during sprite rendering to display the sprites on the s creen.
- For backgrounds: Pattern memory contributes to the rendering of background tiles. The PPU fetches background tile patterns from pattern memory based on the information stored in the name table and attribute table.

c). Location and Storage:

- Pattern memory is typically located in the Character ROM (CHR ROM) section of the game cartridge. CHR ROM contains the graphics data used by the PPU.
- The PPU fetches the appropriate tile patterns from CHR ROM during rendering. The specific location of each tile in pattern memory is determined by the tile index provided by the name table.

d). Tile Index and Addressing:

- The PPU uses a tile index to address a specific tile in pattern memory. The tile index is obtained from the name table, which specifies the arrangement of tiles for background rendering.
- The tile index is combined with the base address of pattern memory to form the complete memory address from which the PPU fetches the graphical pattern.

e). Color Information:

- While pattern memory stores the binary representation of pixel values, color information is determined by the palette assigned to a particular tile. Palettes are managed separately in palette memory.
- The PPU combines the binary pixel values with color information from the palette to determine the final color of each pixel during rendering.

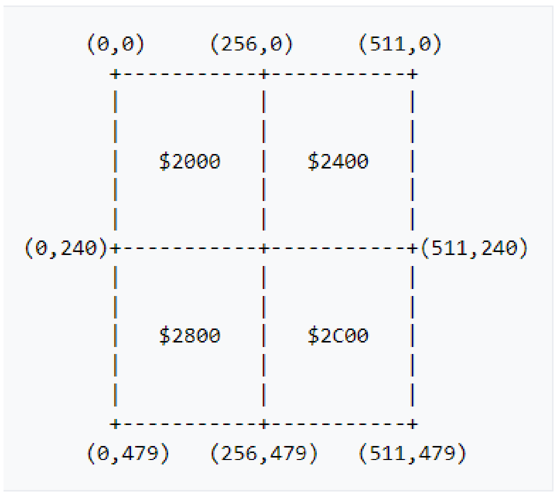
f). CHR Banks and Bank Switching:

- Some NES cartridges may have multiple banks of CHR ROM, allowing for a larger pool of tile patterns. Bank switching mechanisms enable the PPU to access different banks during gameplay, expanding the available graphics resources.

In summary, pattern memory is a fundamental part of the NES PPU's functionality, storing the graphical patterns of sprites and background tiles. It is organized in a way that allows for efficient rendering of 8x8 pixel tiles, and its content is fetched by the PPU during the rendering process to create the visual elements seen on the screen in NES games.

ii). Name Table:

The Name table is a critical component of the Picture Processing Unit (PPU) in the Nintendo Entertainment System (NES), responsible for defining the layout and arrangement of background tiles on the screen. Understanding the Name table is essential for comprehending how the PPU renders background graphics in NES games.



```
     (0,0)     (256,0)     (511,0)
       +-----------+-----------+
       |           |           |
       |           |           |
       |   $2000   |   $2400   |
       |           |           |
       |           |           |
(0,240)+-----------+-----------+(511,240)
       |           |           |
       |           |           |
       |   $2800   |   $2C00   |
       |           |           |
       |           |           |
       +-----------+-----------+
     (0,479)   (256,479)   (511,479)
```

Figure 18 Representation of Name Table

Here's a more detailed explanation:

a). Definition and Purpose:

- The Name table is a region of memory that specifies the arrangement of background tiles to create the visual scene on the screen. It essentially acts as a map that associates specific tiles with screen positions.
- There are typically two-Name Tables (NT0 and NT1) in the NES PPU, each corresponding to a different background layer. These layers can be used for various effects such as scrolling or split-screen gameplay.

b). Tile Indexing:

- The Nametable divides the screen into a grid of 32x30 cells. Each cell represents an 8x8 pixel tile. The intersection of a row and column in the grid specifies a unique screen position.
- The content of each cell is a tile index, which refers to a specific entry in Pattern Memory. This index determines which graphical pattern to fetch for that screen position.

c). Memory Organization:

- The Nametable is stored in the PPU's memory, and the CPU can access it through specific memory-mapped addresses. Reading from or writing to these addresses allows the CPU to configure the arrangement of tiles on the screen.
- The memory size of the Nametable is 2 KB (32 columns x 30 rows x 1 byte per cell), but the NES PPU only displays a portion of it on the screen at a time.

d). Attributes:

- Alongside tile indices, the Nametable contains attributes that define visual characteristics of groups of tiles. The Attribute Table is associated with the Nametable and provides information about the palettes applied to specific regions of the screen.
- Attribute information is often stored in a compressed format, grouping multiple tiles into a single attribute byte. Each attribute byte corresponds to a 2x2 cell region of the Nametable.

e). Scrolling:

- The Nametable is crucial for handling scrolling effects. The PPU maintains scroll registers that adjust the starting position for rendering, effectively scrolling the screen.
- Scrolling allows for dynamic and smooth transitions between different parts of the Nametable, creating the illusion of movement or exploration in NES games.

f). Updates During V-Blank:

- Typically, updates to the Nametable and other PPU registers occur during the Vertical Blank (V-Blank) period when the PPU is not actively rendering. This ensures stability and consistency during the rendering process.

g). Mirroring Modes:

- The NES PPU supports different Nametable mirroring modes, influencing how the Nametable data is used to render the entire screen. Common mirroring modes include horizontal mirroring, vertical mirroring, and one-screen mirroring.

In summary, the Nametable serves as a blueprint for the NES PPU, dictating the arrangement of background tiles on the screen. It is a crucial part of the PPU's functionality, defining the visual structure of the game world and allowing for dynamic effects like scrolling. The CPU interacts with the Nametable through memory-mapped addresses to configure the layout of the screen during gameplay.

iii). Attribute Table:

The Attribute Table is a component closely associated with the Nametable in the Nintendo Entertainment System's (NES) Picture Processing Unit (PPU). It provides additional information about the visual attributes of groups of tiles, allowing for more versatile and varied rendering of backgrounds.

The below figure describes the representation of Attribute Table.

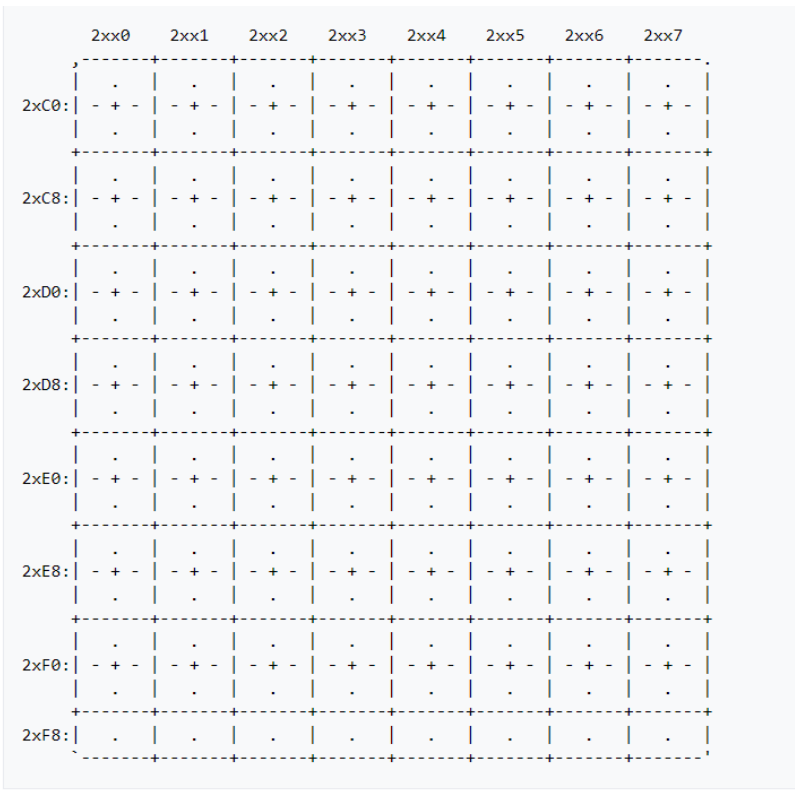


Figure 19 Representation of Attribute Table

Here's a more detailed explanation of the Attribute Table:

a). Role and Purpose:

- The Attribute Table accompanies the Nametable and provides information about the palettes applied to specific regions of the screen. It allows the PPU to apply different color palettes to groups of tiles, enhancing the visual variety in the background.

b). Organization and Structure:

- The Attribute Table is organized into a grid that corresponds to the layout of the Nametable. Each entry in the Attribute Table corresponds to a 2x2 cell region in the Nametable.
- Each entry in the Attribute Table covers a 32x32 pixel area on the screen (4 Nametable cells), as it represents the combined attributes for a 2x2 grouping of tiles

c). Color Information:

- The primary information stored in the Attribute Table is color-related. Each entry in the Attribute Table specifies which of the four available palettes (background palettes) should be applied to the corresponding 2x2 cell region in the Nametable.

- Palettes are composed of three colors (color bits 0-2) and a background color (color bit 3), allowing for a total of four distinct colors for each 2x2 cell region.

d). Compression and Storage:

- Attribute information is often stored in a compressed format to optimize memory usage. Typically, each byte in the Attribute Table covers four 2x2 cell regions (2 bits per region).
- The 2 bits in each region determine which of the four palettes should be applied to that region. The PPU interprets these bits to select the appropriate palette during rendering.

e). Memory Organization:

- Similar to the Nametable, the Attribute Table is stored in the PPU's memory, and the CPU can access it through specific memory-mapped addresses. Reading from or writing to these addresses allows the CPU to configure the attributes of different screen regions.
- The memory size of the Attribute Table is 64 bytes (32 columns x 2 rows), covering the entire 256x240 pixel screen divided into 2x2 cell regions.

f). Updates During V-Blank:

- Updates to the Attribute Table usually occur during the Vertical Blank (V-Blank) period, ensuring that changes to the palettes and attributes are synchronized with the rendering process and do not cause visual artifacts.

g). Mirroring Modes:

- Similar to the Nametable, the NES PPU supports different mirroring modes for the Attribute Table. Common modes include horizontal mirroring, vertical mirroring, and one-screen mirroring.

In summary, the Attribute Table is a crucial component that complements the Nametable in the NES PPU, providing information about color attributes for groups of tiles. It enhances the visual richness of backgrounds by allowing the PPU to apply different palettes to specific screen regions, contributing to the distinctive look of NES games. The CPU interacts with the Attribute Table through memory-mapped addresses to configure the color attributes during gameplay.

iv). Palette Memory:

Palette Memory in the context of the Nintendo Entertainment System (NES) Picture Processing Unit (PPU) is a component responsible for storing color information used in rendering graphics.

The NES PPU supports a limited but effective color palette, and Palette Memory defines the specific colors available for use in both background and sprite rendering.

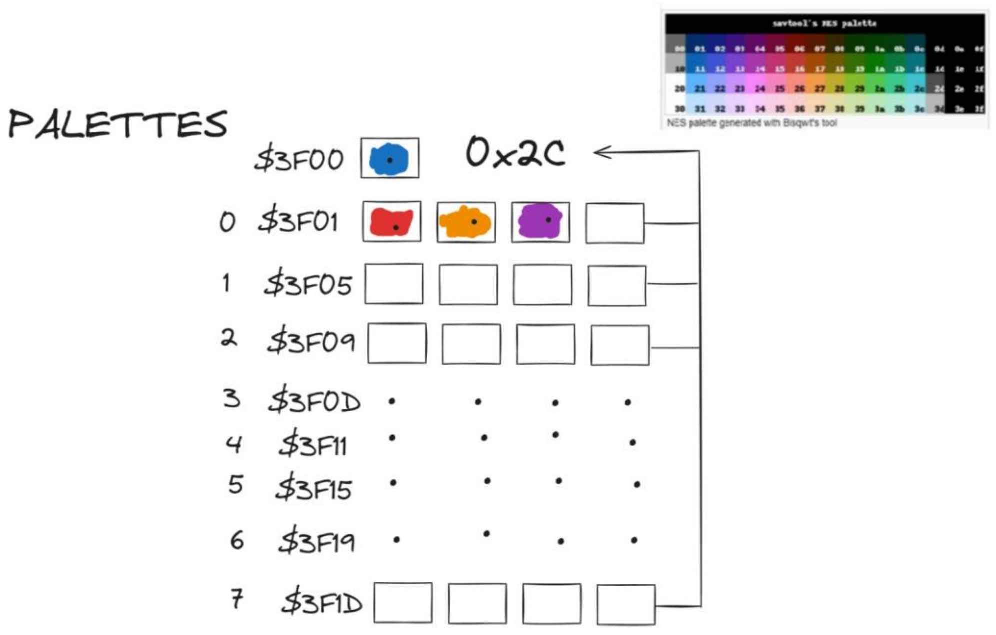


Figure 20 Representation of Color Palette and Palette Memory

Here's a more detailed explanation:

a). Color Palette:

- The NES PPU's color palette consists of 64 distinct colors. These colors are divided into four sets of background palettes, each containing three colors, and four sets of sprite palettes, each also containing three colors.
- Each color in the palette is represented by a combination of red, green, and blue (RGB) values. The NES PPU, however, had a simplified color model with fewer possible shades compared to modern displays.

b). Organization:

- Palette Memory is organized as an array of 32 bytes, with each byte representing one of the 32 possible colors in the NES color palette. The color values are often stored in a specific format where each component (red, green, and blue) is allocated a certain number of bits.
- The arrangement of colors in Palette Memory is such that the first 16 entries are mirrored to create a total of 32 unique colors.

c). Background and Sprite Palettes:

- Palette Memory is divided into two sections: background palettes and sprite palettes. Each section contains four sets of three colors.
- Background palettes are used for rendering the background graphics, and sprite palettes are used for rendering sprites. These palettes provide flexibility in coloring various elements of the game.

d). Color Format:

- The NES PPU uses a simple color format where each component (red, green, and blue) is assigned 2 bits. This results in 6 possible intensity levels for each color component, providing a total of 64 unique colors in the palette.
- The actual color displayed on the screen is determined by a display unit, which may interpret these bits differently depending on the video output.

e). Updates and Configuration:

- The CPU can write to specific memory-mapped addresses to update the values in Palette Memory. During gameplay, the CPU may dynamically change the palette to achieve different visual effects, such as transitioning between scenes or representing different game states.
- Updates to Palette Memory are often performed during the Vertical Blank (V-Blank) period to ensure synchronization with the rendering process.

f). Color Emphasis:

- Palette Memory includes bits for color emphasis, allowing the manipulation of the intensity of certain color components. This feature can be used to create visual effects, such as emphasizing red or blue colors in the display.

g). Mirroring:

- Similar to other PPU components, Palette Memory may exhibit mirroring, where certain memory addresses are mirrored to others. This mirroring ensures efficient memory usage and simplifies the addressing scheme.

In summary, Palette Memory is a vital part of the NES PPU, defining the available colors for background and sprite rendering. It allows for customization of the visual appearance of games and plays a significant role in shaping the distinctive look of NES graphics. The CPU interacts with Palette Memory through memory-mapped addresses to configure and update color information during gameplay.

v). Object Attribute Memory (OAM):

Object Attribute Memory (OAM) is a crucial component of the Nintendo Entertainment System (NES) Picture Processing Unit (PPU). It plays a fundamental role in rendering sprites on the screen.

Here's a more detailed explanation of Object Attribute Memory:

a). Definition and Purpose:

- OAM is a region of memory in the PPU that stores information about sprites. Each entry in OAM represents one sprite and contains attributes such as the sprite's position, tile index, and other properties.
- The NES supports a maximum of 64 sprites on a single scanline, and OAM is used to manage and organize the data for these sprites.

b). Structure of OAM Entries:

- Each entry in OAM is 4 bytes long and contains the following information:
- Y-coordinate: Specifies the vertical position of the sprite on the screen.
- Tile index: Identifies the tile pattern in Pattern Memory that represents the sprite's appearance.
- Attribute byte: Contains information about the sprite's properties, including color emphasis, horizontal and vertical flipping, and sprite priority.
- X-coordinate: Specifies the horizontal position of the sprite on the screen.

c). Memory Organization:

- OAM is organized as a linear array of 256 bytes. The first 64 bytes (0-63) are dedicated to sprite data for the first scanline, the next 64 bytes (64-127) for the second scanline, and so on.
- The organization allows the PPU to efficiently fetch sprite data during the rendering process.

d). Sprite Size and Scaling:

- The NES supports two sprite sizes: 8x8 pixels and 8x16 pixels. The sprite size is determined by a control bit in the PPU's control registers.
- In 8x16 mode, each sprite entry in OAM represents a pair of vertically stacked 8x8 tiles, providing larger and more versatile sprites.

e). Attributes and Properties:

- The attribute byte in each OAM entry contains several bits that control the appearance and behavior of the sprite. These include:
- Priority: Determines whether the sprite appears in front of or behind the background.
- Flipping: Allows the sprite to be horizontally and/or vertically flipped.
- Color Palette: Specifies which color palette from Palette Memory the sprite should use.

f). Fetching and Rendering:

- During the rendering process, the PPU fetches sprite data from OAM based on the sprite information stored for the current scanline. The fetched data includes the tile pattern, color attributes, and position.
- The PPU combines the sprite data with background data to produce the final pixel data that is sent to the display.

g). Sprite Evaluation:

- Before rendering a scanline, the PPU performs sprite evaluation, during which it determines which sprites are visible on the upcoming scanline. The information from OAM is used to make this determination.
- Sprites are evaluated based on their X-coordinates, and a maximum of eight sprites with the highest X-coordinates are selected for rendering on a single scanline.

h). Updates During V-Blank:

- Similar to other PPU components, updates to OAM usually occur during the Vertical Blank (V-Blank) period, ensuring that changes to sprite data do not interfere with the rendering process.

In summary, Object Attribute Memory (OAM) is a dedicated memory region in the NES PPU that stores information about sprites, including their positions, tile patterns, and attributes. It is a critical component for rendering sprites on the screen and contributes to the overall visual presentation of NES games. The CPU interacts with OAM by writing sprite data to it during specific intervals.

vi). Internal Registers:

Internal registers in the context of the Nintendo Entertainment System (NES) Picture Processing Unit (PPU) are special memory locations within the PPU that are used for controlling its operation and maintaining its state. These registers are accessible through memory-mapped addresses, allowing the Central Processing Unit (CPU) to communicate with the PPU.

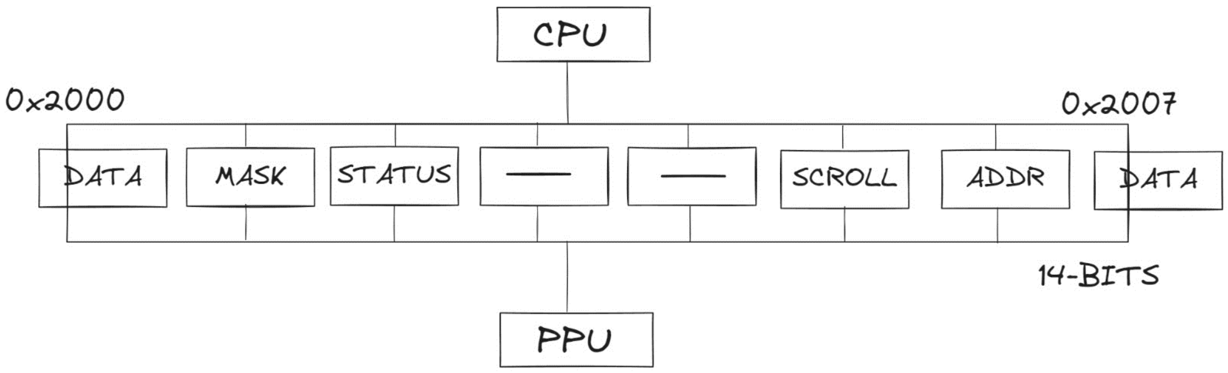


Figure 21 Internal Registers in NES

Here's a more detailed explanation of internal registers in the NES PPU:

a). Control Registers:

- The NES PPU has several control registers that determine various aspects of its behavior. These include:
  - o PPUCTRL (PPU Control Register): Controls the operation mode of the PPU, such as the addressing mode for reading/writing VRAM, the size of the sprites, and the selection of the background pattern table.
  - o PPUMASK (PPU Mask Register): Specifies which parts of the screen are visible (background, sprites, left column), as well as color emphasis and grayscale settings.

b). Status Register:

- PPUSTATUS (PPU Status Register): Provides status information about the PPU. Reading from this register clears certain internal flags, such as the sprite overflow flag and sprite zero hit flag. This register is used by the CPU to synchronize with the PPU's vertical blanking period.

c). Scroll Registers:

- PPUSCROLL (PPU Scroll Register): Contains the scroll position for the next frame. This register is used to adjust the starting position for rendering, allowing for smooth scrolling effects in both the horizontal and vertical directions.

d). Address Registers:

- PPUADDR (PPU Address Register): Determines the memory address for reading/writing data in VRAM. The CPU sets this register to specify the target address for upcoming read or write operations.
- PPUDATA (PPU Data Register): Holds the data being written to or read from VRAM. Reading from or writing to this register increments the VRAM address.

e). Sprite DMA Registers:

- OAMADDR (Object Attribute Memory Address Register): Specifies the address in Object Attribute Memory (OAM) that will be accessed for reading/writing sprite data.
- OAMDATA (Object Attribute Memory Data Register): Holds the data being written to or read from OAM. This register is used to update sprite information during gameplay.

f). DMA Registers:

- DMA (Direct Memory Access): The 0x4014 register is used to initiate a DMA transfer from CPU memory to OAM. It specifies the starting address in CPU memory from which the sprite data will be copied to OAM during the next frame.

g). Overscan Register:

- PPUOAMADDR (PPU OAM Address Register): Specifies the address in OAM for sprite evaluation during the next frame. It is typically used during the Vertical Blank (V-Blank) period to set up OAM for the next frame.

h). Sprite Zero Hit Register:

- PPUADDR (PPU Address Register): The sprite zero hit flag in the PPUSTATUS register is used to detect if a sprite at position 0 on the screen has been hit during rendering. This information is useful for triggering certain game events.

These registers collectively provide the CPU with the ability to configure and control the NES PPU's behavior. Proper synchronization between the CPU and PPU is essential to ensure smooth rendering of graphics and efficient communication between the two units. The PPU's internal registers are crucial for managing rendering, scrolling, sprite evaluation, and other aspects of the graphical display in NES games.

vii). Scroll Registers:

The Scroll Registers in the Nintendo Entertainment System (NES) Picture Processing Unit (PPU) are crucial components that enable control over the positioning and scrolling of the background during rendering. These registers allow for both fine and coarse adjustments in both the horizontal and vertical directions, providing the flexibility needed to create smooth scrolling effects in NES games.

Here's a more detailed explanation:

a). Fine and Coarse Scrolling:

- The NES PPU employs a tile-based graphics system, where the background is composed of 8x8 pixel tiles. Fine scrolling refers to the ability to scroll at the pixel level, providing smoother and more precise scrolling effects. Coarse scrolling, on the other hand, operates at the level of entire tiles, allowing for larger-scale movements.

b). PPUSCROLL (PPU Scroll Register):

- The PPUSCROLL register is an 8-bit register that allows for fine horizontal and vertical scrolling adjustments.
- When writing to PPUSCROLL, two consecutive writes are performed. The first write sets the fine horizontal scroll value (bits 3-0), and the second write sets the fine vertical scroll value (bits 7-0).

c). PPUADDR (PPU Address Register):

- While primarily used for specifying the VRAM address, the PPUADDR register also influences coarse scrolling.
- Bits 11-8 of the VRAM address set the coarse horizontal scroll value, and bits 11-12 and 10-5 set the coarse vertical scroll value.

d). Updating Scroll Registers:

- To achieve smooth scrolling effects, developers typically update the scroll registers during the Vertical Blank (V-Blank) period. This ensures that changes in scrolling do not interfere with the rendering process.
- By adjusting the scroll registers between frames, developers can create animations, parallax scrolling, and other dynamic visual effects.

e). Constraints and Tile Grid:

- Scrolling in the NES is constrained by the 8x8 pixel grid of tiles. The coarse horizontal scroll determines which column of tiles to start rendering, while the coarse vertical scroll determines which row of tiles to start rendering.
- Fine scroll values provide additional pixel-level adjustments within the selected tile.

f). Mirroring Modes:

- The mirroring mode used in the NES game affects how scrolling behaves. In horizontal mirroring, vertical scrolling affects a single row of tiles, while in vertical mirroring, horizontal scrolling affects a single column of tiles.
- Developers need to consider the mirroring mode when implementing scrolling effects to achieve the desired visual outcome.

g). Smooth Scrolling Techniques:

- Developers use a combination of fine and coarse scrolling techniques to achieve various scrolling effects. Fine scrolling is often used for smooth and subtle movements, while coarse scrolling is employed for larger-scale transitions.

h). Dynamic Effects:

- The ability to dynamically adjust the scroll registers allows developers to create dynamic effects such as screen transitions, level changes, and cinematic sequences.
- In summary, the Scroll Registers in the NES PPU provide developers with the tools to control and manipulate the positioning of the background during rendering. These registers are crucial for achieving smooth scrolling effects and dynamic visual presentations in NES games. Fine and coarse scrolling techniques, along with careful updates to the scroll registers, contribute to the overall visual experience and gameplay.

viii). Rendering Pipeline:

The rendering pipeline in the context of a video game or graphics system refers to the sequence of stages through which graphical elements are processed to produce the final image displayed on the screen. In the case of the Nintendo Entertainment System (NES) or similar retro gaming systems, the rendering pipeline involves several steps that collectively generate the visuals seen by the player.

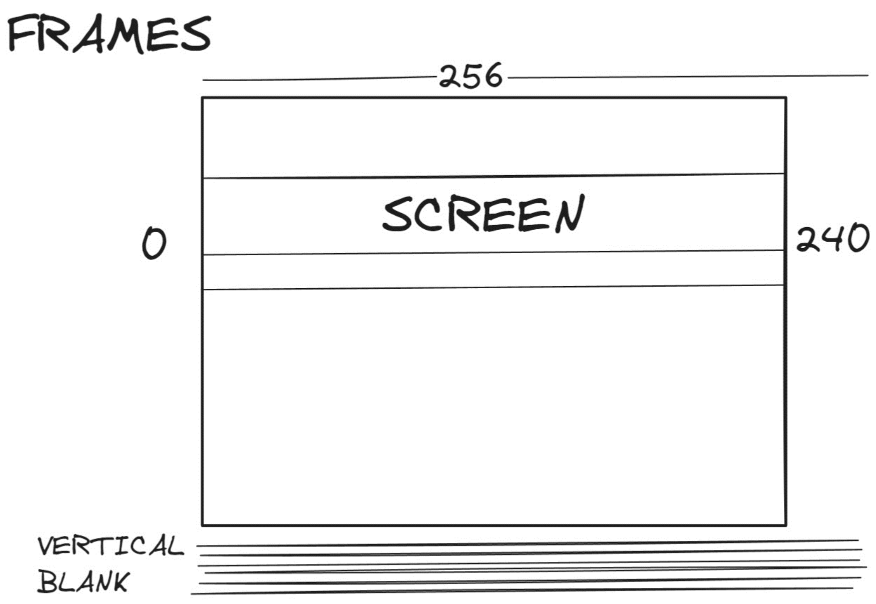


Figure 22 Rendering Pipeline generating the Visual Screen

Here's a more detailed explanation of the rendering pipeline in an NES emulator:

a). Fetch Background Tiles:

- The rendering process begins with the fetching of background tiles. The NES uses a tiled graphics system, where the background is composed of 8x8 pixel tiles. The Picture Processing Unit (PPU) fetches the necessary tiles from VRAM (Video RAM).

b). Tile and Attribute Fetch:

- For each tile, the PPU fetches the tile pattern from Pattern Memory and the corresponding attributes from the Attribute Table. The attributes determine the palette and other properties of the tile.

c). Background Rendering:

- The fetched tiles are then rendered onto the screen according to the current scroll position and mirroring mode. The PPU combines the background tiles based on the current viewport, applying horizontal and vertical scrolling.

d). Sprite Evaluation:

- The PPU evaluates sprites for the current scanline. It checks the Object Attribute Memory (OAM) to determine which sprites are visible and should be rendered on the upcoming scanline.

e). Sprite Fetch and Rendering:

- For each visible sprite, the PPU fetches the sprite pattern from Pattern Memory and renders it onto the screen. The order of rendering is determined by the sprite's position in OAM, with sprites closer to the foreground rendered later.

f). Sprite Zero Hit Detection:

- The PPU performs sprite zero hit detection during the rendering process. This involves checking if a pixel from sprite zero overlaps with a background pixel on the current scanline. This information is crucial for triggering certain game events and is often used to synchronize with the CPU.

g). Rendering Composition:

- The rendered background and sprites are composited to generate the final pixel data for the current scanline. This involves combining the pixel colors from background tiles and sprites based on their priorities and the presence of transparency.

h). Pixel Output:

- The composited pixel data for the current scanline is sent to the display for output. This process occurs iteratively for each scanline, resulting in a complete frame.

i). Vertical Blank (V-Blank) Period:

- After rendering a frame, the PPU enters the Vertical Blank period. During this time, the CPU and game logic have an opportunity to update the game state and prepare for the next frame without interfering with the rendering process.

j). Repeat for Each Frame:

- The rendering pipeline repeats for each frame, creating the illusion of motion and animation by updating the scroll registers, sprite positions, and other parameters between frames.

Understanding the rendering pipeline is essential for designing an emulator that accurately reproduces the visuals of NES games. It involves coordinating the various components of the PPU, such as Pattern Memory, Nametables, Attribute Tables, and OAM, to faithfully replicate the graphics seen on the original hardware.

These components work together to enable the PPU to render graphics in a manner consistent with the capabilities of the original NES hardware. The PPU's ability to efficiently handle tile-based graphics, manage sprites, and apply palettes contributes to the distinctive visual style of NES games.

VI. APU Design of MOS 6502 CPU:

Implementing the Audio Processing Unit (APU) in an NES emulator is a complex task, as it involves accurately emulating the sound generation and processing capabilities of the original hardware. The NES APU is responsible for producing the audio heard in games, including music, sound effects, and other auditory elements. Here's a high-level overview of the design and implementation considerations for the APU in an NES emulator:

i). Channels:

- The NES APU consists of several channels, each responsible for generating specific types of sounds. These channels include pulse wave channels, triangle wave channel, noise channel, and a delta modulation channel for handling sample playback.

ii). Registers:

- The APU has a set of memory-mapped registers that the CPU can write to control the APU's behavior. These registers configure various aspects of sound generation, including frequency, volume, and duty cycle.

iii). Frame Sequencer:

- The APU has a frame sequencer that controls the timing of envelope and sweep units. It generates timing signals for different APU components, ensuring that sound elements change over time according to the specified parameters.

iv). Pulse Wave Channels:

- Pulse wave channels generate square waveforms. They have adjustable duty cycles and can be used to create a variety of sound effects. The CPU writes to registers to control frequency, duty cycle, and volume.

v). Triangle Wave Channel:

- The triangle wave channel produces a triangular waveform. It is often used for basslines or certain melodic elements. The CPU sets the frequency and linear counter parameters.

vi). Noise Channel:

- The noise channel generates a pseudo-random waveform. It's commonly used for percussive sounds and special effects. The CPU configures the frequency, volume, and various modes of the noise generator.

vii). Delta Modulation Channel (DMC):

- The DMC channel allows for the playback of sampled sounds. The CPU provides a sample address, and the APU fetches and plays back the samples. This channel has a variable playback rate and volume.

viii). Envelope Unit:

- Each sound channel has an envelope unit that controls the volume envelope over time. The envelope can be used to create fades, crescendos, or decrescendos in the sound.

ix). Accuracy:

- Emulating the APU with high accuracy is essential for reproducing the authentic audio experience of NES games. This includes accurately implementing the frequency sweeps, volume envelopes, and other nuances of the original hardware.

x). Synchronization with CPU:

- The APU needs to be synchronized with the CPU to ensure that sound changes occur at the correct times. This often involves coordinating the APU clock cycles with the overall system clock.

xi). Sample Rate and Buffering:

- Determining the sample rate at which the emulator processes audio is crucial. Proper buffering techniques should be employed to ensure smooth audio playback without glitches or interruptions.

xii). Real-time Audio Rendering:

- Implementing real-time audio rendering is necessary for a responsive and immersive gaming experience. The emulator needs to generate audio samples and pass them to the audio subsystem for playback in a timely manner.

xiii). Integration with Emulator Core:

- The APU needs to be integrated into the overall emulator architecture, interacting with the Bus component to read and write memory-mapped registers. It also needs to respond to events such as resets and frame sequencer updates.

xiv). Testing and Debugging:

- Extensive testing and debugging are crucial for ensuring that the APU accurately reproduces the audio of various NES games. This includes testing against reference hardware or known good implementations.

4. Implementation and Testing

4.1 Tools and Technologies used for Project work:

I. Programming Language:

- C++ This is the language used for emulator development due to its performance and low-level capabilities given its strong support for system-level programming.

II. Integrated Development Environment (IDE):

- Visual Studio provide a comprehensive set of tools for C++ development, including code editing, debugging, and project management.

III. Version Control:

- Git: Git is widely used for version control, allowing developers to track changes, collaborate, and manage the project's source code effectively. Platforms like GitHub or GitLab are commonly used for hosting repositories.

IV. Build System:

- CMake: Build systems like CMake is employed to automate the compilation and building of the emulator project. They help manage dependencies and ensure the project is portable across different platforms.

V. Graphics Library:

- OpenGL: Use OpenGL for graphics rendering instead of SDL. OpenGL is a powerful cross-platform graphics API that can be utilized for rendering the NES graphics.

VI. Audio Library:

- SDL Audio: SDL Audio was utilized to handle audio output. These libraries allow for generating and playing back audio samples.

VII. Debugger/Profiler:

- Visual Studio Debugger: Debuggers help identify and fix issues in the code, while profilers like Valgrind (for memory profiling) can aid in optimizing the emulator's performance.

4.2 Algorithm/Pseudocode used:

a simplified overview of the key components and processes involved in the emulator. This pseudocode assumes a basic understanding of NES hardware architecture.

plaintext

Copy code

```
// NES Emulator Pseudocode


// Initialize NES Emulator
function initializeNES():
    // Create and initialize components
    createAndInitializeCPU()
    createAndInitializePPU()
    createAndInitializeAPU()
    createAndInitializeBus()
    loadCartridge()
    // Other initialization tasks


// Emulator Main Loop
function runEmulator():
    while (true):
        // Execute one frame
        executeFrame()
```

```
// Execute one frame
function executeFrame():
    // Reset PPU for a new frame
    ppu.reset()

    // Execute CPU cycles for the frame
    while (not inVBlank):
        // Clock the CPU
        bus.clock()
        // Clock the PPU (3 times slower than CPU)
        if (cpuCycles % 3 == 0):
            ppu.clock()
        // Handle APU events
        apu.clock()

    // Handle user input
    processInput()

    // Render graphics
    renderGraphics()

    // Play audio
    playAudio()

// Process user input
```

```
function processInput():
    // Read input from controllers
    bus.controller[0] = readControllerInput(0)
    bus.controller[1] = readControllerInput(1)

// Render graphics
function renderGraphics():
    // Update graphics buffer based on PPU state
    graphicsBuffer = ppu.getGraphicsBuffer()

    // Render graphics buffer using OpenGL or other graphics library

// Play audio
function playAudio():
    // Generate audio samples based on APU state
    audioSamples = apu.generateAudioSamples()

    // Play audio samples using audio library

// Read controller input
function readControllerInput(controllerNumber):
    // Read input from physical controllers or simulate input
    // Map input to controller registers on the Bus

// Load NES cartridge
```

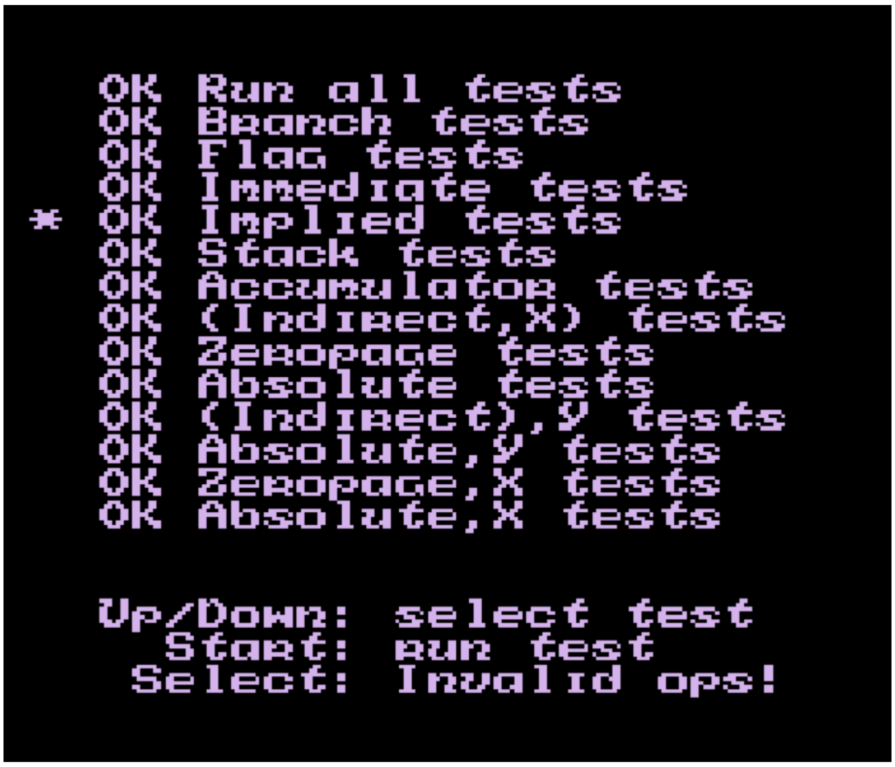
```
function loadCartridge():
    // Prompt user to select a ROM file
    romFile = selectROMFile()

    // Create a Cartridge object and insert it into the Bus
    cartridge = createCartridge(romFile)
    bus.insertCartridge(cartridge)

// Create and initialize CPU
function createAndInitializeCPU():
    // Create CPU object
    bus.cpu = new olc6502()

    // Set CPU reset vector and other initial configuration

// Create and initialize PPU
function createAndInitializePPU():
    // Create PPU object
    bus.ppu = new olc2C02()

    // Set initial PPU configuration

// Create and initialize APU
function createAndInitializeAPU():
    // Create APU object
    bus.apu = new APU()


    // Set initial APU configuration


// Create and initialize Bus
function createAndInitializeBus():
    // Create Bus object


    // Connect CPU, PPU, APU, and other components to the Bus
    bus.cpu.ConnectBus(bus)
    bus.ppu.ConnectBus(bus)
    bus.apu.ConnectBus(bus)
    // Other components


// Select a ROM file
function selectROMFile():
    // Use a file dialog to prompt the user to select a ROM file
    // Return the selected file path


// Create Cartridge object
function createCartridge(romFile):
    // Create a Cartridge object from the specified ROM file
    // Initialize the Cartridge with ROM data
    // Return the created Cartridge
```

This pseudocode provides a simplified representation of the main components and processes involved in an NES emulator. Keep in mind that actual implementation details, especially for the CPU, PPU, and APU, are much more complex and involve detailed knowledge of the NES hardware architecture. The pseudocode serves as a high-level overview and starting point for furth.

4.3 Testing Techniques and Test Cases:

For us project we have created and compiled an NES Rom which includes all the test cases and in case any of the case fails the problem is logged into the terminal and the interrupt is called.

The figure shows various test cases for invalid opcodes.



```
   OK Run all tests
   OK Branch tests
   OK Flag tests
   OK Immediate tests
 * OK Implied tests
   OK Stack tests
   OK Accumulator tests
   OK (Indirect,X) tests
   OK Zeropage tests
   OK Absolute tests
   OK (Indirect),Y tests
   OK Absolute,Y tests
   OK Zeropage,X tests
   OK Absolute,X tests

   Up/Down: select test
     Start: run test
    Select: Invalid ops!
```

Figure 23 Tests for Invalid Opcodes

Some of the test cases used by our ROM are:

I. Branch Tests:

i). Branch on Zero (BEQ):

- Set the zero flag.
- Execute a BEQ instruction with a branch offset.

- Verify that the program counter (PC) correctly updates if the zero flag is set.

ii). Branch on Not Zero (BNE):

- Clear the zero flag.
- Execute a BNE instruction with a branch offset.
- Verify that the PC correctly updates if the zero flag is not set.

iii). Branch on Carry Clear (BCC):

- Clear the carry flag.
- Execute a BCC instruction with a branch offset.
- Verify that the PC correctly updates if the carry flag is clear.

iv). Branch on Carry Set (BCS):

- Set the carry flag.
- Execute a BCS instruction with a branch offset.
- Verify that the PC correctly updates if the carry flag is set.

v). Branch on Negative (BMI):

- Set the negative flag.
- Execute a BMI instruction with a branch offset.
- Verify that the PC correctly updates if the negative flag is set.

vi). Branch on Positive or Zero (BPL):

- Clear the negative flag.
- Execute a BPL instruction with a branch offset.
- Verify that the PC correctly updates if the negative flag is clear.

II. Flag Tests:

i). Clear Carry Flag (CLC):

- Set the carry flag.
- Execute a CLC instruction.
- Verify that the carry flag is clear.

ii). Set Carry Flag (SEC):

- Clear the carry flag.
- Execute a SEC instruction.
- Verify that the carry flag is set.

iii). Clear Zero Flag (CLC):

- Set the zero flag.
- Execute a CLZ instruction.
- Verify that the zero flag is clear.

iv). Set Zero Flag (SEC):

- Clear the zero flag.
- Execute a SEZ instruction.
- Verify that the zero flag is set.

v). Clear Overflow Flag (CLV):

- Set the overflow flag.
- Execute a CLV instruction.
- Verify that the overflow flag is clear.

vi). Set Overflow Flag (SEC):

- Clear the overflow flag.
- Execute a SEV instruction.
- Verify that the overflow flag is set.

III. Immediate Tests:

i). Load Accumulator Immediate (LDA #Value):

- Load a specific value into the accumulator using the immediate addressing mode.
- Verify that the accumulator contains the expected value.

ii). Add with Carry Immediate (ADC #Value):

- Load a value into the accumulator.
- Execute an ADC instruction with an immediate value.

- Verify that the accumulator contains the correct sum with the carry.

iii). AND Immediate (AND #Value):

- Load a value into the accumulator.
- Execute an AND instruction with an immediate value.
- Verify that the accumulator contains the correct bitwise AND result.

IV. Implied Tests:

i). Clear Carry Flag (CLC):

- Set the carry flag.
- Execute a CLC instruction (implied addressing mode).
- Verify that the carry flag is clear.

ii). Clear Decimal Mode (CLD):

- Set the decimal mode flag.
- Execute a CLD instruction (implied addressing mode).
- Verify that the decimal mode flag is clear.

iii). No Operation (NOP):

- Execute a NOP instruction (implied addressing mode).
- Verify that the CPU state remains unchanged.

5. Results and Discussions

5.1 User Interface Representation

As a NES emulator often operates in a console or command-line environment, the user interface representation is code-based. The primary interface involves running the emulator through a command-line interface, specifying the NES ROM file to load.

5.1.1 Brief Description of Various Modules of the System

i). CPU Module:

- Responsible for executing NES CPU instructions.
- Implements various addressing modes, arithmetic, and logical operations.

ii). PPU Module:

- Manages the Picture Processing Unit responsible for graphics rendering.
- Includes components for rendering backgrounds, sprites, and handling nametables.

iii). APU Module:

- Manages the Audio Processing Unit responsible for generating sound.
- Handles different sound channels, volume, and frequency control.

iv). Bus Module:

- Acts as a communication bus connecting CPU, PPU, APU, and other components.
- Handles memory reads and writes, facilitating data exchange between components.

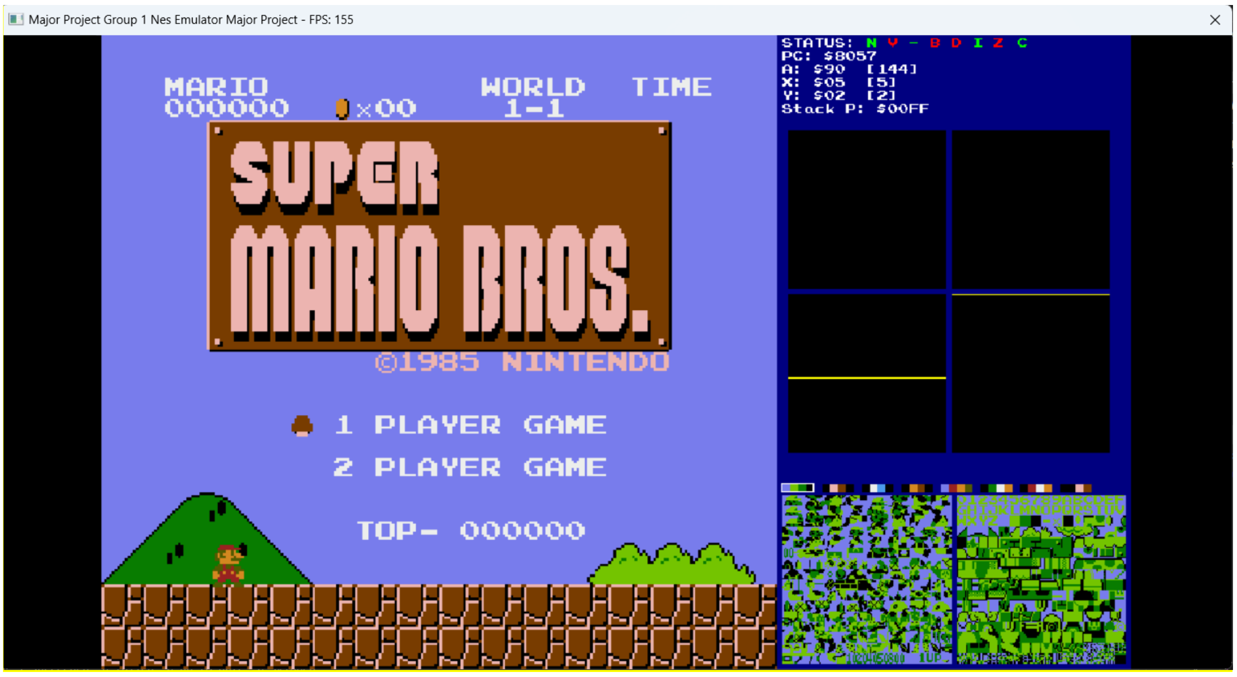
v). Cartridge Module:

- Represents the NES cartridge, including ROM and potentially RAM.
- Manages loading and handling game data from the cartridge.

5.2 Snapshots of the System with Brief Details and Discussion:

I. Emulator in Action:

The figure shows the emulator running the Super Mario Bros. (World ROM)

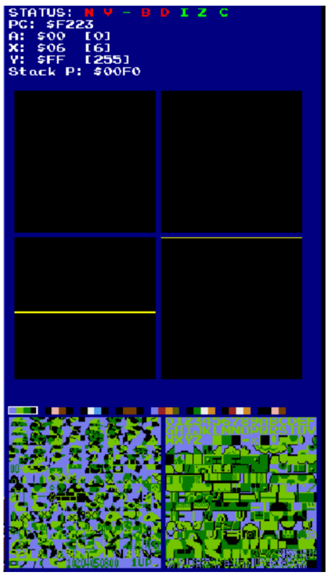


```
STATUS: N V - B D I Z C
PC: $8057
A: $90  [144]
X: $05  [5]
Y: $02  [2]
Stack P: $00FF
```

Figure 24 Emulator running Super Mario Bros. (World)

II. Debugging Features:

The following figure shows the various debugging tools which showcases the various register states. The current address of the PC and the various values of the registers.



```
STATUS: N V - B D I Z C
PC: $F223
A: $00  [0]
X: $06  [6]
Y: $FF  [255]
Stack P: $00F0
```

Figure 25 PPU and CPU Debugging Interface

6. Conclusion and Future Scope

6.1 Conclusion

Emulating the MOS 6502 for vintage computing offers a balance between preservation, accessibility, education, and community engagement. It provides an excellent educational tool for learning about computer architecture and low-level programming. It can serve as a hands-on way for students and hobbyists to understand the inner workings of early microprocessors. It ensures the enthusiasts can continue to run and experience programs and games. Emulation makes it easier to access vintage computing experiences without the need for rare and often expensive hardware. There is debugging tools so that developers can write and test code more efficiently, speeding up the process of creating or porting software for these classic platforms.

6.2 Future Scope

The future scope for emulating MOS 6502 for vintage computing involves a blend of technological advancements, community collaboration, educational initiatives. Emulators may become more seamlessly integrated with modern computing platforms, allowing for easier accessibility and use. It could play a significant role in educational initiatives, providing hands-on experiences for learning about computer architecture and programming. The retro computing community may contribute to and drive further emulation projects. Collaboration could result in the development of new emulators, enhancements to existing ones, and the creation of tools to simplify the emulation experience.

7. References

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