

NAMEER IQBAL ANSARI

✉ n.i.ansari200@gmail.com · 📞 03363033155 · [in](#) · [🌐](#)

OBJECTIVE

As an individual, NAMEER is known for his dedication, organization, and methodical approach. He excels in interpersonal skills, which makes him an excellent team worker. He possesses a strong desire to learn and develop new skills, always seeking new responsibilities in diverse and challenging areas. He is reliable, trustworthy, and eager to positively impact the field of Open-Source Semiconductor technology.

EDUCATION

- Usman Institute of Technology University** Karachi, Pakistan 📍 📅 July 2019 ▶ Now
Electrical Engineering (Computer Systems) ; GPA: 3.3/4
Courses: Digital logic Design, Digital Image processing, Embedded Systems, Computer Graphics, Programming Fundamentals, Data Structures and Algorithms, Computer Architecture, Data Base Management System, Data Warehouse etc ..
- Adamjee Government and Science college** Karachi, Pakistan 📍 📅 2017 ▶ 2019
Secondary Education (Intermediate in Science)
- S.M.Public Acadmey** Karachi, Pakistan 📍 📅 2010 ▶ 2017
Primary Education (Matriculation in Science)

PROFESSIONAL SUMMARY

NAMEER IQBAL ANSARI is a BE (Computer System Engineering) student at the USMAN INSTITUTE OF TECHNOLOGY. He is pursuing his studies while actively contributing to the field of the Semiconductor industry field.

With a strong focus on RISC-V technology, NAMEER has dedicated 2 years to working in this field. His expertise lies in designing and testing RTL (Register Transfer Level) using hardware descriptive languages such as Verilog and SystemVerilog. He is proficient in tools like Xilinx, AWS-FPGA, Verilator, VCS, and more, ensuring high-quality results.

He is currently gaining valuable experience as a Research Intern at MERL (Micro Electronic Research Lab) at UITU Karachi. Additionally, he is a trainee at Xcelerium. With that he is a contributor in the GSoC'22 (Google Summer of Code) program, and a Co-Mentor for GSoC'23, demonstrating his commitment to personal growth and contribution to the open-source community.

SKILLS

Xilinx Vivado 📁	YAML 📁	Amazon EC2 Cloud FPGA 📁	Fusesoc 📁	Verilog 📁
C++ 📁	Proteus 📁	Cache 📁	ESP32n 📁	Linux 📁
MATLAB 📁	Logisim 📁	AutoCAD 📁	NI Multisim 📁	

WORK EXPERIENCE

Internship Trainee

Xcelerium

📅 Dec 2022 ▶ Now

- RTL designing.
- RTL verification, testbench, MakeFile scripting.

- C testing on a Virtual platform.

Research Intern

Micro Electronics Research Lab

📅 Mar 2021 ▶ Now

The journey begins with the creation of an [RV32I](#) processor from scratch in SystemVerilog. This involved designing and implementing the processor's architecture, instruction set, and control logic. After that, I implemented Tilelink uncached lightweight BUS and FuseSoC packet manager in that and simulated using Verilator. Through this process, I gained valuable insights into the intricacies of processor design and low-level hardware programming.

Now working on different Open-Source projects.

Co- Mentor

Google Summer Of Code 2023

📅 May 2023 ▶ Now

"TileLink Uncached Heavyweight (TL-UH) implementation in Azadi-SoC" is the project I'm mentoring.

[Project Link](#)

Contributor

Google Summer Of Code 2022

📅 Jun 2022 ▶ Sep 2022

The project aims to "Add FuseSoC support at SoC level for Azadi-SoC and Rebase ibex core with the latest commit". The ibex core used in the Azadi SoC was not the latest committed version, and Fusesoc was supported only on this ibex core which needed to support the whole SoC in this project. [Project Link](#)

OTHER PROJECTS

NOVA

📅 Feb 2022 ▶ Sep 2022

NOVA, an Open-Source System-on-Chip (SoC) that incorporated various peripherals such as UART, MATMUL, BRAM, PLIC, and CLINT, with DDR serving as the main memory. To validate the functionality and performance of the NOVA SoC, it was emulated on an AWS EC2 instance utilizing AWS Cloud FPGA capabilities. Additionally, the Zypher operating system was successfully booted on the NOVA SoC, further enhancing its capabilities. [Project Link](#)

MARCore

"Multicore SOC for SMP Linux" is my FINAL YEAR PROJECT, it is based on the OpenPiton Open-Source framework, used to generate cache coherence for multicore systems and Ariane as a base processor which is a 6-stage pipeline RISC-V IMFC processor. [Project Link](#)

AWARDS AND HONORS

Scholarship - HASHAM CHARITABLE FOUNDATION

📅 Oct 2022

Got a scholarship in the 7th semester for one semester on the basis of CGPA.