Nameer Iqbal Ansari

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Education

Usman Institute of Technology University Karachi, Pakistan July 2019 ▸ Aug 2023
Electrical Engineering (Computer Systems) (CGPA: 3.289/4)
Courses: Digital logic Design, Digital Image processing, Embedded Systems, Computer Graphics, Programming Fundamentals, Data Structures and Algorithms, Computer Architecture, Data Base Management System, Data Warehouse
Scholarship: **HASHAM CHARITABLE FOUNDATION** Oct 2022

Adamjee Government and Science College Karachi, Pakistan 2017 ▸ 2019
Secondary Education (Intermediate in Science)

S.M.Public Acadmey Karachi, Pakistan 2010 ▸ 2017
Primary Education (Matriculation in Science)

Work Experience

Trainee Engineer at Xcelerium Sep 2023 ▸ Now

Research Intern at Micro Electronics Research Lab Mar 2020 ▸ Aug 2023

- Made RV32I processor from scratch in SystemVerilog in initial training.
- Implemented TLUH BUS, FuseSoC packet manager in that and simulated using Verilator and ported in Arty a7 FPGA in the second phase.
- Done some other OpenSource collaborative projects.

Internship Trainee at Xcelerium Nov 2022 ▸ Mar 2023

- RTL designing/verification, MakeFile scripting, C testing, Virtual platform.
- Worked on VCS, Questa, Verilator, AWS-FPGA, etc.

Contributor in Google Summer Of Code 2022 Jun 2022 ▸ Sep 2022
Project: **Add FuseSoC support at SoC level for Azadi-SoC and Rebase ibex core with the latest commit**

Leadership and Activities

Co- Mentor in Google Summer Of Code 2023 May 2023 ▸ Aug 2023
Project: **TileLink Uncached Heavyweight (TL-UH) implementation in Azadi-SoC**

Skills

Xilinx Vivado	YAML	Amazon EC2 Cloud FPGA	Fusesoc	Verilog
C++	Proteus	SystemVerilog	ESP32n	GitHub
MATLAB	GTKwaves	VCS	EDA playground	Verilator

Projects

- **MARCore (Multicore SOC for SMP Linux)**
- **NOVA1 (Open-Source System-on-Chip)**