Nameer Iqbal Ansari

0336-3033155 | nameeriqbalansari@gmail.com | Karachi, Pakistan
linkedin.com/in/nameer-ansari | github.com/Nameer-Iqbal-Ansari

Professional Summary

Computer Systems Engineer specializing in **SoC design**, **RTL development**, and **FPGA-based design**, with expertise in **RISC-V**. Hands-on experience in integrating **Synopsys** and other third-party IPs. Proficient in **Cadence** and **Synopsys tools**, and skilled in **Power, Performance, and Area (PPA) optimization**. Certified **RISC-V Foundational Associate (RVFA)**, committed to delivering scalable, verified, and high-quality designs.

Technical Expertise

Hardware Design: RTL Development (Verilog/SystemVerilog), Vector/Scalar LSU, JTAG infrastructure, High Speed subsystem using SerDes, PCIe, and CDC
Tools: Synopsys VCS, QuestaSim, Verilator, Vivado, Verdi, GTKWave, JasperGold
ASIC Implementation: SpyGlass, FusionCompiler, Prime Time, Timing Closure (12lpp)
Languages & Scripts: C/C++, RISC-V Assembly, Tcl, Shell Scripting, Makefile, CI/CD, Linux (Ubuntu)

Professional Experience

XCLR Technologies (Pvt.) Ltd. Karachi, Pakistan
Hardware Design Engineer *2025 – Present*

- Designed and verified microarchitecture for complex digital components like **Vector Load-Store Units (LSU)** and multilayered **cache subsystems**.
- Performed cycle improvements and reliability features within **Vector LSUs**, translating complex requirements into formal microarchitecture specifications.
- Led integration and configuration of **32Gbps SerDes** and **PCIe controller IPs** for high-bandwidth off-chip data transfer.
- Achieved **timing closure** for **RISC-V-based SoCs** by resolving setup/hold violations and placement bottlenecks at the **12lpp** technology node.
- Built **FPGA-based SoC subsystems** facilitating Shell-to-SoC interfacing with **JTAG**, **UART**, and **DDR4** support.

Xcelerium Karachi, Pakistan
Associate Engineer *Sept 2023 – 2025*

- Developed and validated **JTAG debug infrastructure** ensuring **AWS-SHELL compatibility** for SoC-level FPGA implementations.
- Performed emulation testing of SoC design via **C drivers** and **JTAG** to verify accessibility at both emulation and **AWS simulation environment** levels.
- Facilitated the use of **logic analyzers**, **CDCs**, **AXI**, **data width and bus protocol converters**, and **FSMs** in RTL.
- Authored comprehensive technical documentation and block diagrams to aid **design reviews** and **knowledge transfer**.

Micro Electronics Research Lab (MERL) Karachi, Pakistan
Research Assistant *Aug 2023 – Present*

- Developed open-source **RV32I CPU core** using **SystemVerilog**, simulated with **Verilator**, and emulated on **Arty A7 FPGA**.
- Speaker at **RISC-V Karachi Meetup 2023**, presenting architectural implementation of **NOVA1 SoC**.

Open Source Contributions & Research

Google Summer of Code (GSoC) MERL
Mentor (2023) & Contributor (2022) *2022 – 2023*

- Provided **FuseSoC** support on the **Azadi-SoC** and rebased the **Ibex core** to latest upstream commits, enhancing **IP modularity**.

NOVA1 & MARCore Projects MERL
Research Lead / Contributor *2021 – 2024*

- Optimized multicore **RTL** and **cache-coherent memory systems** using **OpenPiton** and **Ariane** to support full-stack **Linux boot workloads**.
- Developed **NOVA1 SoC**, an open-source SoC featuring integrated **ML accelerators** and **high-speed memory controllers** with **AWS-emulation** support.

Education & Certifications

Usman Institute of Technology Karachi, Pakistan
B.E. in Electrical Engineering (Major: Computer Systems) *2019 – 2023*

- **Certifications** : RISC-V Foundational Associate **(RVFA)**, RISC-V Fundamentals **(LFD210)**.
- **Honors**: Linux Foundation **LiFT** Scholarship Recipient (2024) .