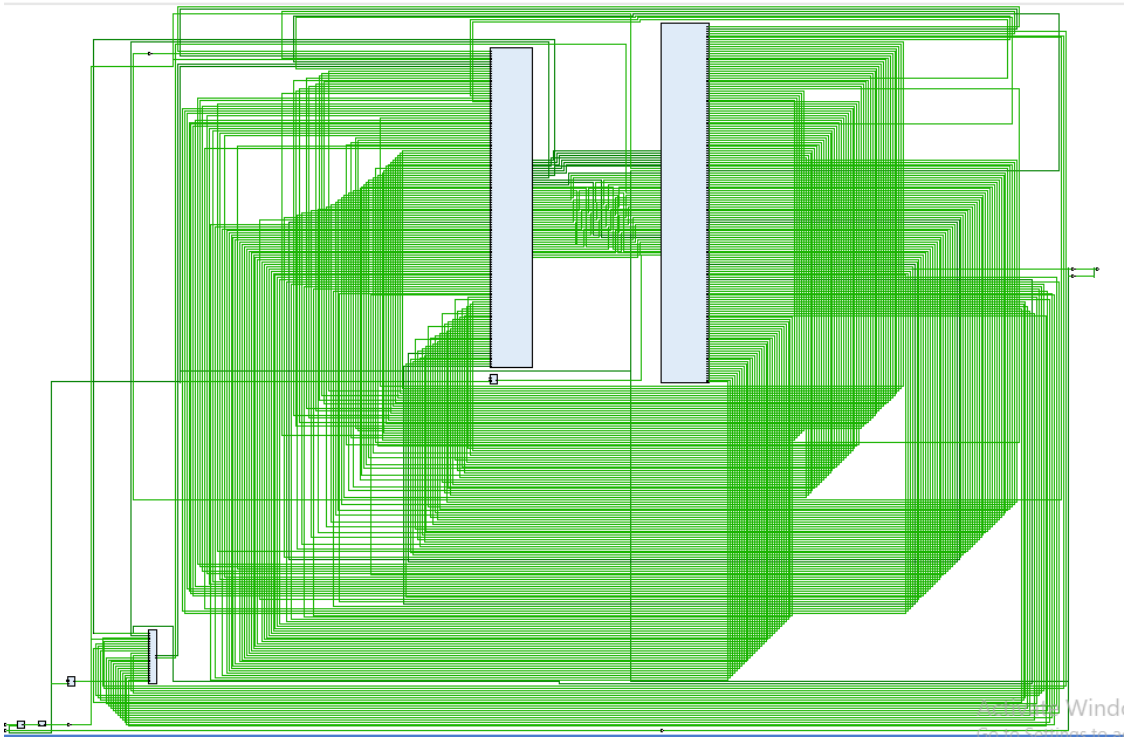
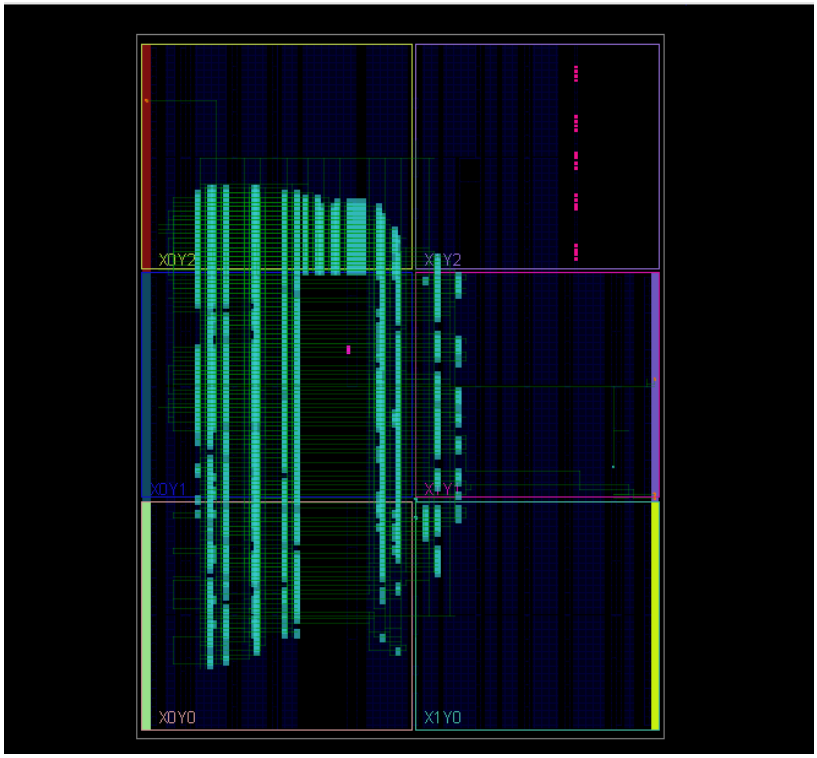
The core is tested on Arty A7-35T fpga and the following are the testing stages result's images:

SCHEMATIC DESIGN



Device



TIMING

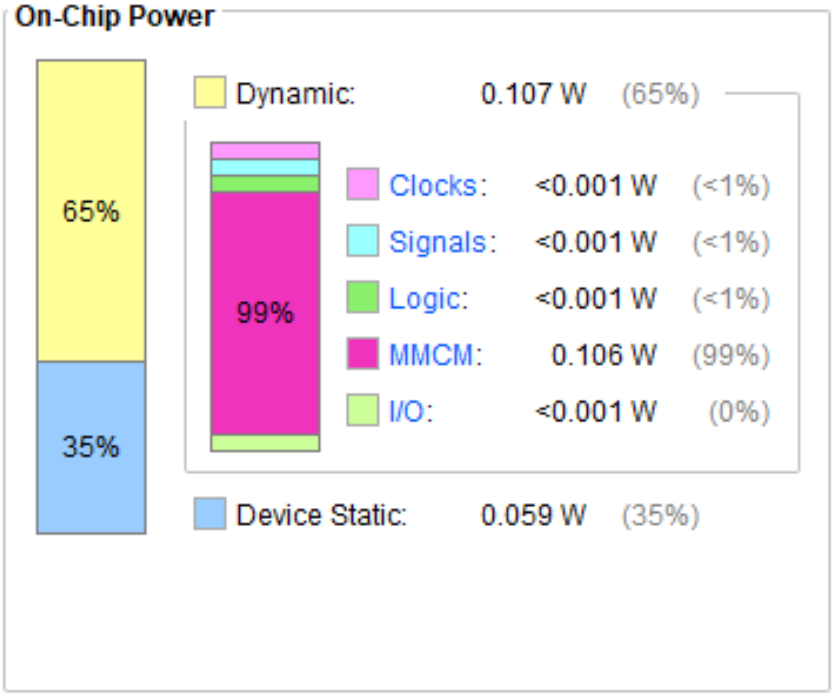
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	95.745 ns	Worst Hold Slack (WHS):	0.113 ns	Worst Pulse Width Slack (WPWS):	3.000 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	57	Total Number of Endpoints:	57	Total Number of Endpoints:	35

POWER

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.165 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.8°C**
Thermal Margin:	74.2°C (15.4 W)
Effective ϑJA:	4.8°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



REPORT UTILIZATION

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Bonded IOB (210)	BUFGCTRL (32)	MMCME2_ADV (5)
top_main	4836	1117	1409	544	1513	2084	2752	67	4	4	1
cd (Clock_divider)	12	29	0	0	12	12	0	2	0	0	0
clk_wiz (clk_wiz_0)	0	0	0	0	0	0	0	0	0	2	1
core (top)	1339	1088	257	0	650	1339	0	5	0	0	0
d2 (channel_d)	0	0	0	0	0	0	0	0	0	0	0
data_mem_adapter (d...	2224	0	1088	544	566	176	2048	0	0	0	0
inst_mem_adapter (in...	1263	0	64	0	407	559	704	0	0	0	0