MIPS Processor

GROUP - 10

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Motivation

- Old processors weren’t capable of using the hardware optimally.
- Additionally, they cannot process large sized data (in terms of bits).
- MIPS has a fixed-length, regularly encoded instruction set and uses a load/store data model.
- MIPS uses memory efficiently and parallelly uses all the stages.
- MIPS microprocessor are used in variety of applications like game consoles, office automation, internet modems and set-top boxes.
- MIPS is used by companies like NEC, Cisco, Silicon Graphics, Sony and Nintendo.

Specifications

Clock Speed 100 MHz

Can Perform upto 64 Unique Instructions

Data Bus 16 bit

High speed Multiplication

Address Bus 16 bit

Data Memory Storage Capacity : 1 MB

Number of I/O Pins : 37

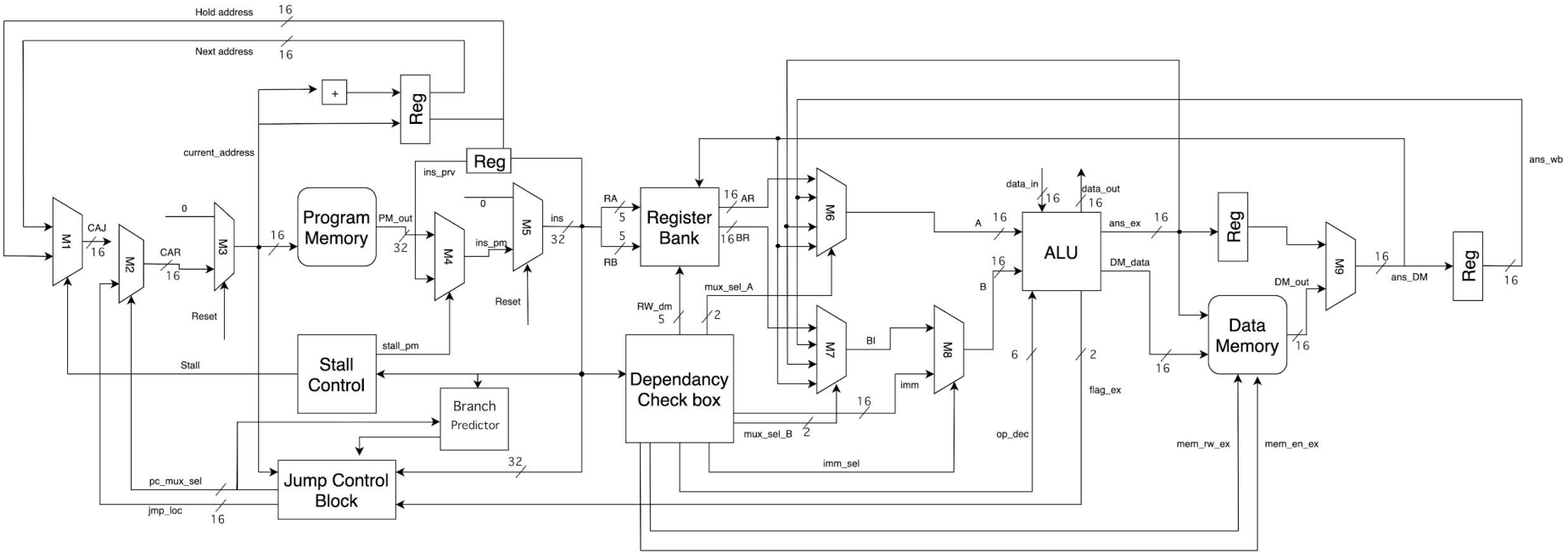
Single Cycle Pipelined Processor

16 bit RISC based Architecture

2 MB Program Memory ROM

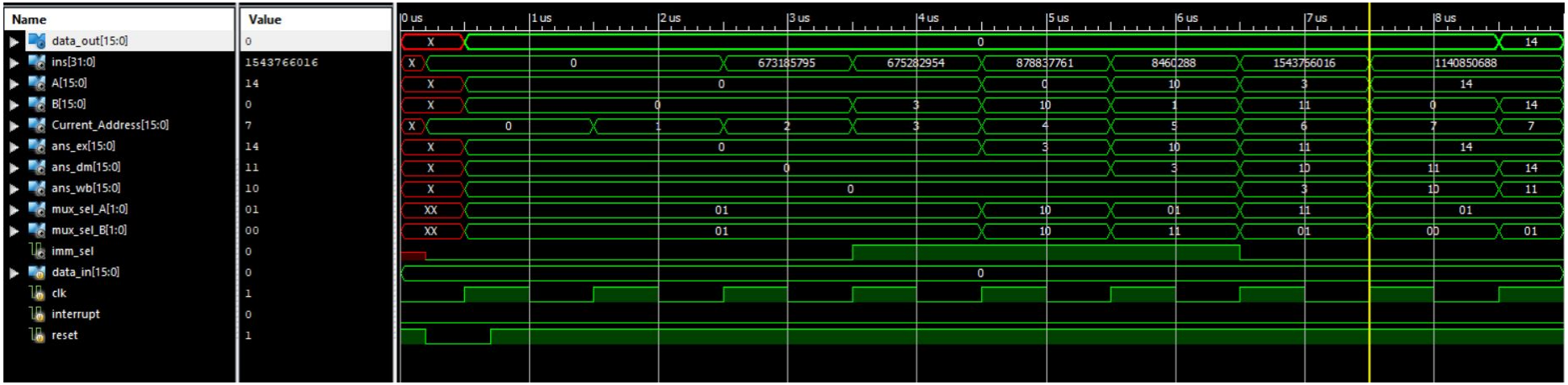
Branch Prediction

Block Diagram



Simulation Results

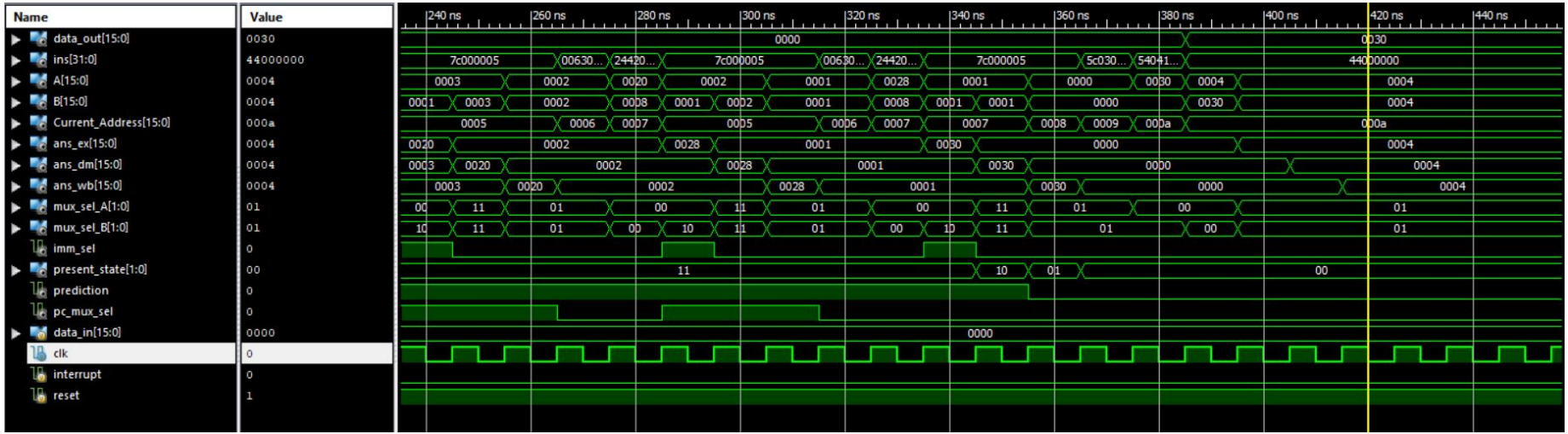
- Addition Instruction



Clock Speed : 500 ns
Addition Output : 8.5 µs

Simulation Results

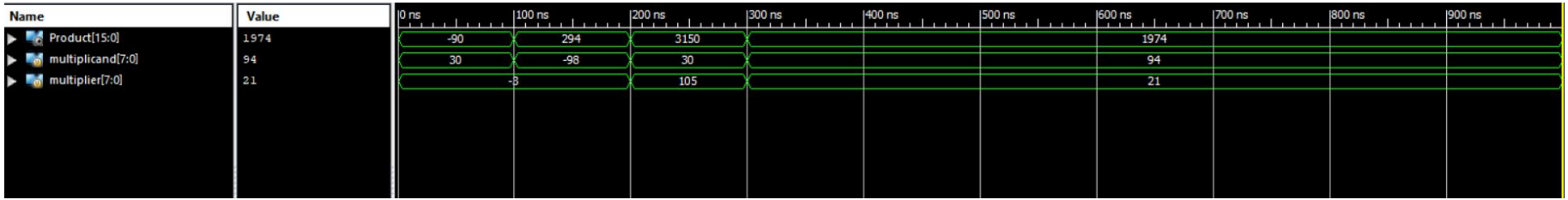
- Multiplication Instruction and Branch Prediction

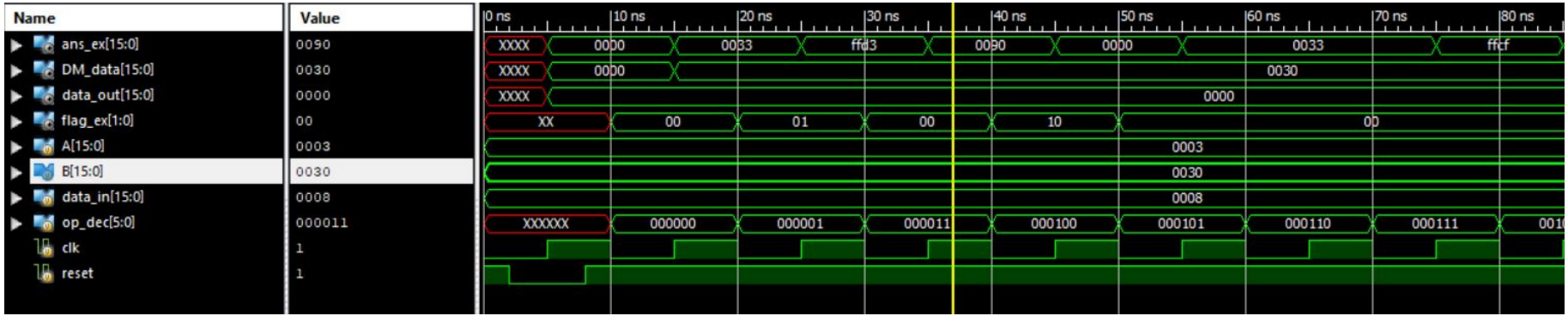


Clock Speed : 5 ns
Multiplication Results : 382.5 ns (ADD + SUB + JUMP (This all instructions has their own processing time))

Simulation Results

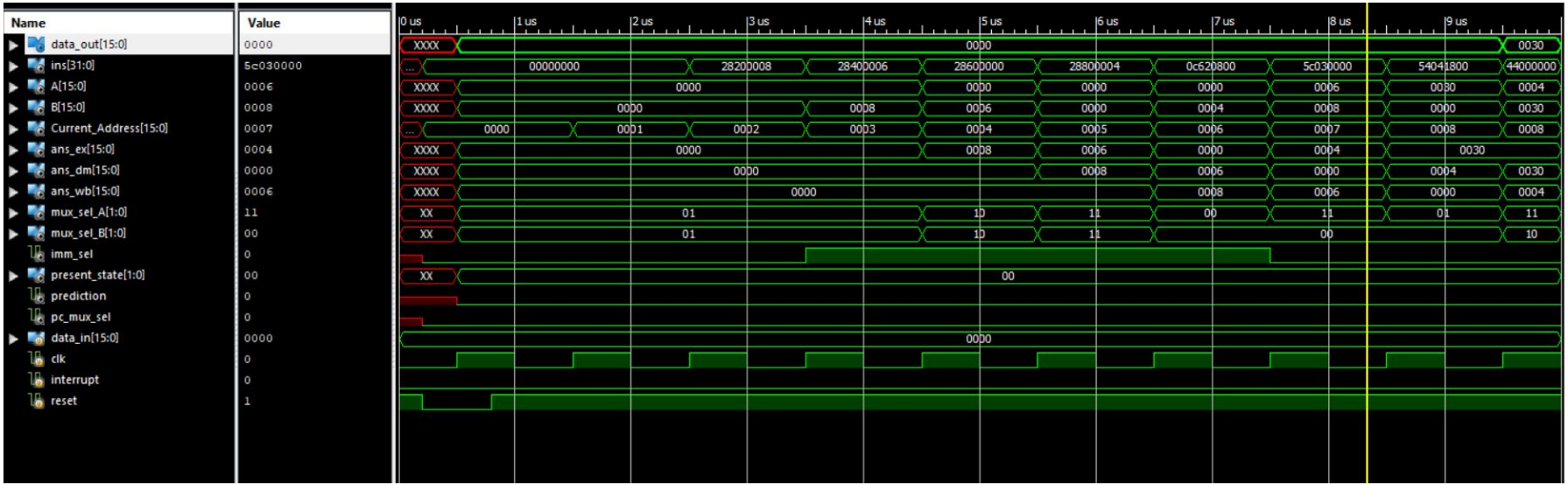
- Booth Multiplier (Separate Module Results & ALU Results)





Simulation Results

- Booth Multiplier (MIPS Results)



Clock Speed : 500 ns
Multiplication Output : 9.5 µs

Clock Speed : 5 ns
Multiplication Output : 95 ns

Simulation Results

Booth Multiplier

Clock Speed : 5 ns
Multiplication Output : 95 ns

```
ADD $0 $0 $0
MVI  $1 #0 #8
MVI  $2 #0 #6
MVI  $3 #0 #0
MVI  $4 #0 #4
BTH $3 $2 $1
OUT #0 $2 #0
ST    #0 $4 $3
HLT  #0 #0 #0
```

VS

Normal Multiplication

Clock Speed : 5 ns
Multiplication Results : 382.5 ns

```
ADD $0 $0 $0
MVI  $1 #0 #8
MVI  $2 #0 #6
MVI  $3 #0 #0
MVI  $4 #0 #4
ADD $3 $3 $1
SBI   $2 $2 #1
JNZ  #0 #05
OUT #0 $2 #0
ST    #0 $4 $3
HLT  #0 #0 #0
```

Comparison

VS

8085

Intel's world famous berserker

MIPS

Our beloved MIPS architecture

8085		MIPS
8 bits	← Data Width →	16 bits
16 bits	← Address Width →	16 bits
Von - Neumann	← Architecture →	Harvard
246	← Instructions →	29
Semi - CISC	← ISA →	RISC
X	← Pipelining →	✓
✓	← Accumulator→	X
8	← No. of Registers →	32
16 bits	← IR →	32 bits
2 bits	← Memory Control →	1 bit

Challenges

Multiply error

We got wrong answer while multiplying two numbers as we stalled excessively in the Jump Control Block

Booth Delay

Booth algorithm took more cycles than expected in the development phase due to code error

WARNING!

Avoiding warnings while designing the architecture was another major challenge

Module Integration

We got wrong answer while multiplying two numbers as we stalled excessively in the Jump Control Block

Feedback of pipeline Processor

- Pipelining increased the speed up factor of processor, thus reducing the time of instruction execution.
- Cache memory , multi core processor and floating point values are some functionality that can be added to our processor to make it faster and more user friendly .
- Efficient use of all the components of the processor is possible through pipelining, while it is not possible in non pipelined processor.