

EE_533_Neuromorphic Computing PROJECT-1

Analysis 1: Channel-length dependence of the Early voltage in MOS deep inversion (over threshold)

- a. For an nMOS, perform an I_{DS} vs. V_{DS} sweep at $V_{GS} = 1\text{ V}$ for $(W/L) = (1/1)$ when $L = [1, 2, 5, 10, 25, 50]\text{ }\mu\text{m}$.

Simulation Setup

For the simulation, a new **library named "Neuromorphic_project_1"** was created, and a corresponding **cell named "nmos_IDS_VDS_Sweep_L"** was implemented. The **technology library "NCSU_TechLib_tsmc04_4M2P"** was selected and attached to the existing technology database. The **schematic design** consists of an **nMOS transistor** connected with appropriate **voltage sources (V_GS and V_DS)** to perform the required sweep analysis. The entire setup and simulations were executed using **Cadence ADE L (Analog Design Environment)**.

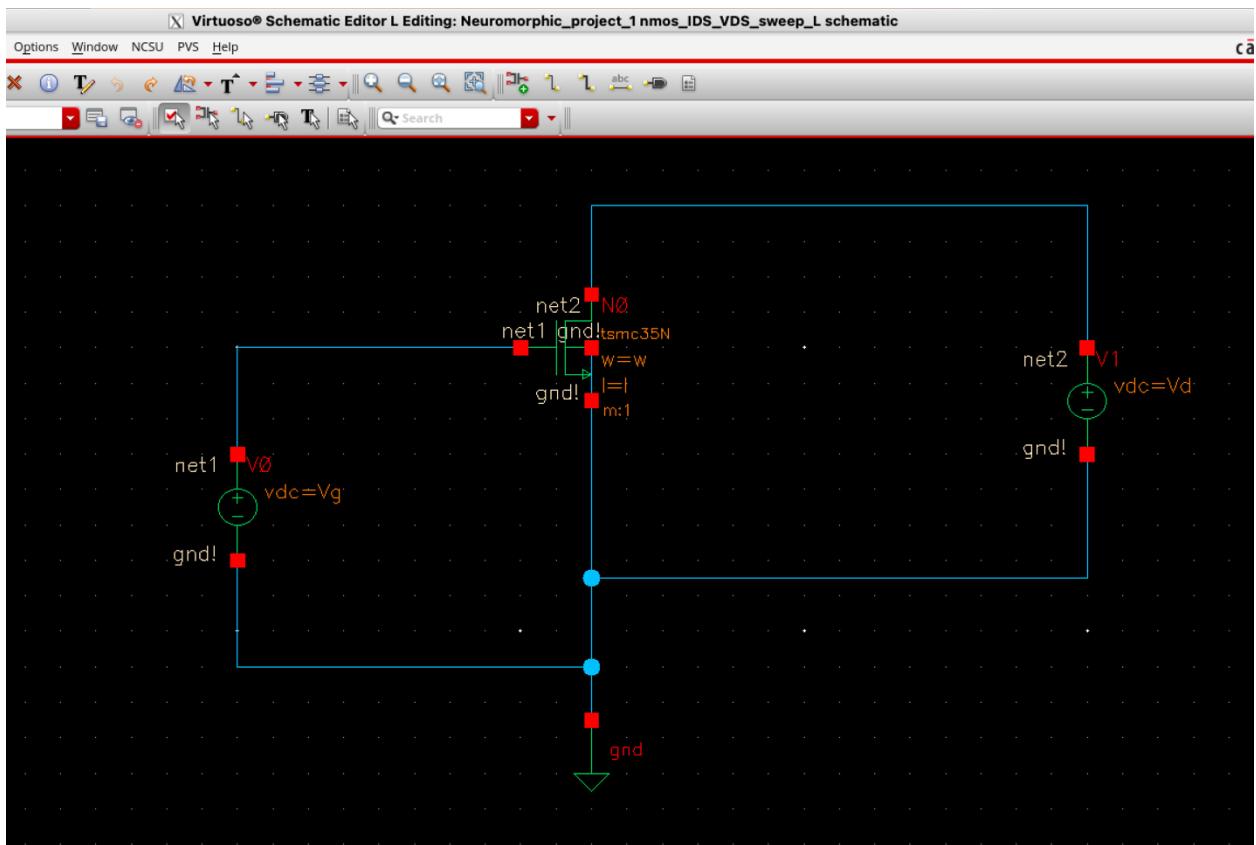
Design Parameters and Setup

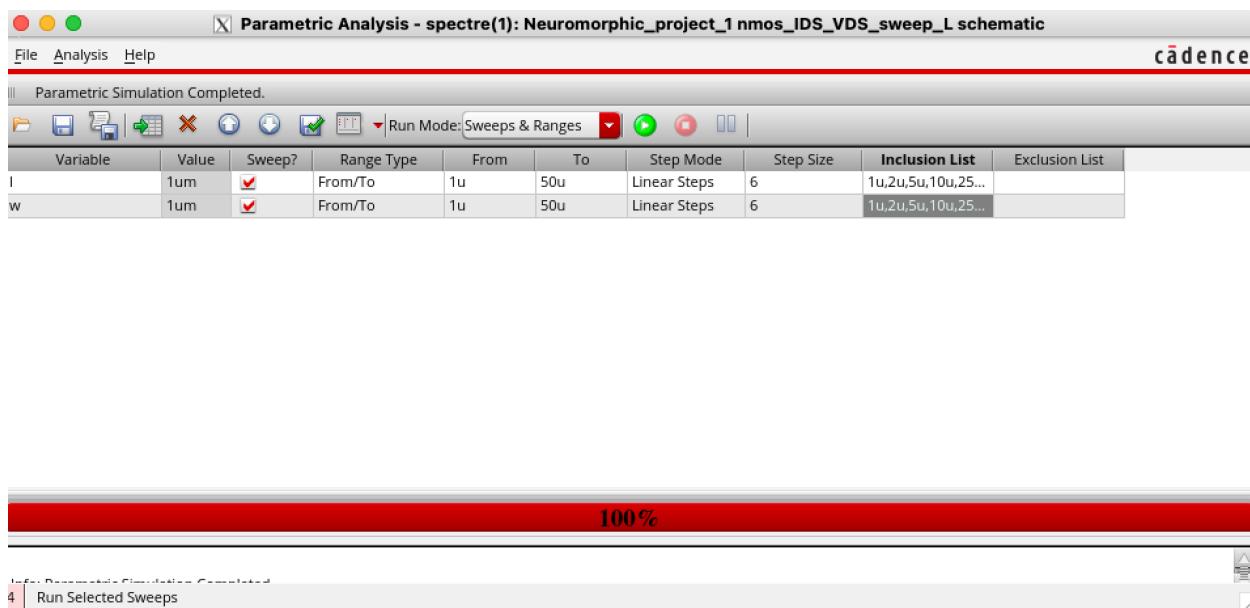
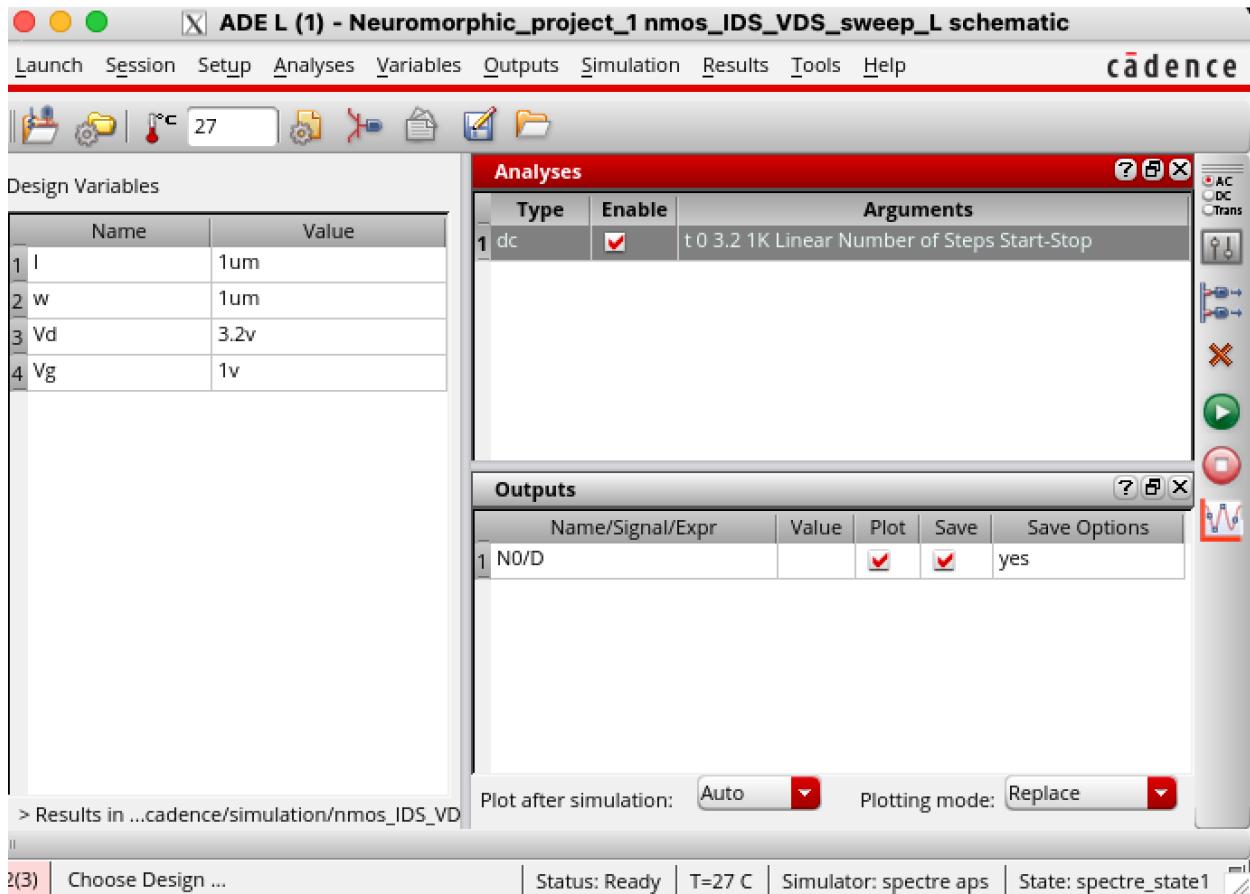
The primary design variables include **L = 1 μm** as the initial value, which is later varied across **[1, 2, 5, 10, 25, 50] μm** , while the transistor width remains constant at **W = 1 μm** . The applied voltages are **V_G = 1V** and **V_D = 3.2V**. The simulation is configured as a **DC Sweep**, where **V_DS** is selected as the sweeping variable. The **start-to-stop range** for **V_DS** is set from **0V to 3.2V**, with a **linear sweep** method. The **step size** is chosen to be **1k**, ensuring a sufficient number of data points for an accurate analysis of the transistor's behavior in different saturation regions.

Parametric Analysis Setup

To analyze the effect of channel length (L) on the transistor's characteristics, a **parametric sweep** was performed in **Cadence ADE L**. The **sweep variable** was set to **L (length of the transistor)**, allowing multiple simulations for different values of L within the defined range.

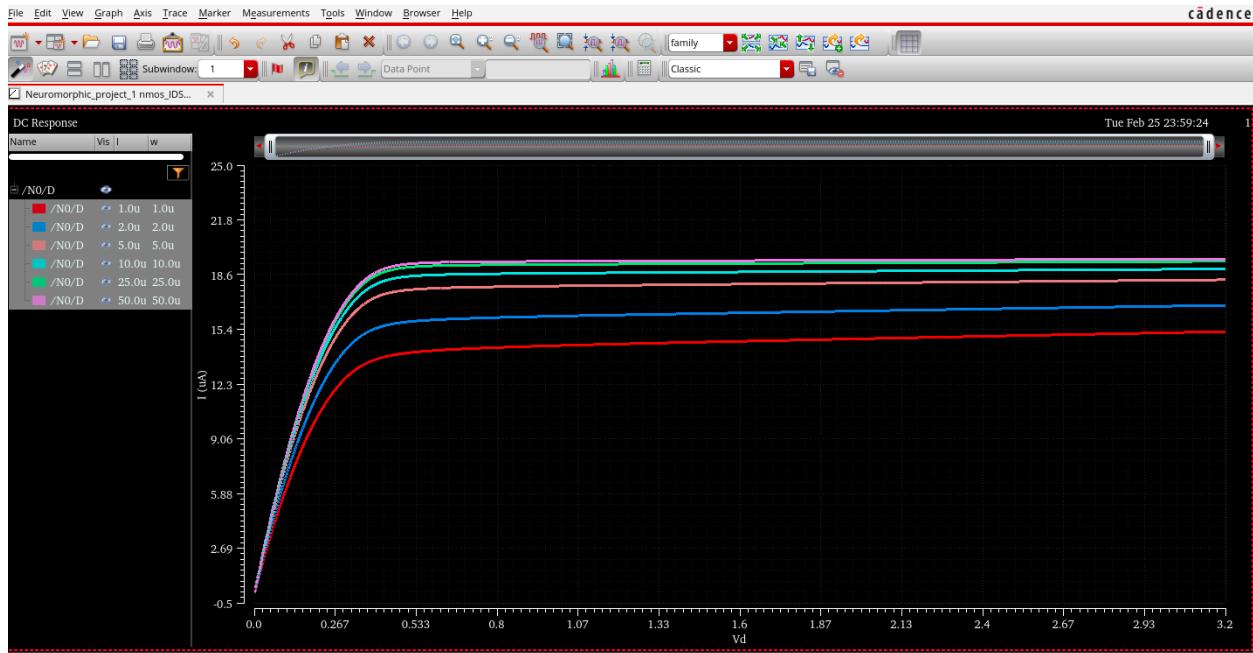
The **sweep range** for L was set from **1 μm to 50 μm** , with specific discrete values: **1u, 2u, 5u, 10u, 25u, and 50u**. A **linear step mode** was chosen to ensure an even distribution of data points, and the **step size** was set to **6**, determining the increment between each simulation point. This setup allowed the extraction of relevant transistor parameters, ensuring a detailed comparative analysis of **output resistance (r_o)** across different L values.





DC RESPONSE OF IDS vs. VDS sweep at $VGS = 1\text{ V}$ for $(W/L) = (1/1)$ when

$L=W = [1, 2, 5, 10, 25, 50]\mu\text{m}$.



b. Calculating the output resistance, r_o , in the saturation region for each case.

⑥ In saturation region for calculating r_o :

We know that,

$$r_o = \frac{V_L - V_I}{I_2 - I_1} \quad \text{--- (1)}$$

Case(i) :- $(W, L) = (1, 1)$ $(V_{ds1}, I_{ds1}) = (1.2864V, 14.6157mA)$
 $(V_{ds2}, I_{ds2}) = (2.9248V, 15.21mA)$

Case(ii) :- $(W, L) = (2, 2)$ $(V_{ds1}, I_{ds1}) = (1.2768V, 16.295mA)$
 $(V_{ds2}, I_{ds2}) = (2.9376V, 16.765mA)$

Case(iii) :- $(W, L) = (5, 5)$ $(V_{ds1}, I_{ds1}) = (1.2864V, 18.0147mA)$
 $(V_{ds2}, I_{ds2}) = (2.9184V, 18.2792mA)$

Case(iv) :- $(W, L) = (10, 10)$ $(V_{ds1}, I_{ds1}) = (1.2384V, 18.7365mA)$
 $(V_{ds2}, I_{ds2}) = (2.9184V, 18.7233mA)$

Case(v) :- $(W, L) = (25, 25)$ $(V_{ds1}, I_{ds1}) = (1.2704V, 19.2432mA)$
 $(V_{ds2}, I_{ds2}) = (2.9376V, 19.3777mA)$

Case(vi) :- $(W, L) = (50, 50)$ $(V_{ds1}, I_{ds1}) = (1.296V, 19.2454mA)$
 $(V_{ds2}, I_{ds2}) = (2.9984V, 19.3869mA)$

Case(i) :- $r_o = \frac{1.6384}{0.5943} = 2.7M\Omega$

Case(ii) :- $r_o = \frac{1.6608}{0.47} = 3.42M\Omega$

Case(iii) :- $r_o = \frac{2.2686}{0.2645} = 8.57M\Omega$

Case(iv) :- $r_o = \frac{1.6804}{0.1868} = 9M\Omega$

Case(v) :- $r_o = \frac{1.66836}{0.1345} = 12.4M\Omega$

Case(vi) :- $r_o = \frac{1.6384}{0.1345} = 12.4M\Omega$

Part (c) Extracting the early voltage, (V_A)

⑤ Extracting the early voltage, (V_A) :-

$$V_A = \gamma_o \cdot I_{ds}$$

$$\text{Case(i)} : - I_{ds} = \frac{I_{ds1} + I_{ds2}}{2} = \frac{14.6157 + 15.21}{2} = 14.91 \text{ mA}$$

$$\text{Case(ii)} : - I_{ds} = \frac{16.295u + 16.705u}{2} = 16.53 \text{ mA.}$$

$$\text{Case(iii)} : - I_{ds} = \frac{18.0147 + 18.2792}{2} = 18.14 \text{ mA.}$$

$$\text{Case(iv)} : - I_{ds} = \frac{18.7365 + 18.9233}{2} = 18.82 \text{ mA}$$

$$\text{Case(v)} : - I_{ds} = \frac{19.2432 + 19.3777}{2} = 19.31 \text{ mA}$$

$$\text{Case(vi)} : - I_{ds} = \frac{19.245u + 19.3825}{2} = \frac{19.315}{2} \text{ mA.}$$

$$\Rightarrow V_{Ai} = 14.91 \times 10^{-6} \times 2.7 \times 10^6 = 40.25 \text{ V}$$

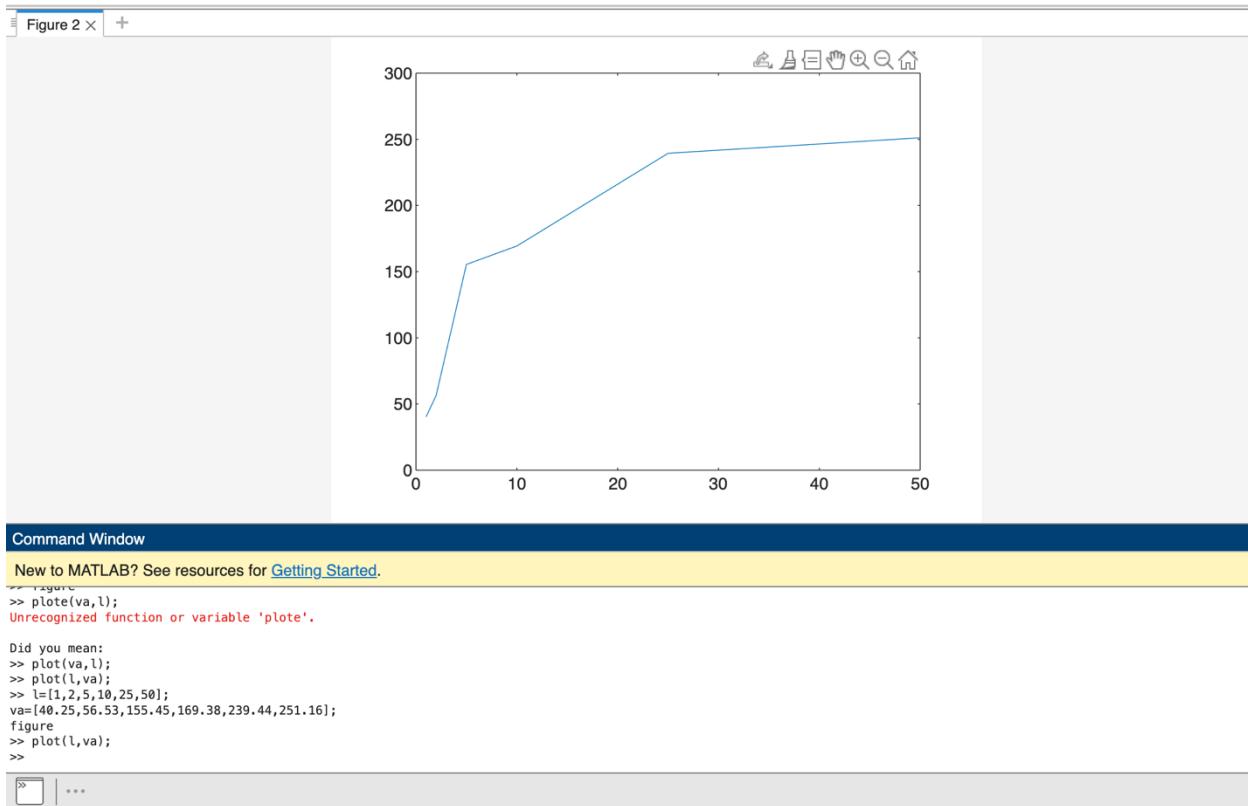
$$\Rightarrow V_{Aii} = 3.42 \times 10^{-6} \times 16.53 \times 10^6 = 56.53 \text{ V}$$

$$\Rightarrow V_{Aiii} = 18.14 \times 10^{-6} \times 8.57 \times 10^6 = 155.45 \text{ V}$$

$$\Rightarrow V_{Aiv} = 9 \times 10^{-6} \times 18.82 \times 10^6 = 169.38 \text{ V}$$

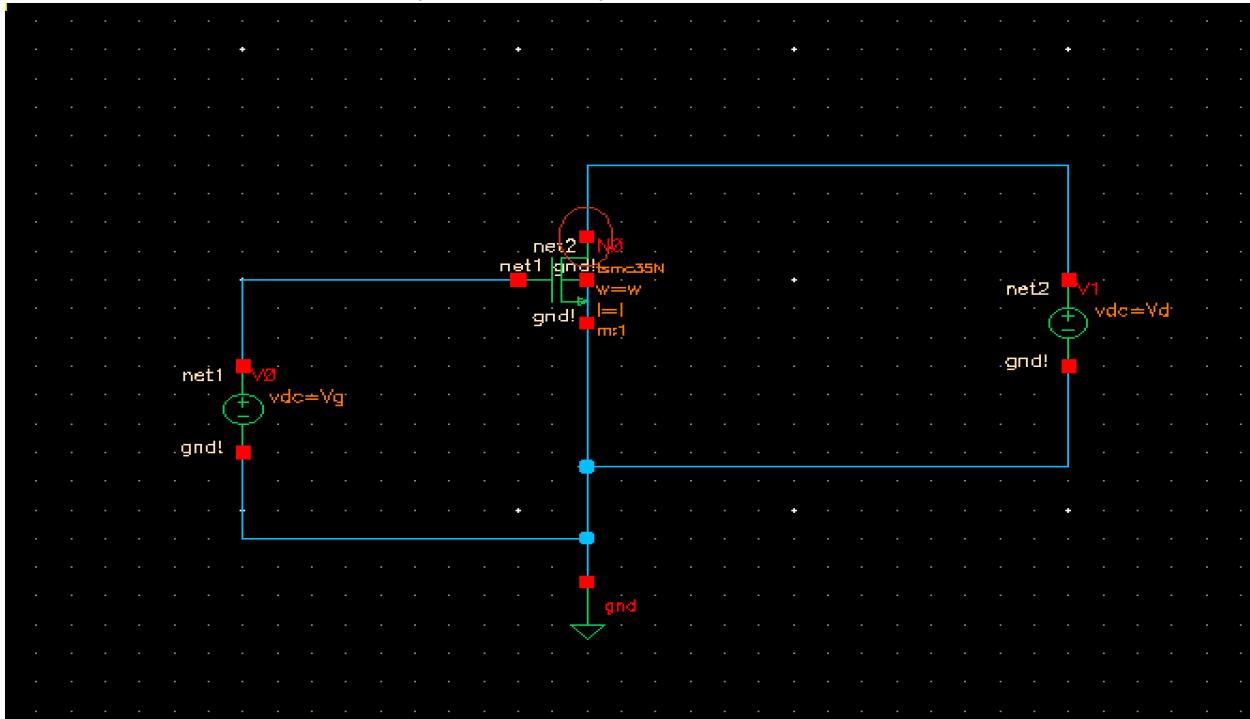
$$\Rightarrow V_{Av} = 12.4 \times 10^{-6} \times 19.31 \times 10^6 = 239.44 \text{ V}$$

$$\Rightarrow V_{Avi} = 13 \times 10^{-6} \times 19.38 \times 10^6 = 251.16 \text{ V}$$

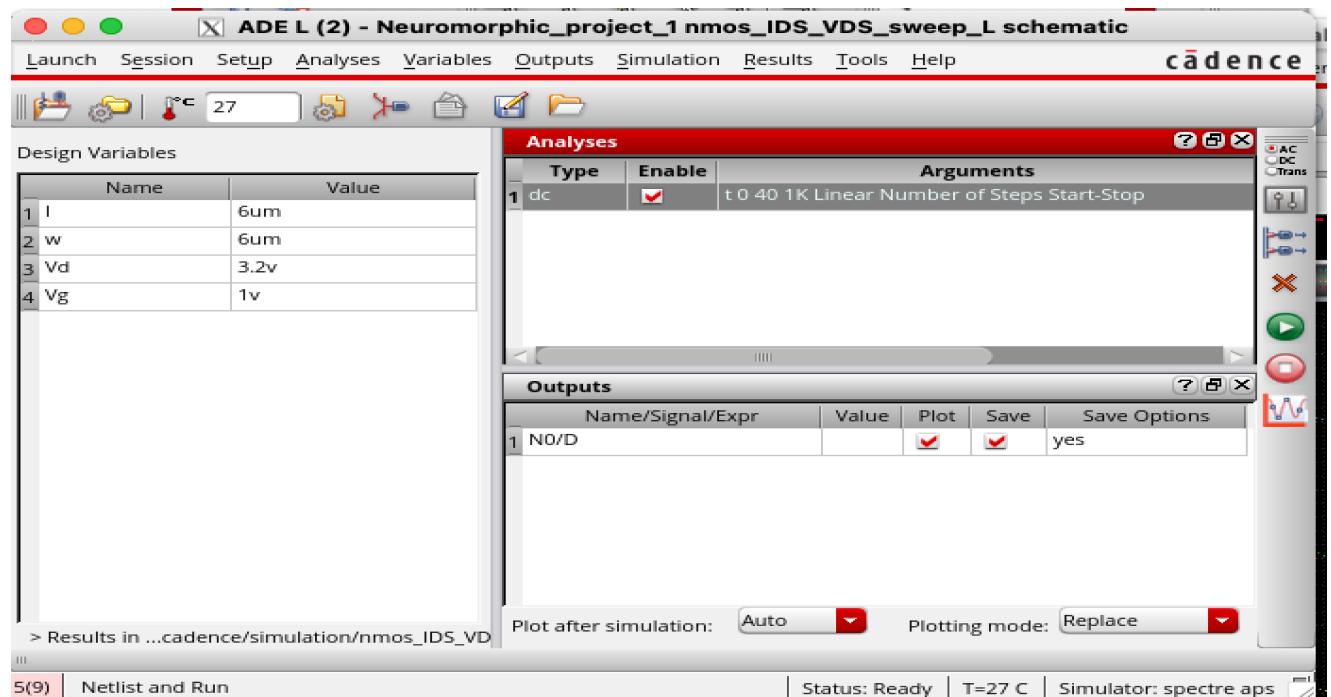


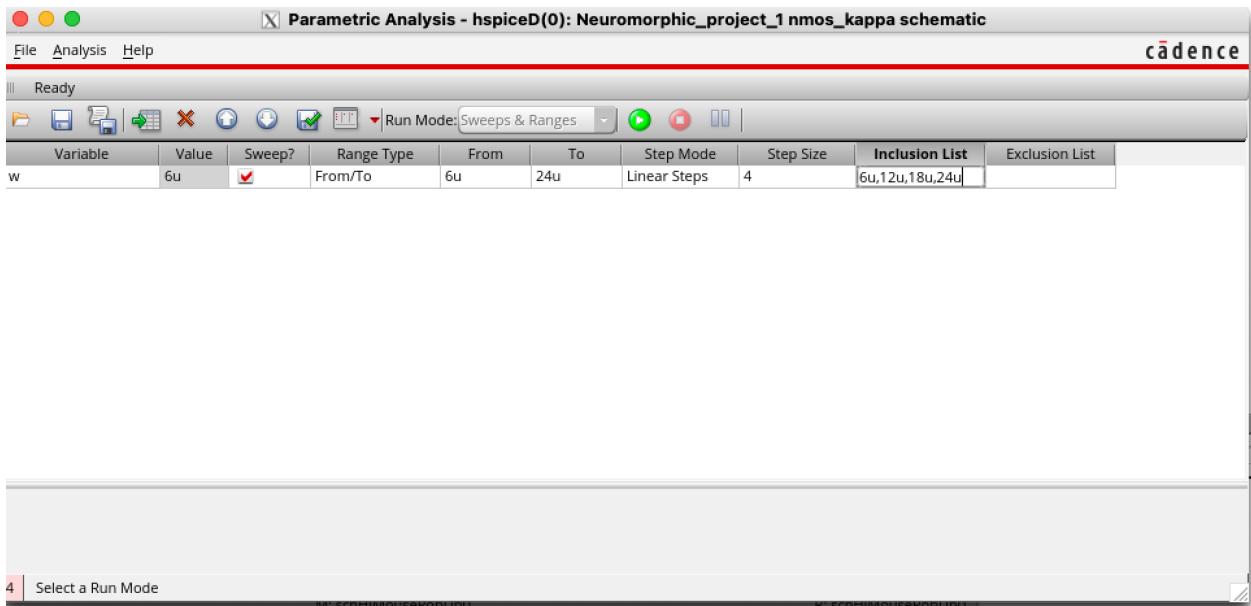
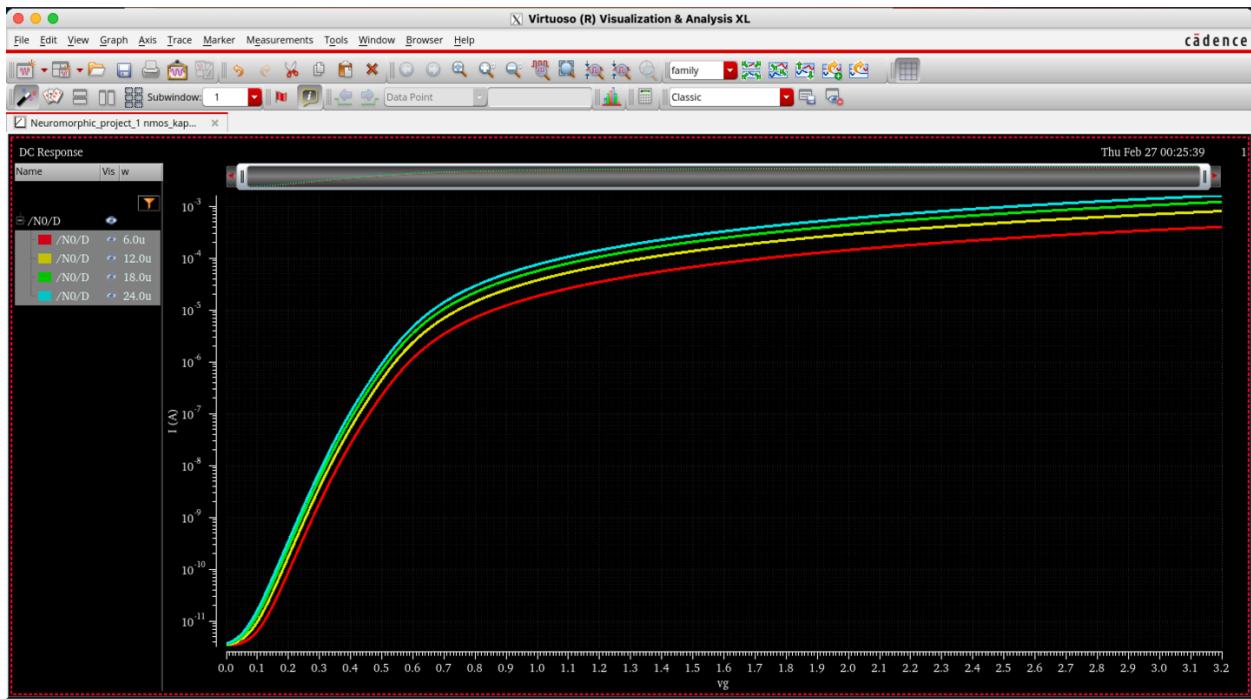
increasing the size of the NMOS transistor results in a higher early voltage applied to the NMOS. In conclusion, the NMOS size while keeping the W/L ratio constant equal to 1 increases the resistance of the given circuit.

- Analysis 2: Extracting kappa, κ in MOS weak inversion (subthreshold):
Designing the schematic setups and performing the required simulations nMOS with $W = [6, 12, 18, 24] \mu\text{m}$ and $L = 6 \mu\text{m}$



DC simulations were performed to extract the drain current





Conducting the analysis, to extract κ :

$$k = \frac{d \ln(I_{ds})}{dV_g} * U_T ; \text{ For } U_T = 26mV$$

MATLAB-based Evaluation:

```
% Extract Voltage (Vg) and Current (Ids)
Vg = data(2:end,1); % Ignoring the first row as mentioned
Ids = data(2:end,2);

% Constants
UT = 26e-3; % Thermal voltage in Volts

% Compute d(ln(Ids))/dVg using numerical differentiation
dlnIds_dVg = diff(log(Ids)) ./ diff(Vg);

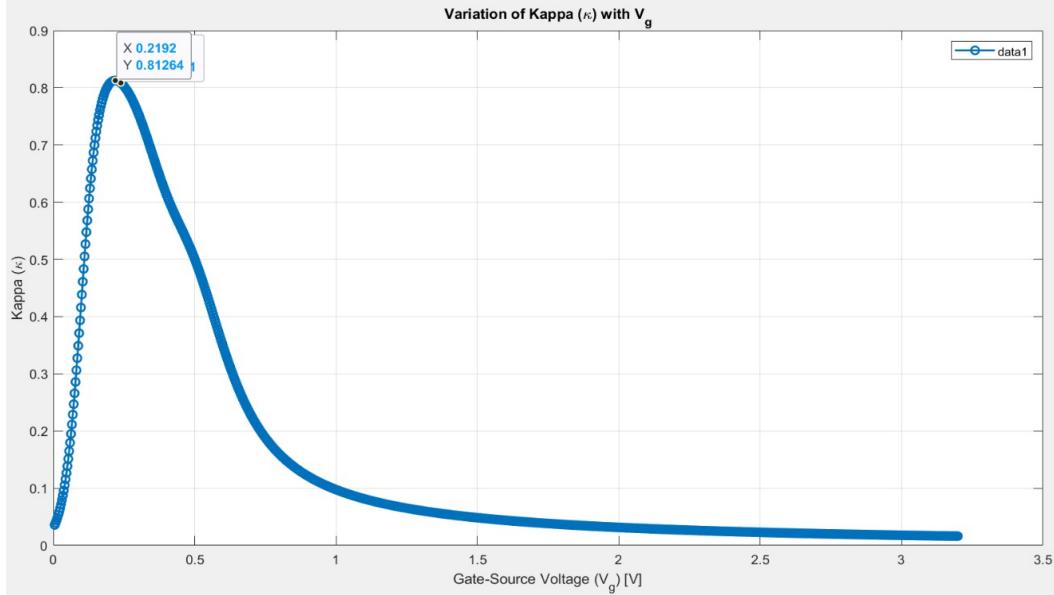
% Compute kappa ( $\kappa$ )
kappa = dlnIds_dVg * UT;

% Compute midpoints for Vg to match dimensions
Vg_mid = (Vg(1:end-1) + Vg(2:end)) / 2;

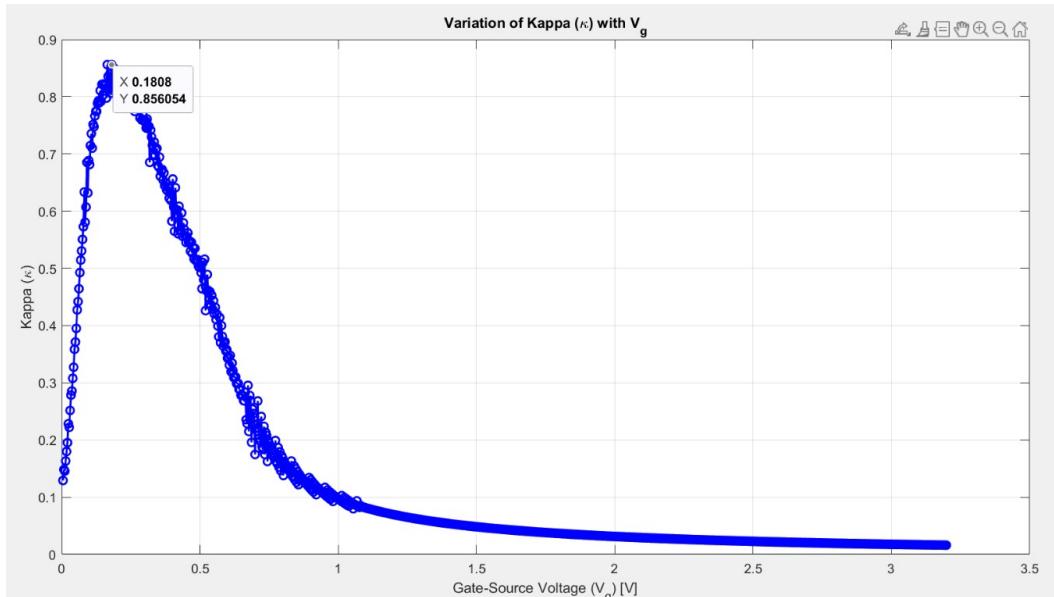
% Plot kappa vs Vg
figure;
plot(Vg_mid, kappa, '-bo', 'LineWidth', 1.5);
xlabel('Gate-Source Voltage (V_g) [V]');
ylabel('Kappa ( $\kappa$ )');
title('Variation of Kappa ( $\kappa$ ) with V_g');
grid on;

% Display kappa values
disp('Computed Kappa values:');
disp(kappa);
```

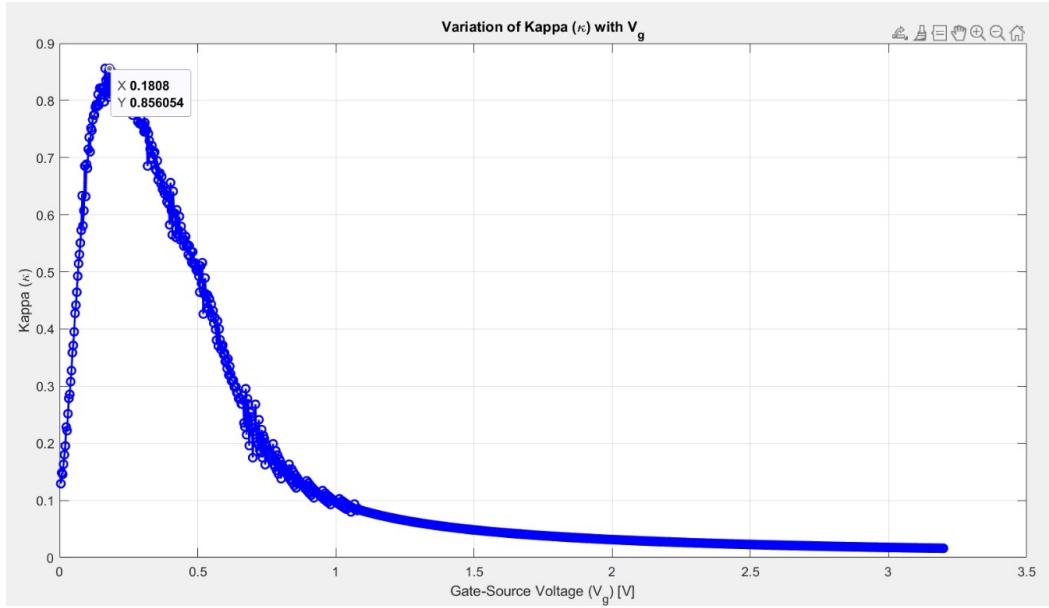
When W=6; L=6;



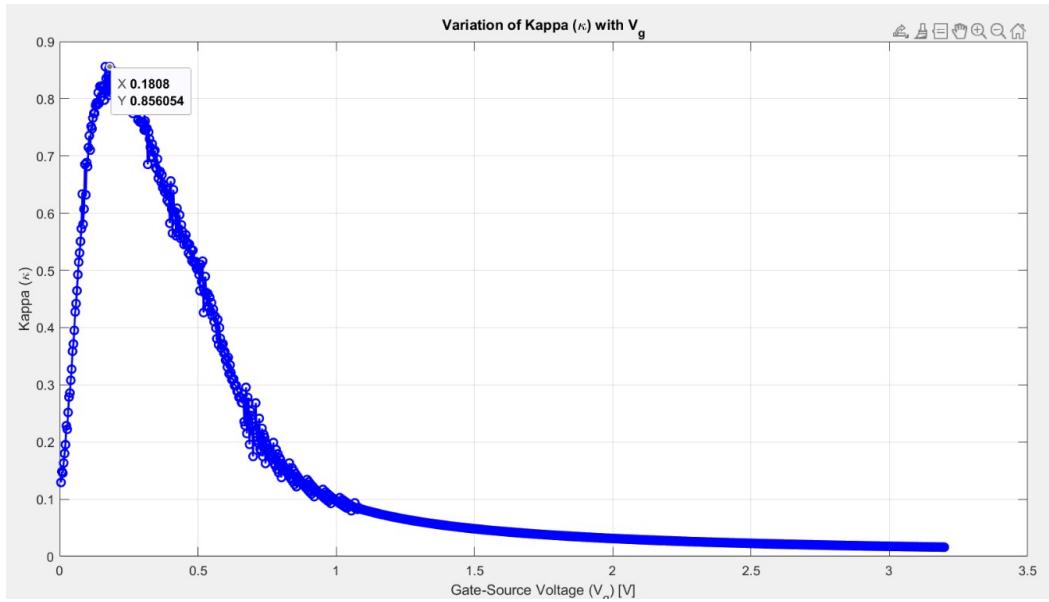
When W=12; L=6;



When W=18; L=6;



When W=24; L=6;



W	MAXIMUM KAPPA
6	0.8126
12	0.8560
18	0.8660
24	0.8720

Kappa value changes as we change the voltage but for maximum kappa value it remains the nearly same even changing the width of NMOS transistor.