

# **Video Processing System Based On Neural Network That Performs The Color Detection**

## **Team Members:**

- Ushasri Badinidi
- Rohini Panikara
- Prasanth Rayudu
- Shaik Shaheed Basha
- Namrata Yadav

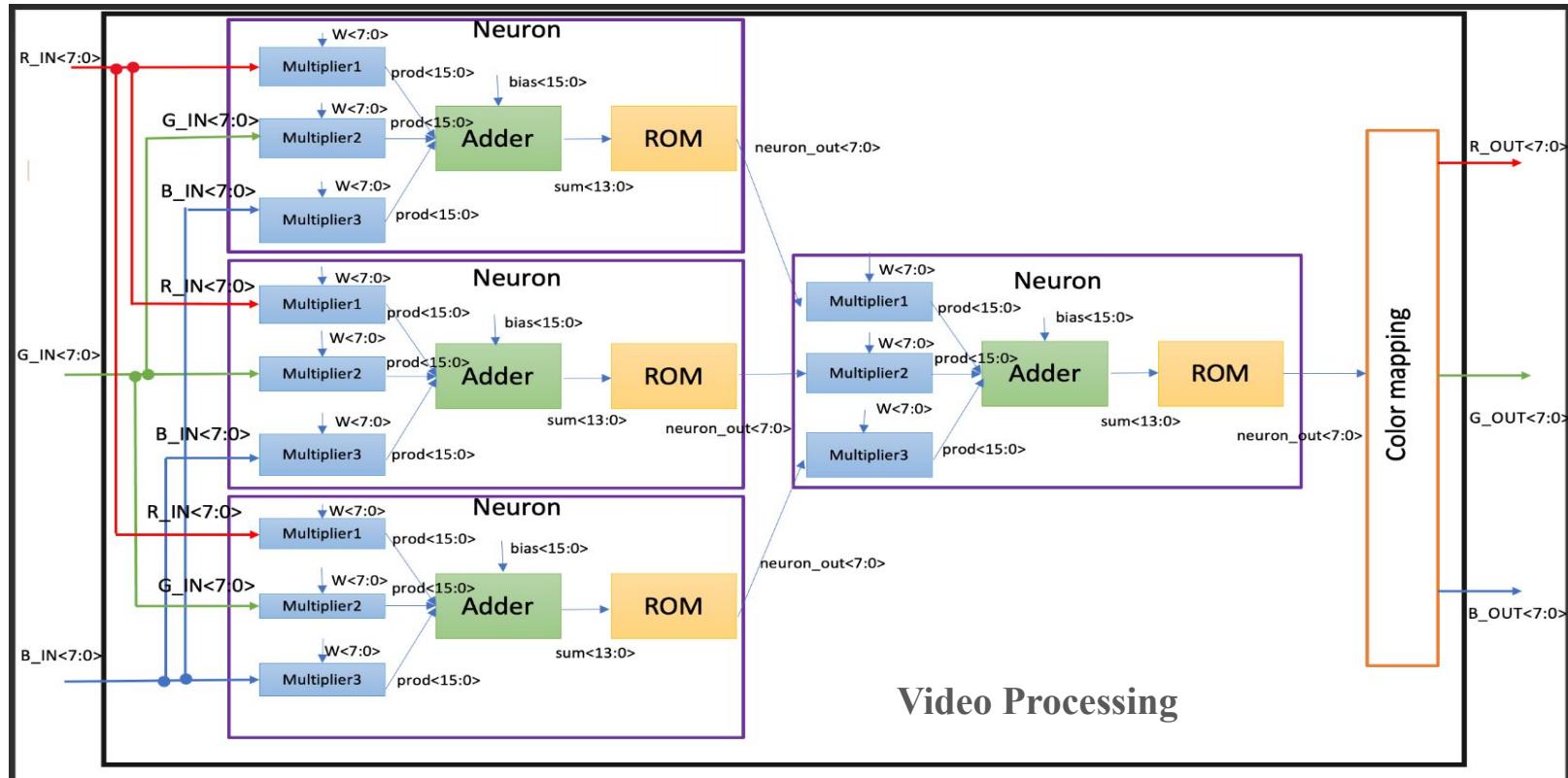
### Project 4 Task Assignment:

Task #	Task Description	Assigned To	Due Date
15	Perform sub-block circuit layout	Ushasri	Nov 14, 2024
16	Perform DRC/LVS at the block level	Namrata	Nov 16, 2024
17	Perform the system layout (integrate all sub-block layouts)	Prasanth	Nov 18, 2024
18	Perform DRC/LVS at the system level	Rohini	Nov 20, 2024
19	Run system use-case with extracted netlist to validate performance	Shaheed	Nov 22, 2024
20	Compare results vs schematic view, comment on performance degradations	Namrata	Nov 24, 2024
21	Prepare the Project 4 group report (PPT)	Shaheed	Nov 28, 2024

# Tasks List

S.No	Task	Status	Contributed by
1	Adder Transistor level Schematic,Validation	Finished	Namrata
2	Multiplier Transistor level Schematic,Validation	Finished	Prashanth
3	Rom Schematic	Finished	Ushasri
4	Color Mapping Block Transistor level Schematic,Validation	Finished	Shaheed
5	Comparing results vs Schematic and View	Finished	Rohini
7	Project 3 report	Finished	Shaheed

# Block Diagram



# Objective:

The primary objective of this project is to design, implement, and validate a high-performance system through the following stages:

1. **Sub-block Circuit Layout:** Create accurate layouts for individual sub-blocks, ensuring adherence to design constraints.
2. **Block-Level Verification:** Perform **Design Rule Checks (DRC)** and **Layout vs. Schematic (LVS)** validation to confirm the accuracy of individual sub-block layouts.
3. **System Integration:** Integrate all sub-block layouts into a cohesive system layout while maintaining design hierarchy and functionality.
4. **System-Level Verification:** Conduct DRC/LVS at the system level to ensure compliance with foundry rules and consistency with the schematic.
5. **Post-Layout Simulation:** Validate system performance by running use-case simulations on the extracted netlist, ensuring tapeout-readiness.
6. **Performance Analysis:** Compare post-layout simulation results with schematic-level results to identify and analyze performance degradations.
7. **Final Specification Review:** Summarize the design's final specifications, highlighting key performance metrics, compliance with design requirements, and any trade-offs.

# Verification and Validation Overview

## **Blocks Under Verification:**

1. Adder Block
2. Multiplier Block
3. Color Mapping Block

## **Verification Tasks Performed:**

1. **Layout Design:**
  - Developed accurate circuit layouts for all blocks following design constraints and foundry rules.
2. **DRC (Design Rule Check):**
  - Ensured all block layouts comply with manufacturing design rules for tapeout readiness.
3. **LVS (Layout vs. Schematic):**
  - Verified that the physical layout matches the intended schematic functionality.

# Adder Schematic

**Adder schematic consists of:**

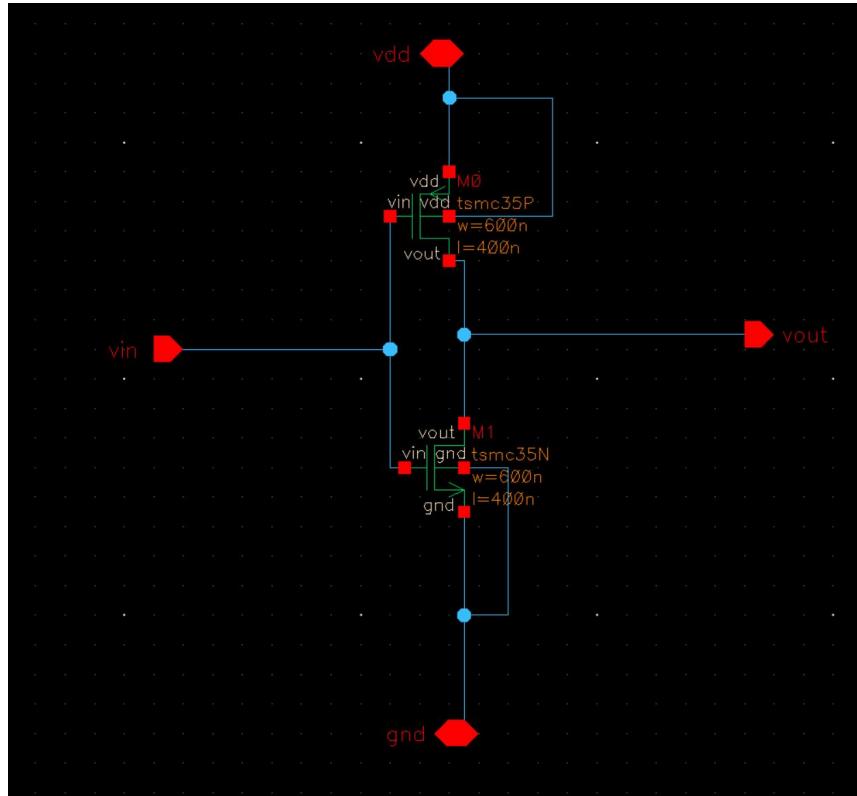
1. AND
2. OR
3. XOR
4. HALF ADDER
5. FULL ADDER
6. ADDER

# Multiplier Schematic

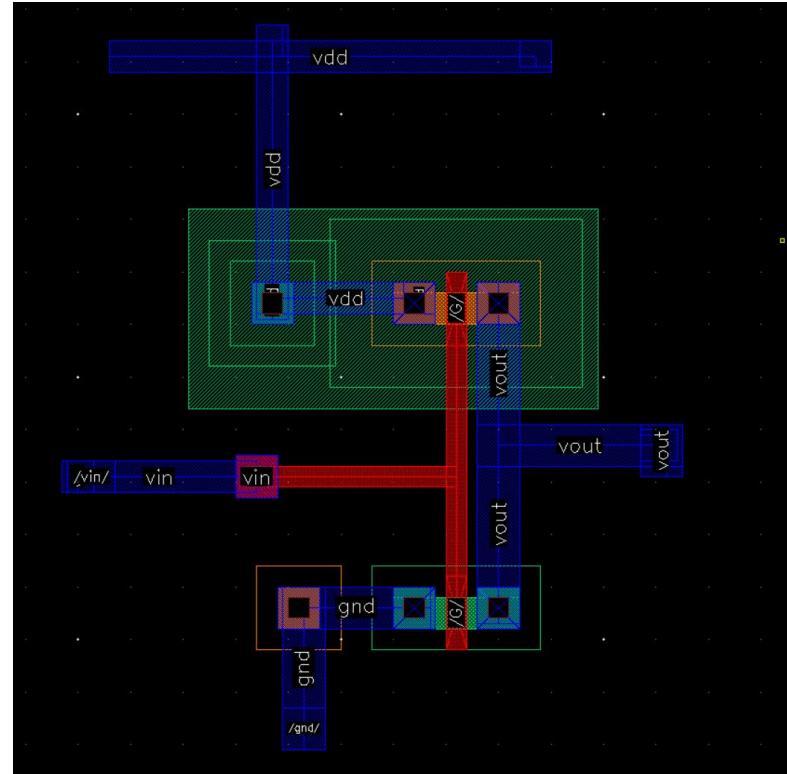
**Multiplier schematic consists of**

1. AND
2. OR
3. XOR
4. Half adder
5. Full adder
6. MUX

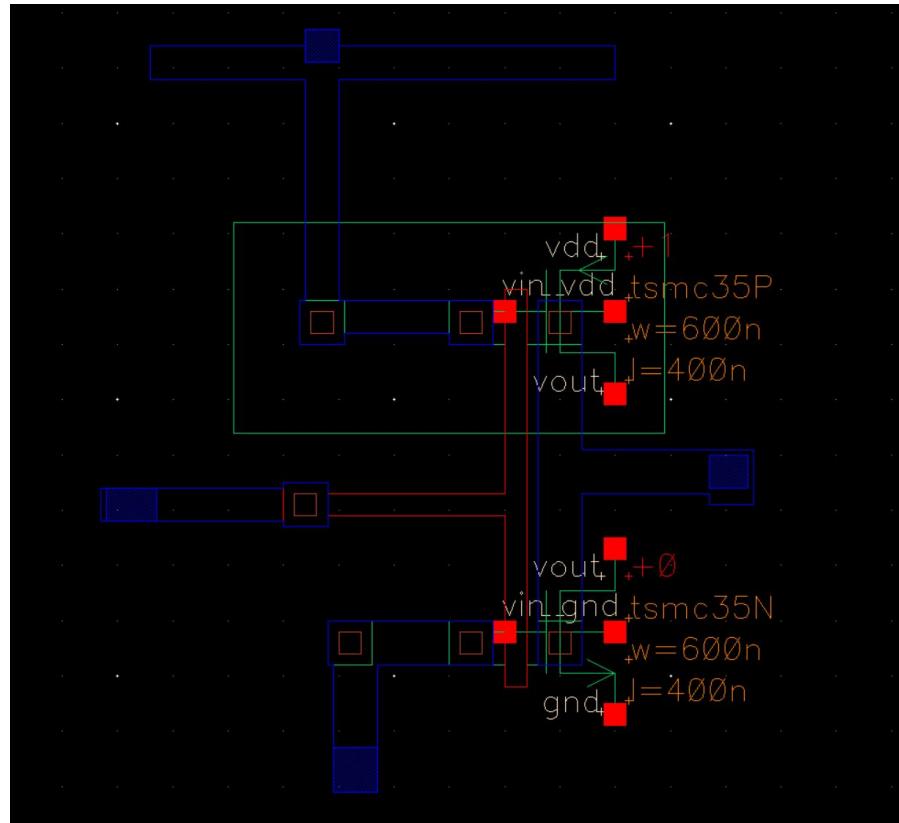
# INVERTER Schematic



# INVERTER LAYOUT



# INVERTER EXTRACTED



# INVERTER VERIFICATION

```

drc(ceEdge (notch < (lambda * 3.0)) errMsg)
executing: drc(ce (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1)))) ...
executing: drc(CapacitorElecEdge ceEdge (enc < (lambda * 3.0)) errMsg)
executing: drc(TransistorElecEdge ceEdge (enc < (lambda * 2.0)) errMsg)
executing: saveDerived(geomAndNot(ce elec) "(SCMOS Rules 13.3,13.4) electrode enclosure of cont...
executing: drc(ceEdge polyEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerived(geomOutside(geomAnd(ce poly) CapacitorElec) errMsg)
executing: drc(ceEdge activeEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerived(geomAnd(ce active) errMsg)
executing: drc(via2Edge (width < (lambda * 2.0)) errMsg)
drc(via2Edge (sep < (lambda * 3.0)) errMsg)
executing: drc(via2 (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1))))...
executing: drc(metal2Edge via2Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerived(geomAndNot(via2 metal12) errMsg)
executing: drc(metal3Edge (width < (lambda * 3.0)) errMsg)
drc(metal3Edge (sep < (lambda * 3.0)) errMsg)
drc(metal3Edge (notch < (lambda * 3.0)) errMsg)
executing: drc(metal3Edge via2Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerived(geomAndNot(via2 metal13) errMsg)
executing: drc(via3Edge (width < (lambda * 2.0)) errMsg)
drc(via3Edge (sep < (lambda * 3.0)) errMsg)
executing: drc(via3 (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1))))...
executing: drc(metal3Edge via3Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerived(geomAndNot(via3 metal13) errMsg)
executing: drc(metal4Edge (width < (lambda * 6.0)) errMsg)
drc(metal4Edge (sep < (lambda * 6.0)) errMsg)
drc(metal4Edge (notch < (lambda * 6.0)) errMsg)
executing: drc(metal4Edge via3Edge (enc < (lambda * 2.0)) errMsg)
executing: saveDerived(geomAndNot(via3 metal14) errMsg)
executing: drc(tactiveEdge (width < (lambda * 4.0)) errMsg)
drc(tactiveEdge (sep < (lambda * 4.0)) errMsg)
drc(tactiveEdge (notch < (lambda * 4.0)) errMsg)
executing: drc(tactiveEdge activeEdge (enc < (lambda * 4.0)) errMsg)
drc(tactiveEdge activeEdge (sep < (lambda * 4.0)) errMsg)
executing: drc(geomAnd(tactive geomAnd(geomOr(nNotOhmic pNotOhmic) poly)) (width < (lambda * 3....
executing: saveDerived(geomStraddle(active tactive) "(SCMOS Rule 24.6) active may not straddle ...
DRC started.....Sun Dec 8 20:16:25 2024
completed ....Sun Dec 8 20:16:25 2024
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "Inverter layout" *****
Total errors found: 0

```

Using terminal names as correspondence points.  
Compiling Diva LVS rules...

Net-list summary for /home/sshaik2680/project/LVS/layout/netlist  
count  
4 nets  
4 terminals  
1 pmos  
1 nmos

Net-list summary for /home/sshaik2680/project/LVS/schematic/netlist  
count  
4 nets  
4 terminals  
1 pmos  
1 nmos

Terminal correspondence points  
N2 N3 gnd  
N0 N2 vdd  
N3 N0 vin  
N1 N1 vout

Devices in the rules but not in the netlist:  
cap nfet pfet nmos4 pmos4

The net-lists match.

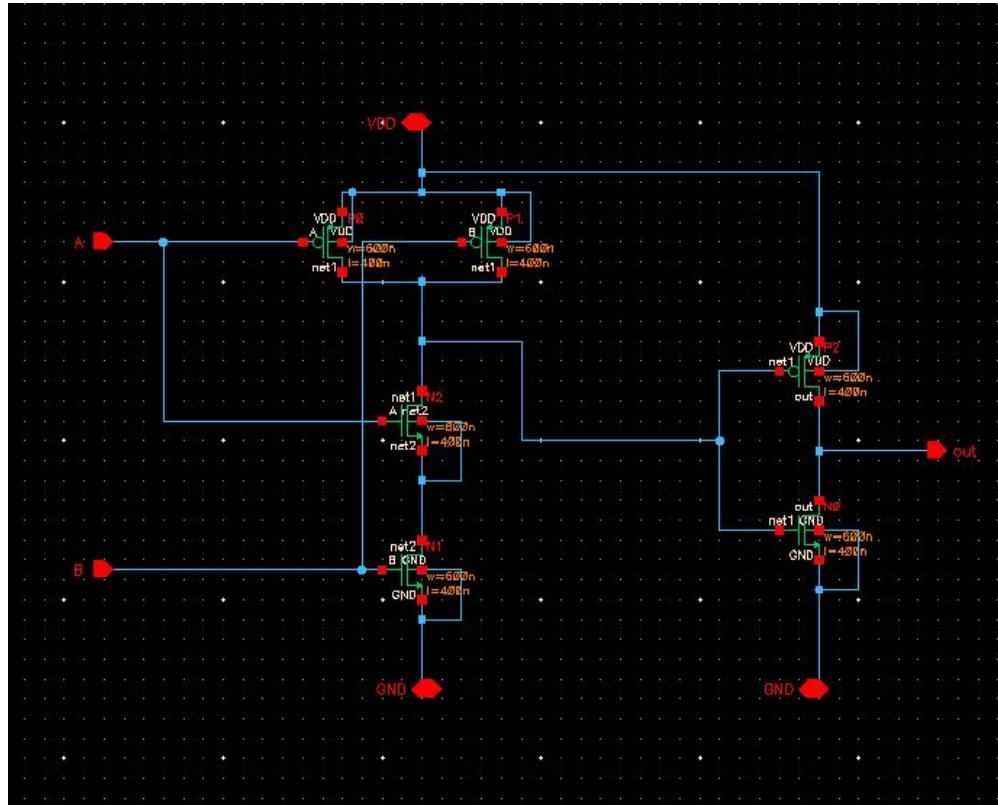
	layout	schematic
	instances	instances
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	2	2
total	2	2

	nets
un-matched	0
merged	0
pruned	0
active	4
total	4

	terminals
un-matched	0
matched but different type	0
total	4

Probe files from /home/sshaik2680/project/LVS/schematic

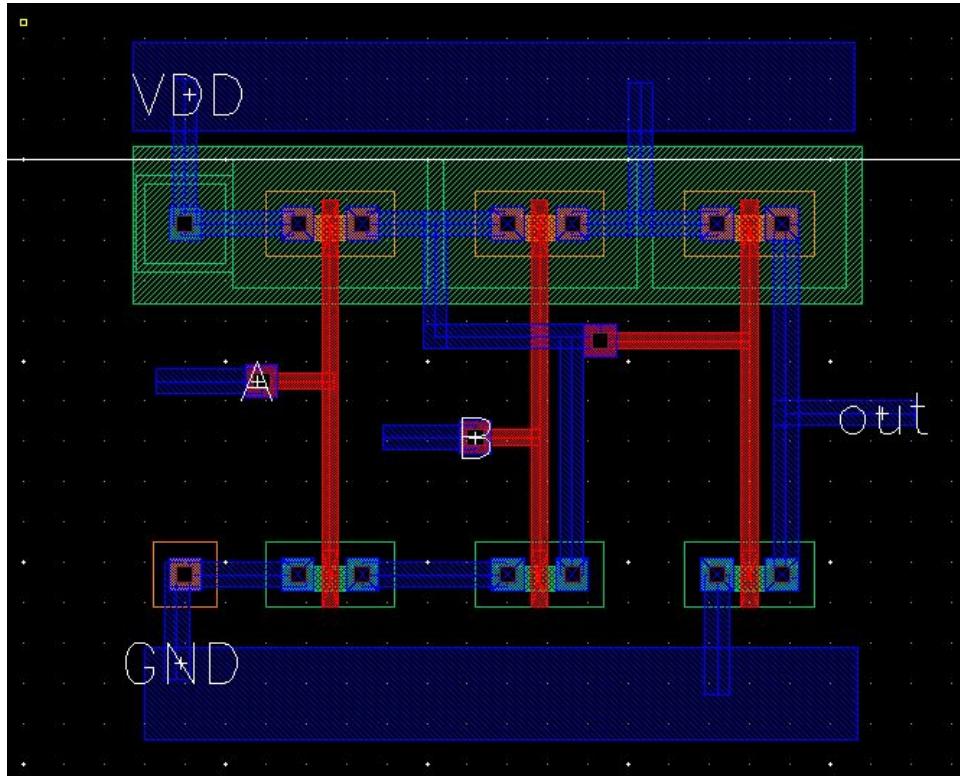
# AND Block Schematic



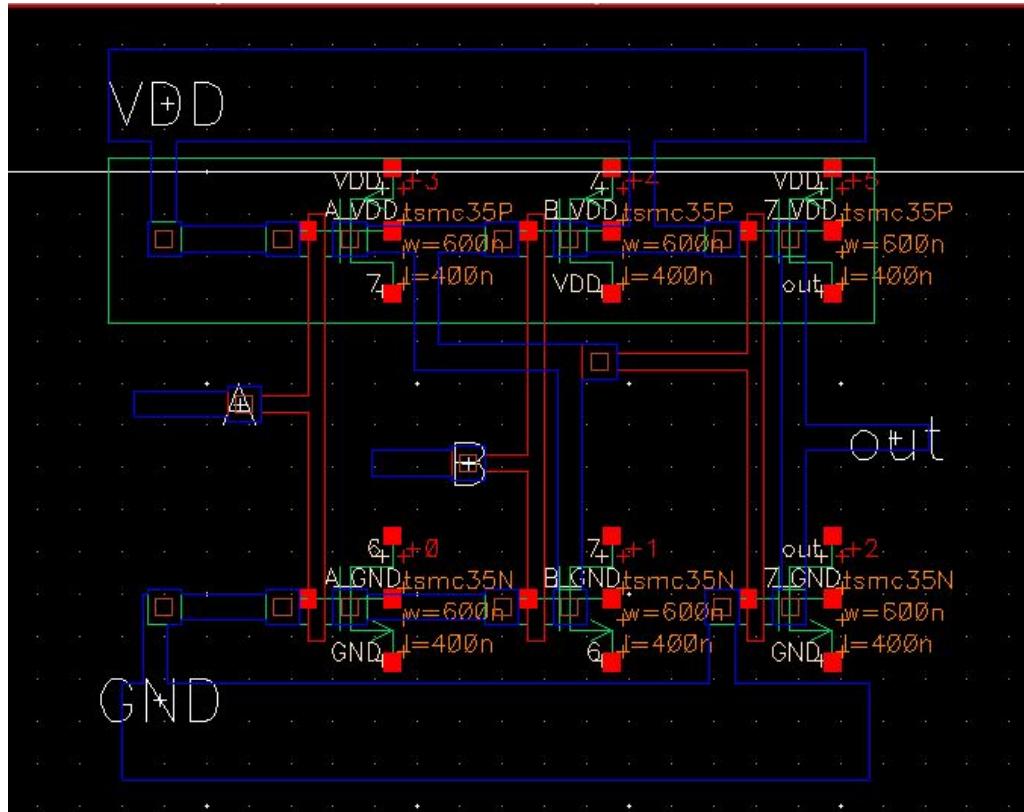
AND Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

# AND LAYOUT



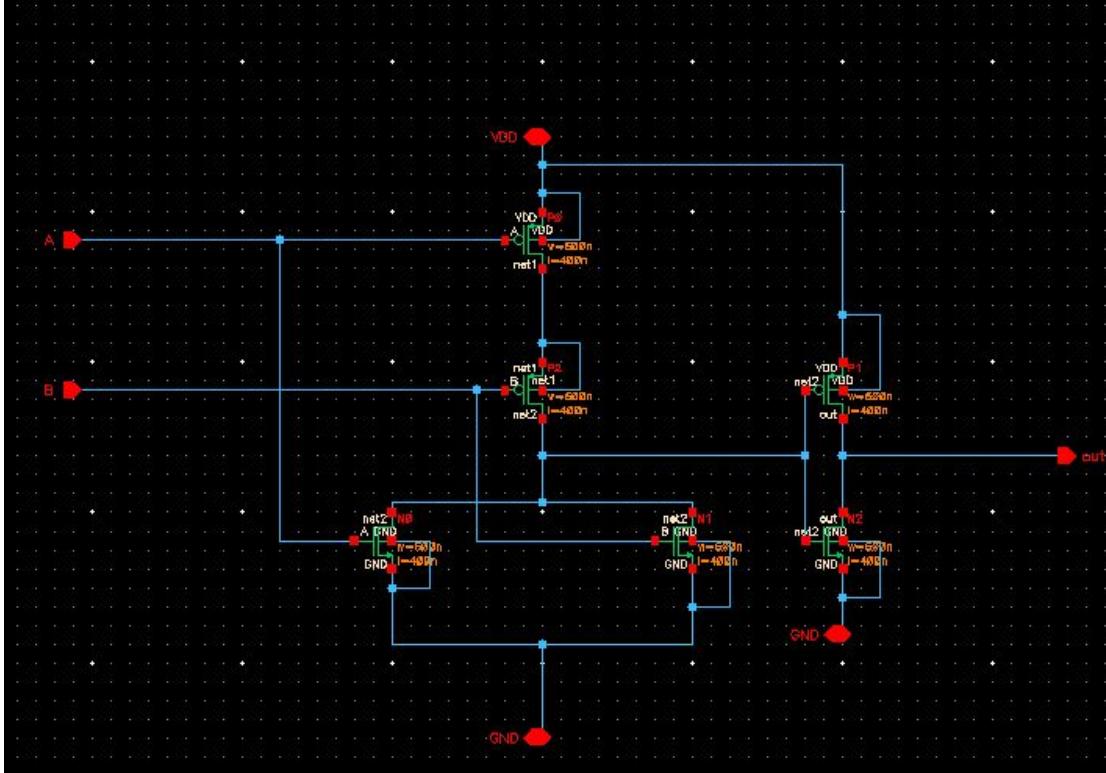
# AND EXTRACTED



# AND VERIFICATION

```
executing: drc(geomGetEdge("elec")) geomGetEdge("metal14") (sep < (lambda * 2.0)) errMsg
executing: saveDerived(geomOverlap(metal14 elec diffnet)) errMsg
executing: drc(geomGetEdge("elec")) geomGetEdge("metal13") (sep < (lambda * 2.0)) errMsg
executing: drc(geomGetEdge("elec")) geomGetEdge("metal12") (sep < (lambda * 2.0)) errMsg
executing: saveDerived(geomOverlap(metal12 elec diffnet)) errMsg
executing: drc(geomGetEdge("elec")) geomGetEdge("metal11") (sep < (lambda * 2.0)) errMsg
executing: saveDerived(geomOverlap(metal11 elec diffnet)) errMsg
executing: drc(transistorElecEdge (width < (lambda * 2.0)) errMsg)
drc(transistorElecEdge (notch < (lambda * 3.0)) errMsg)
executing: drc(transistorElecEdge activeEdge (enc < (lambda * 2.0)) errMsg)
drc(transistorElecEdge activeEdge (sep < (lambda * 1.0)) errMsg)
executing: drc(transistorElecEdge polyEdge (sep < (lambda * 2.0)) errMsg)
drc(transistorElecEdge polyEdge (ovlp < (lambda * 2.0)) errMsg)
executing: drc(transistorElecEdge cpEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerived(geomAnd((transistorElec cp) errMsg))
executing: drc(transistorElecEdge caEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerived(geomAnd((transistorElec ca) errMsg))
executing: drc(cEdge (width < (lambda * 2.0)) errMsg)
drc(cEdge (notch < (lambda * 3.0)) errMsg)
executing: drc(cEdge (sep < (lambda * 3.0)) errMsg)
executing: drc(cEdge (area > ((lambda * 2.0) * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1))) ... )
executing: drc(capacitorElecEdge ceEdge (enc < (lambda * 3.0)) errMsg)
executing: drc(transistorElecEdge ceEdge (enc < (lambda * 2.0)) errMsg)
executing: saveDerived(geomAndNotice elec ("SCMOS Rules 13.3,13.4) electrode enclosure of cont..."))
executing: drc(cEdge polyEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerived(geomAnd((geomAnd(cEdge poly) CapacitorElec) errMsg))
executing: drc(cEdge activeEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerived(geomAnd((active) errMsg))
executing: drc(via2Edge (width < (lambda * 2.0)) errMsg)
drc(via2Edge (sep < (lambda * 3.0)) errMsg)
executing: drc(via2 (area > ((lambda * 2.0) * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1)))...)
executing: drc(via2Edge via2Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerived(geomAndNot(via2 metal12)) errMsg
executing: drc(metal1Edge (width < (lambda * 3.0)) errMsg)
drc(metal1Edge (sep < (lambda * 3.0)) errMsg)
drc(metal1Edge (notch < (lambda * 3.0)) errMsg)
executing: drc(metal1Edge via2Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerived(geomAndNot(via2 metal13)) errMsg
executing: drc(via3Edge (width < (lambda * 2.0)) errMsg)
drc(via3Edge (sep < (lambda * 3.0)) errMsg)
executing: drc(via3 (area > ((lambda * 2.0) * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1)))...)
executing: drc(metal1Edge via3Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerived(geomAndNot(via3 metal13)) errMsg
executing: drc(metal1Edge (width < (lambda * 6.0)) errMsg)
drc(metal1Edge (sep < (lambda * 6.0)) errMsg)
drc(metal1Edge (notch < (lambda * 6.0)) errMsg)
executing: drc(metal1Edge via3Edge (enc < (lambda * 2.0)) errMsg)
executing: saveDerived(geomAndNot(via3 metal14)) errMsg
executing: drc(activeEdge (width < (lambda * 4.0)) errMsg)
drc(activeEdge (sep < (lambda * 4.0)) errMsg)
drc(activeEdge (notch < (lambda * 4.0)) errMsg)
executing: drc(activeEdge activeEdge (enc < (lambda * 4.0)) errMsg)
drc(activeEdge activeEdge (sep < (lambda * 4.0)) errMsg)
executing: drc(geomAnd((active geomAnd(geomOrInNotHmic pNotHmic) poly)) (width < (lambda * 3....)
executing: saveDerived(geomStraddle(active inactive) "(SCMOS Rule 24.6) active may not straddle ...")
DRC started.....Sun Dec 8 18:27:55 2024
completed ....Sun Dec 8 18:27:55 2024
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "AND layout" *****
Total errors found: 0
```

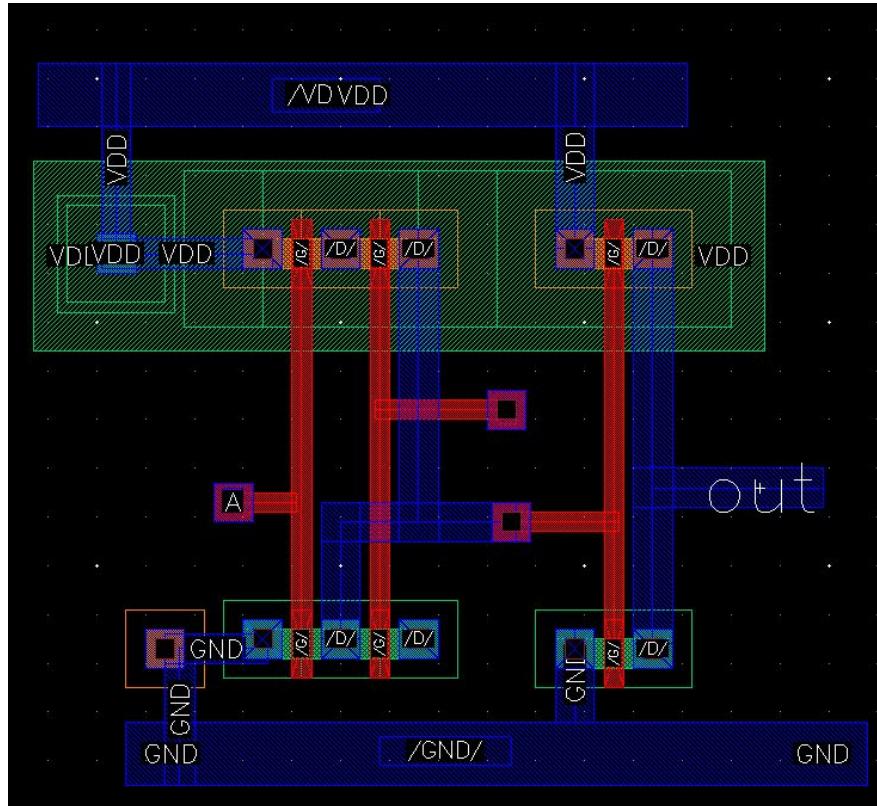
# OR Schematic



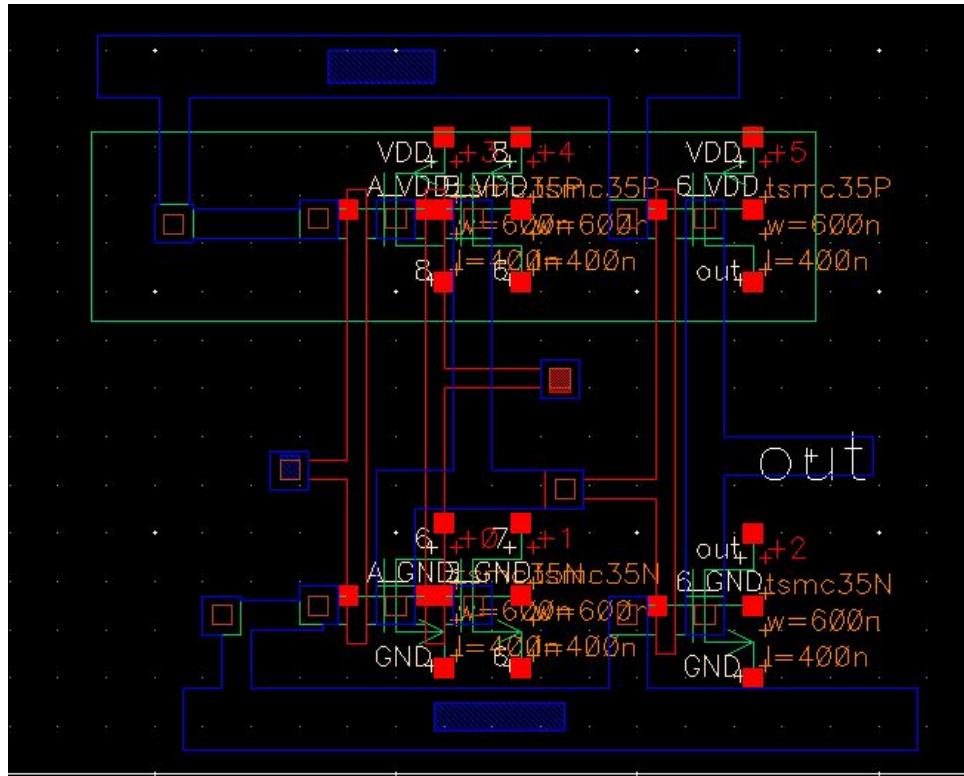
OR Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

# OR LAYOUT



# OR EXTRACTED



# OR VERIFICATION

```

executing: drc(geomGetEdge("elec")) geomGetEdge("metal4") (sep < (lambda * 2.0)) errMsg
executing: saveDerived(geomOverlap(metal4 elec diffNet) errMsg)
executing: drc(geomGetEdge("elec")) geomGetEdge("metal3") (sep < (lambda * 2.0)) errMsg
executing: saveDerived(geomOverlap(metal3 elec diffNet) errMsg)
executing: drc(geomGetEdge("elec")) geomGetEdge("metal2") (sep < (lambda * 2.0)) errMsg
executing: saveDerived(geomOverlap(metal2 elec diffNet) errMsg)
executing: drc(geomGetEdge("elec")) geomGetEdge("metal1") (sep < (lambda * 2.0)) errMsg
executing: saveDerived(geomOverlap(metal1 elec diffNet) errMsg)
executing: drc(TtransistorForLecEdge (width < (lambda * 2.0)) errMsg)
executing: drc(TtransistorForLecEdge (sep < (lambda * 3.0)) errMsg)
executing: drc(TtransistorForLecEdge (notch < (lambda * 3.0)) errMsg)
executing: drc(TtransistorForLecEdge activeEdge (enc < (lambda * 2.0)) errMsg)
executing: drc(TtransistorForLecEdge activeEdge (sep < (lambda * 1.0)) errMsg)
executing: drc(TtransistorForLecEdge polyEdge (sep < (lambda * 2.0)) errMsg)
executing: drc(TtransistorForLecEdge polyEdge (wp < (lambda * 2.0)) errMsg)
executing: drc(TtransistorForLecEdge cpEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerived(geomAndNot(ccelec cp) errMsg)
executing: drc(TtransistorForLecEdge caEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerived(geomAndNot(TransistorElec ca) errMsg)
executing: drc(cEdge (width < (lambda * 2.0)) errMsg)
executing: drc(cEdge (sep < (lambda * 3.0)) errMsg)
executing: drc(cEdge (notch < (lambda * 3.0)) errMsg)
executing: drc((cce (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1)))) ...))
executing: drc(Capacitor cEdge cEdge (enc < (lambda * 3.0)) errMsg)
executing: drc(TtransistorForLecEdge (enc < (lambda * 2.0)) errMsg)
executing: saveDerived(geomAndNot(cc elec) "SCMOS Rule 13.3,13.4) electrode enclosure of cont...
executing: drc(ccePolyEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerived(geomOutside(geomAndNot(cce poly)) CapacitorElec) errMsg
executing: drc(cceEdge activeEdge (sep < (lambda * 3.0)) errMsg)
executing: drc(viaEdge width (sep < (lambda * 2.0)) errMsg)
executing: drc(viaEdge (width < (lambda * 2.0)) errMsg)
executing: drc(viaEdge (sep < (lambda * 3.0)) errMsg)
executing: drc(via2Edge (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1)))) ...))
executing: drc(metal2Edge via2Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerived(geomAndNot(via2 metal2) errMsg)
executing: drc(metal3Edge (width < (lambda * 3.0)) errMsg)
executing: drc(metal3Edge (sep < (lambda * 3.0)) errMsg)
executing: drc(metal3Edge (notch < (lambda * 3.0)) errMsg)
executing: drc(metal3Edge via2Edge (enc < (lambda * 4.0)) errMsg)
executing: saveDerived(geomAndNot(via2 metal3) errMsg)
executing: drc(via3Edge (width < (lambda * 2.0)) errMsg)
executing: drc(via3Edge (sep < (lambda * 3.0)) errMsg)
executing: drc(via3Edge (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1)))) ...))
executing: drc(metal3Edge via3Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerived(geomAndNot(via3 metal3) errMsg)
executing: drc(metal4Edge (width < (lambda * 3.0)) errMsg)
executing: drc(metal4Edge (sep < (lambda * 6.0)) errMsg)
executing: drc(metal4Edge via3Edge (enc < (lambda * 2.0)) errMsg)
executing: saveDerived(geomAndNot(via3 metal4) errMsg)
executing: drc(tactiveEdge (width < (lambda * 4.0)) errMsg)
executing: drc(tactiveEdge (sep < (lambda * 4.0)) errMsg)
executing: drc(tactiveEdge activeEdge (enc < (lambda * 4.0)) errMsg)
executing: drc(tactiveEdge activeEdge (sep < (lambda * 4.0)) errMsg)
executing: drc(geomAndTactive geomOr(nhotOmic photOmic) poly)) (width < (lambda * 3.0)) ...
executing: saveDerived(geomStraddle(tactive tactive) "(SCMOS Rule 24.6) active may not straddle ...
DRC started.....Sun Dec 8 18:32:04 2024
completed ...Sun Dec 8 18:32:04 2024
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "OR layout" *****
Total errors found: 0

```

## Terminal correspondence points

N5	N0	A
N4	N1	B
N3	N4	GND
N6	N3	VDD
N2	N2	Y

## Devices in the netlist but not in the rules:

pcapacitor

## Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

## The net-lists match.

layout	schematic
instances	

un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	6	6
total	6	6

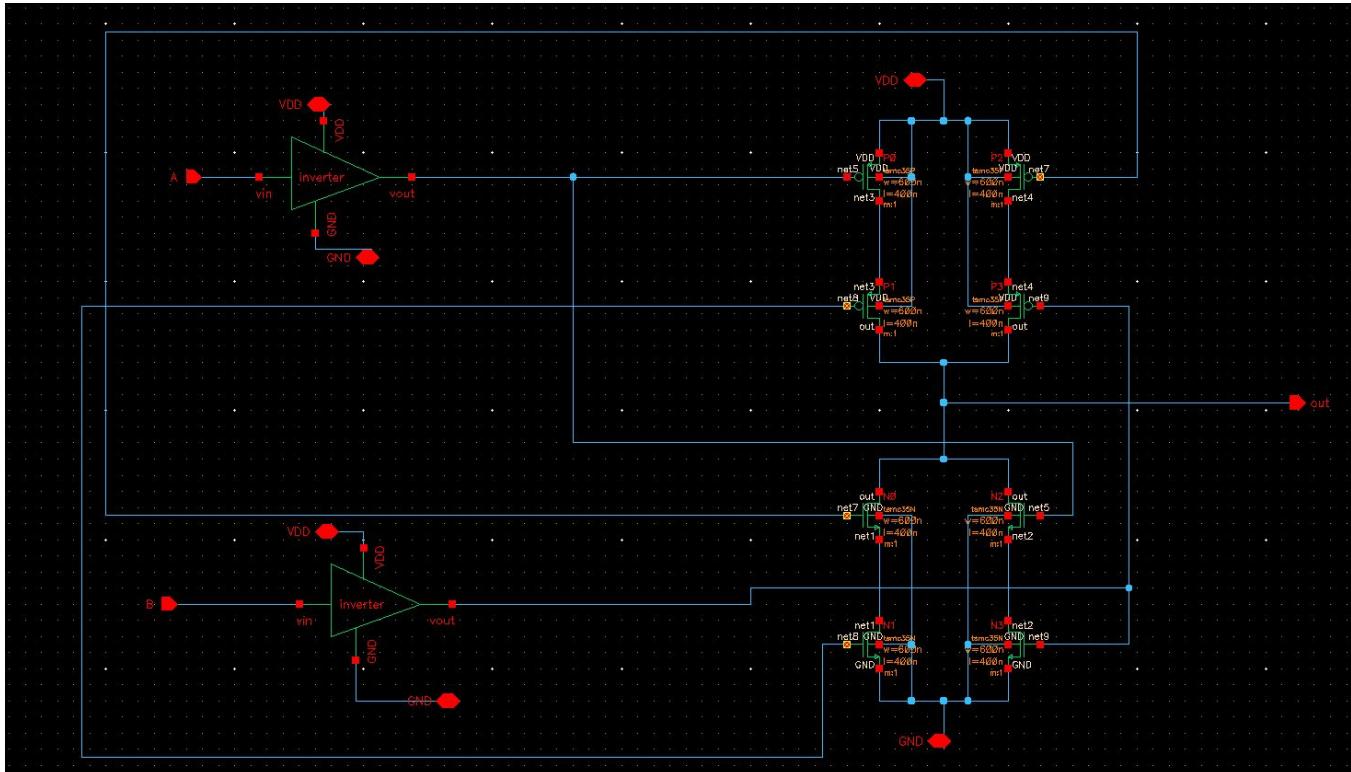
## nets

un-matched	0	0
merged	0	0
pruned	0	0
active	7	7
total	7	7

## terminals

un-matched	0	0
matched but different type	0	0
total	5	5

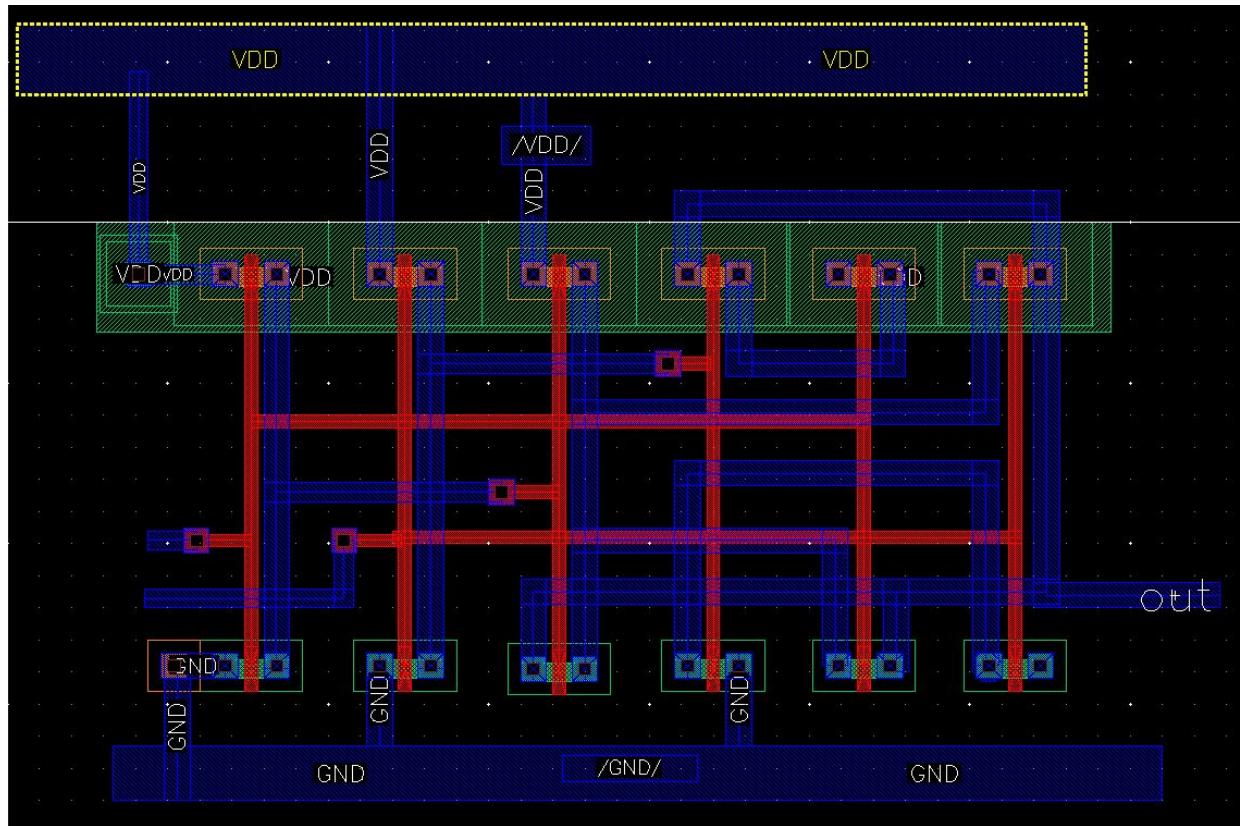
# XOR Schematic



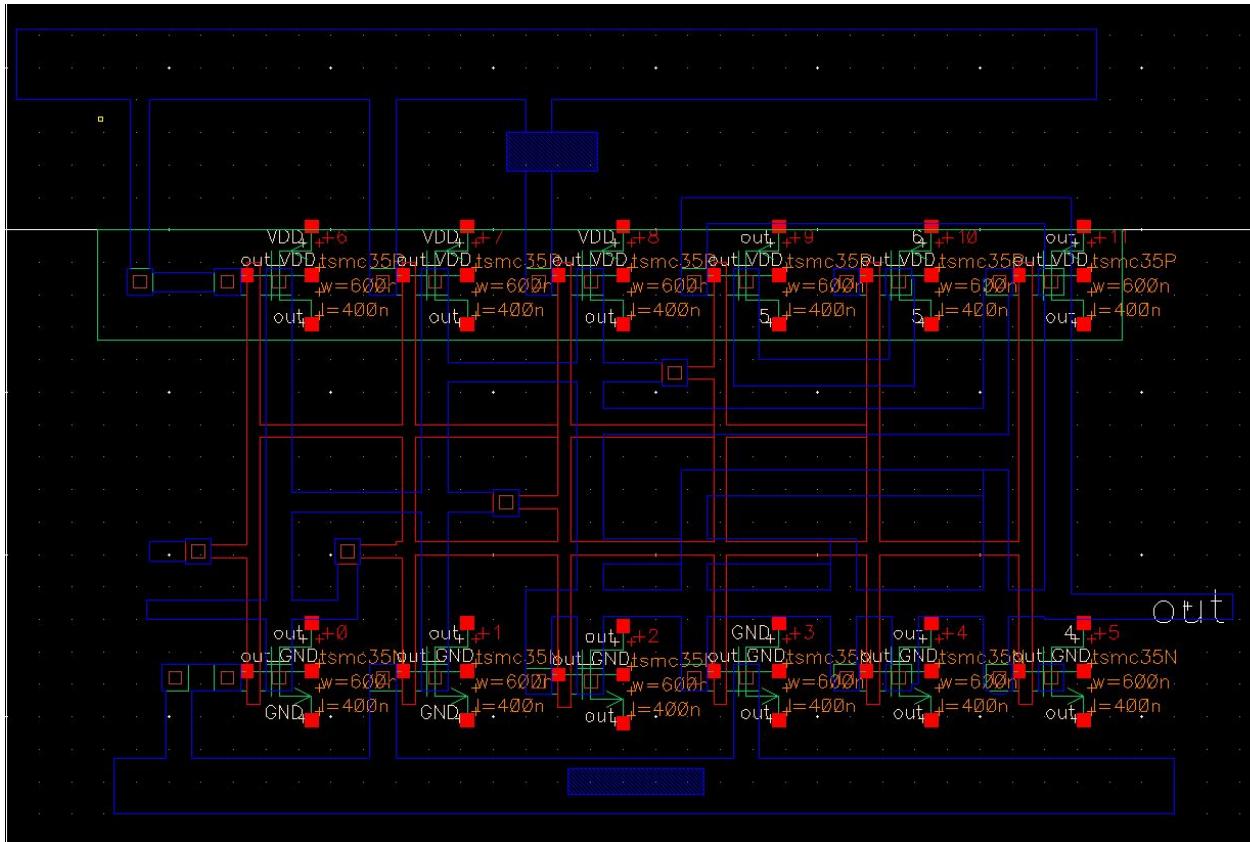
XOR Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

# XOR LAYOUT



# XOR EXTRACTED

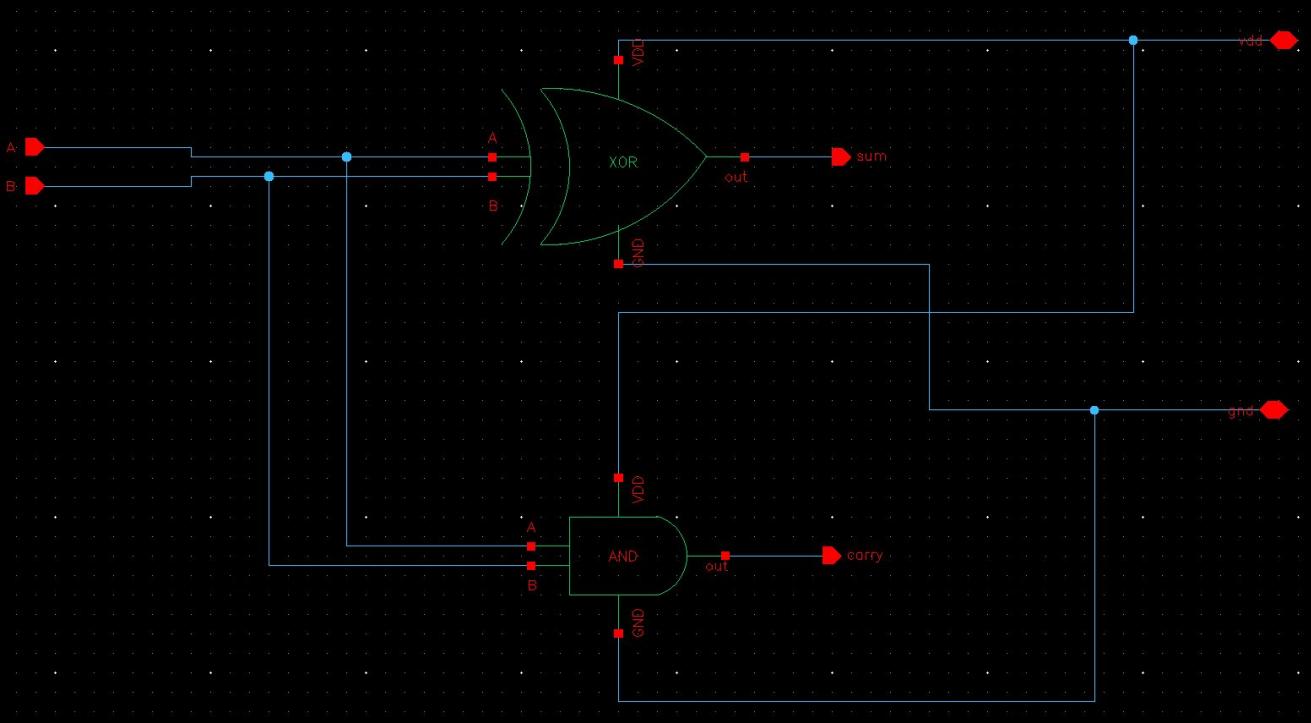


# XOR VERIFICATION

---

```
executing: drc(geomGetEdge("elec") geomGetEdge("metal14") (sep < (lambda * 2.0)) errMsg)
executing: saveDerivedGeomOverlap(metal4 elec diffNet) errMsg
executing: drc(geomGetEdge("elec") geomGetEdge("metal13") (sep < (lambda * 2.0)) errMsg)
executing: saveDerivedGeomOverlap(metal3 elec diffNet) errMsg
executing: drc(geomGetEdge("elec") geomGetEdge("metal12") (sep < (lambda * 2.0)) errMsg)
executing: saveDerivedGeomOverlap(metal2 elec diffNet) errMsg
executing: drc(geomGetEdge("elec") geomGetEdge("metal11") (sep < (lambda * 2.0)) errMsg)
executing: saveDerivedGeomOverlap(metal1 elec diffNet) errMsg
executing: drc(TransistorElecEdge (width < (lambda * 3.0)) errMsg)
executing: drc(TransistorElecEdge (notch < (lambda * 3.0)) errMsg)
executing: drc(TransistorElecEdge activeEdge (enc < (lambda * 2.0)) errMsg)
executing: drc(TransistorElecEdge activeEdge (sep < (lambda * 1.0)) errMsg)
executing: drc(TransistorElecEdge polyEdge (sep < (lambda * 2.0)) errMsg)
executing: drc(TransistorElecEdge polyEdge (oval < (lambda * 2.0)) errMsg)
executing: drc(TransistorElecEdge cpEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerivedGeomAnd(TransistorElec cp) errMsg
executing: drc(TransistorElecEdge caEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerivedGeomAnd(TransistorElec ca) errMsg
executing: drc(cEEdge (width < (lambda * 2.0)) errMsg)
executing: drc(cEEdge (sep < (lambda * 3.0)) errMsg)
executing: drc(cEEdge (notch < (lambda * 3.0)) errMsg)
executing: drc(cEEdge (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1)))) ...
executing: drc(CapacitorElecEdge ceEdge (enc < (lambda * 3.0)) errMsg)
executing: drc(TransistorElecEdge ceEdge (enc < (lambda * 2.0)) errMsg)
executing: saveDerivedGeomAndNot(ce elec) "(SCMOS Rules 13.3,13.4) electrode enclosure of cont...
executing: drc(cEEdge polyEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerivedGeomOutside(geomAndNotce poly) CapacitorElec) errMsg
executing: drc(cEEdge activeEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerivedGeomAnd(ce active) errMsg
executing: drc(via2Edge (width < (lambda * 2.0)) errMsg)
executing: drc(via2Edge (sep < (lambda * 3.0)) errMsg)
executing: drc(via2Edge (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1))))...
executing: drc(via2Edge via2Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerivedGeomAndNot(via2 metal2) errMsg
executing: drc(metal2Edge (width < (lambda * 3.0)) errMsg)
executing: drc(metal2Edge (sep < (lambda * 3.0)) errMsg)
executing: drc(metal2Edge (notch < (lambda * 3.0)) errMsg)
executing: drc(metal2Edge via2Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerivedGeomAndNot(via2 metal3) errMsg
executing: drc(via3Edge (width < (lambda * 2.0)) errMsg)
executing: drc(via3Edge (sep < (lambda * 3.0)) errMsg)
executing: drc(via3Edge (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1))))...
executing: drc(via3Edge via3Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerivedGeomAndNot(via3 metal3) errMsg
executing: drc(metal4Edge (width < (lambda * 6.0)) errMsg)
executing: drc(metal4Edge (sep < (lambda * 6.0)) errMsg)
executing: drc(metal4Edge (notch < (lambda * 6.0)) errMsg)
executing: drc(metal4Edge via3Edge (enc < (lambda * 2.0)) errMsg)
executing: saveDerivedGeomAndNot(via3 metal4) errMsg
executing: drc(activeEdge (width < (lambda * 4.0)) errMsg)
executing: drc(activeEdge (sep < (lambda * 4.0)) errMsg)
executing: drc(activeEdge (notch < (lambda * 4.0)) errMsg)
executing: drc(activeEdge activeEdge (enc < (lambda * 4.0)) errMsg)
executing: drc(activeEdge activeEdge (sep < (lambda * 4.0)) errMsg)
executing: drc(geomAnd(tactive geomAnd(geomOr(notOhmic pNotOhmic) poly)) (width < (lambda * 3....)
executing: saveDerivedGeomStraddle(active tactive) "(SCMOS Rule 24.6) active may not straddle ...
DRC started.....Sun Dec 8 18:36:12 2024
completed.....Sun Dec 8 18:36:12 2024
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "XOR layout" *****
Total errors found: 0
```

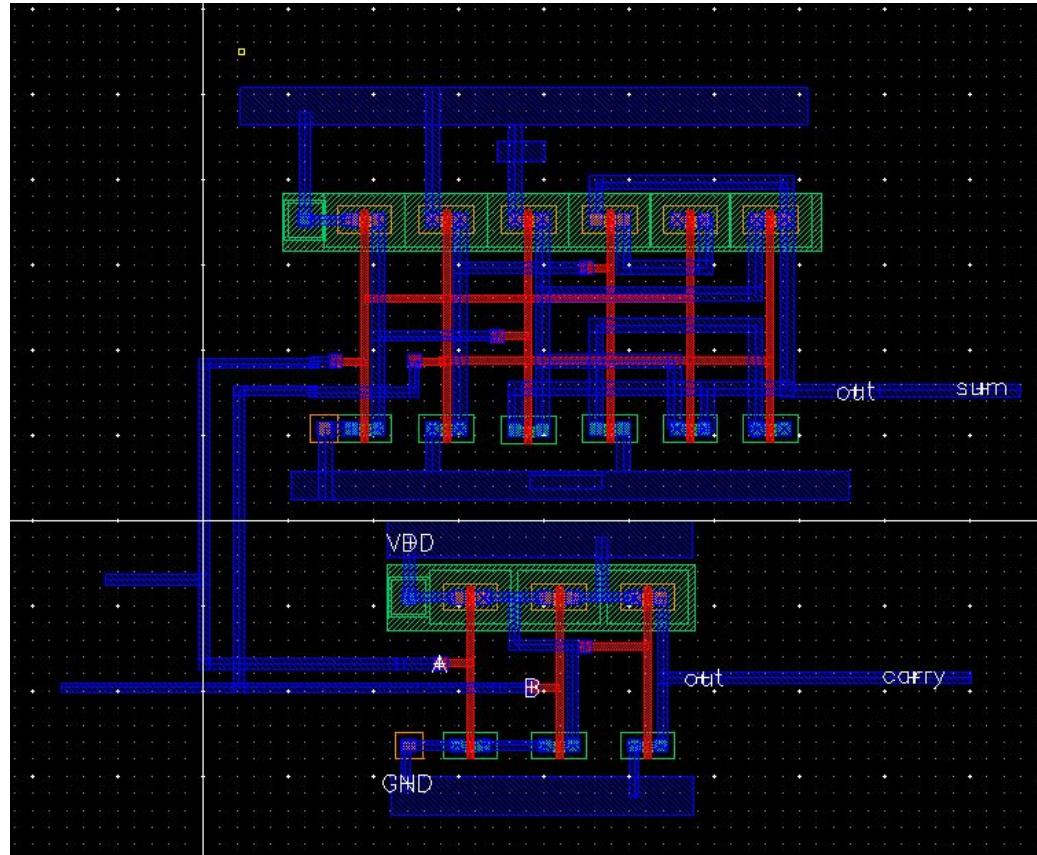
# HALF ADDER Schematic



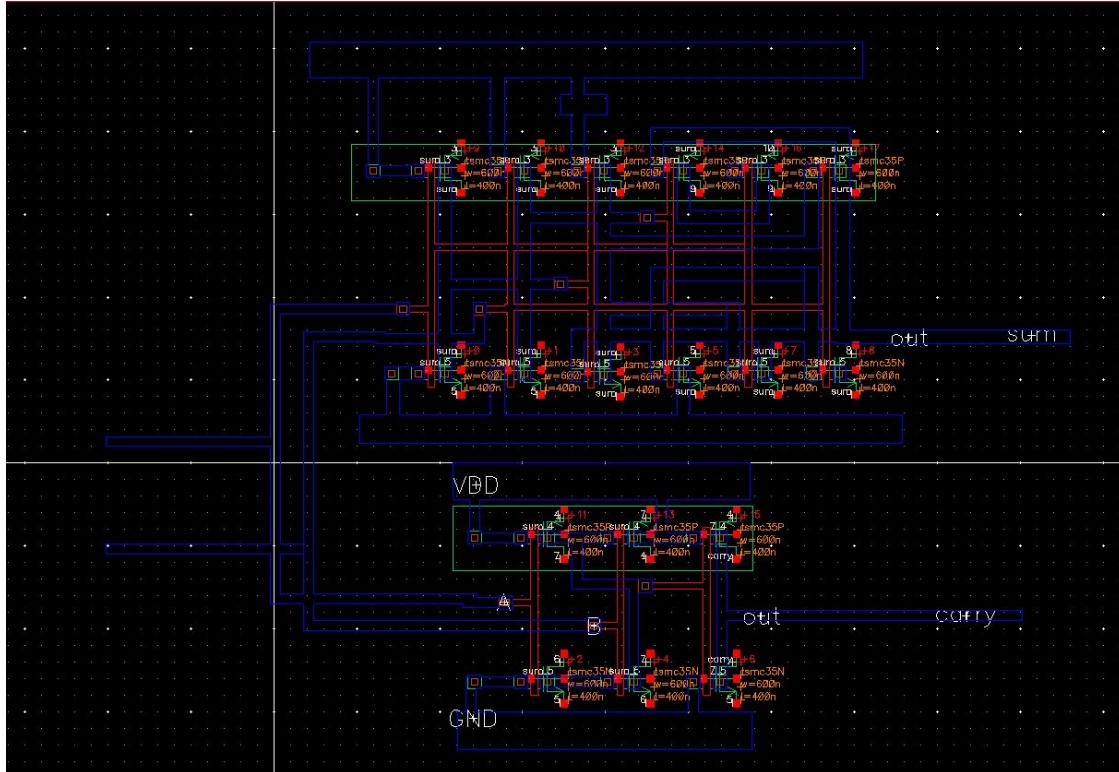
Half Adder

A	B	C Out	Sum
0	0	0	0
1	0	0	1
0	1	0	1
1	1	1	0

# HALF ADDER LAYOUT



# HALF ADDER EXTRACTED



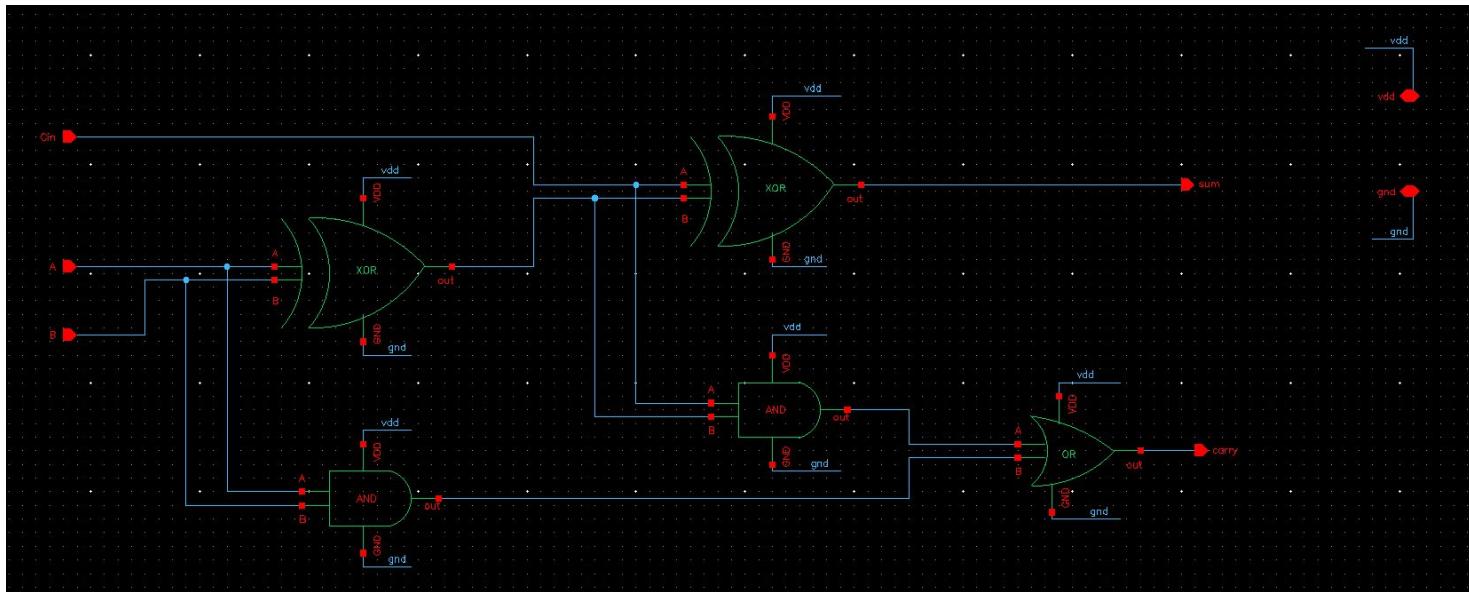
# HALF ADDER VERIFICATION

```

executing: drc|geomGetEdge("elec") geomGetEdge("metal1") (sep < (lambda * 2.0)) errMsg)
executing: saveDerived(geomOverlap|metal14 elec diffNet) errMsg)
executing: drc|geomGetEdge("elec") geomGetEdge("metal3") (sep < (lambda * 2.0)) errMsg)
executing: saveDerived(geomOverlap|metal13 elec diffNet) errMsg)
executing: drc|geomGetEdge("elec") geomGetEdge("metal2") (sep < (lambda * 2.0)) errMsg)
executing: saveDerived(geomOverlap|metal12 elec diffNet) errMsg)
executing: drc|geomGetEdge("elec") geomGetEdge("metal1") (sep < (lambda * 2.0)) errMsg)
executing: saveDerived(geomOverlap|metal1 elec diffNet) errMsg)
executing: drc|TransistorElecEdge width (< (lambda * 2.0)) errMsg)
drc|TransistorElecEdge sep (< (lambda * 3.0)) errMsg)
drc|TransistorElecEdge (width < (lambda * 3.0)) errMsg)
executing: drc|TransistorElecEdge activeEdge (enc < (lambda * 2.0)) errMsg)
drc|TransistorElecEdge activeEdge (sep < (lambda * 1.0)) errMsg)
executing: drc|TransistorElecEdge polyEdge (sep < (lambda * 2.0)) errMsg)
drc|TransistorElecEdge polyEdge (ovlp < (lambda * 2.0)) errMsg)
executing: drc|TransistorElecEdge cpEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerived(geomAnd|TransistorElec cp) errMsg)
executing: drc|TransistorElecEdge caEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerived(geomAnd|TransistorElec ca) errMsg)
executing: drc|eEdge (width < (lambda * 2.0)) errMsg)
executing: drc|eEdge (sep < (lambda * 3.0)) errMsg)
executing: drc|eEdge (notch < (lambda * 3.0)) errMsg)
executing: drc|ice (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1))) ...))
executing: drc|CapacitorElecEdge ceEdge (enc < (lambda * 3.0)) errMsg)
executing: drc|TransistorElecEdge ceEdge (enc < (lambda * 2.0)) errMsg)
executing: saveDerived(geomAnd|transistor(elec) (SCMOS 13.3,15.4) electrode enclosure of cont...))
executing: drc|eEdge viaEdge (enc < (lambda * 2.0)) errMsg)
executing: saveDerived(geomOutside|geodAnd((ce poly) CapacitorElec) errMsg)
executing: drc|eEdge activeEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerived(geomAnd|(ce active) errMsg)
executing: drc|via2Edge (width < (lambda * 2.0)) errMsg)
executing: drc|via2Edge (sep < (lambda * 3.0)) errMsg)
executing: drc|via2Edge (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1)))...))
executing: drc|metal2Edge via2Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerived(geomAnd|Not(via2 metal2) errMsg)
executing: drc|metal3Edge (width < (lambda * 3.0)) errMsg)
drc|metal3Edge (sep < (lambda * 3.0)) errMsg)
drc|metal3Edge (notch < (lambda * 3.0)) errMsg)
executing: drc|metal3Edge via2Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerived(geomAnd|Not(via3 metal3) errMsg)
executing: drc|via3Edge (width < (lambda * 2.0)) errMsg)
executing: drc|via3Edge (sep < (lambda * 3.0)) errMsg)
executing: drc|metal3Edge via3Edge (enc < (lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1)))...))
executing: drc|metal3Edge via3Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerived(geomAnd|Not(via3 metal3) errMsg)
executing: drc|metal4Edge (width < (lambda * 6.0)) errMsg)
drc|metal4Edge (notch < (lambda * 6.0)) errMsg)
executing: drc|metal4Edge via3Edge (enc < (lambda * 2.0)) errMsg)
executing: saveDerived(geomAnd|Not(via3 metal4) errMsg)
executing: drc|tactiveEdge (width < (lambda * 4.0)) errMsg)
drc|tactiveEdge activeEdge (sep < (lambda * 4.0)) errMsg)
drc|tactiveEdge (notch < (lambda * 4.0)) errMsg)
executing: drc|tactiveEdge activeEdge (enc < (lambda * 4.0)) errMsg)
drc|tactiveEdge activeEdge (sep < (lambda * 4.0)) errMsg)
executing: drc|geomAnd|(tactiveEdge And((geomDrift|photonicPhotoHic poly)) (width < (lambda * 3....))
executing: saveDerived(geomAnd|(geodaddle(active tactive) (SCMOS Rule 24.6) active may not straddle ...))
DRC started at Sun Aug 8 18:49:03 2024
Completed at Sun Aug 8 18:49:03 2024
  CPUTIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "Half_adder layout" *****
Total errors found: 0

```

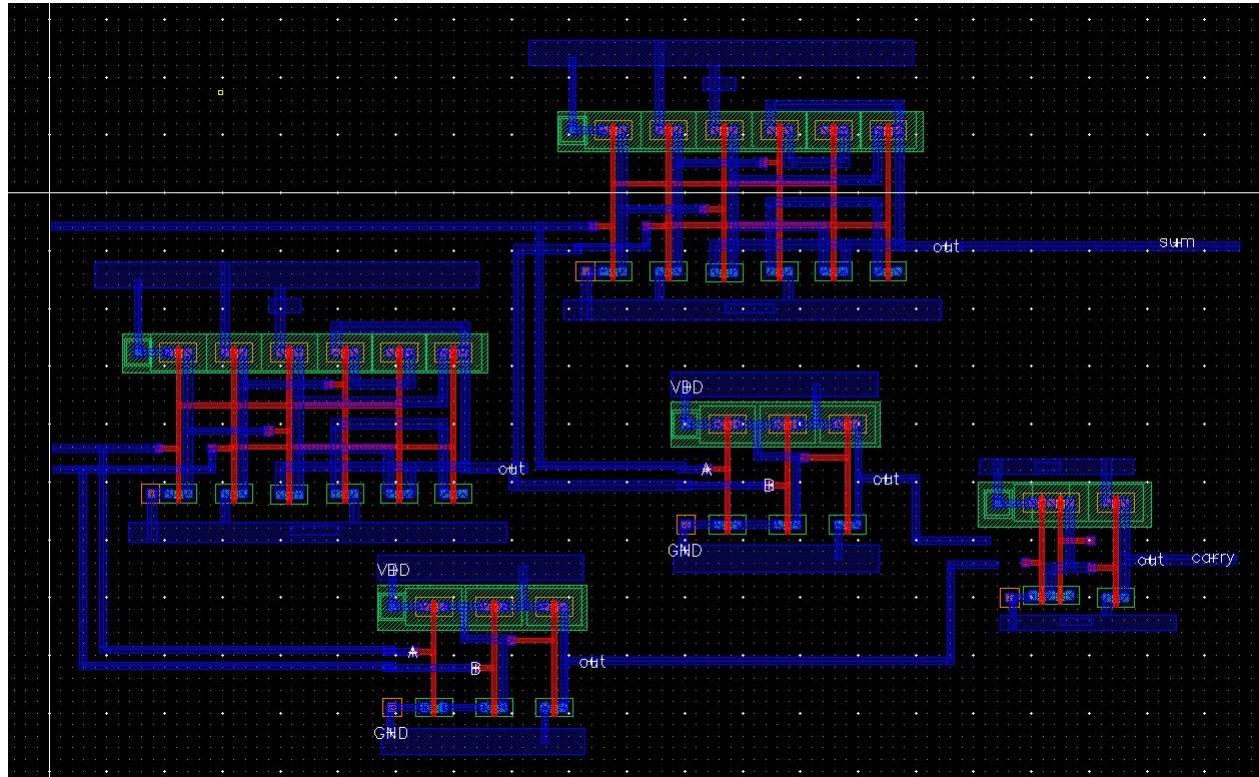
# FULL ADDER Schematic



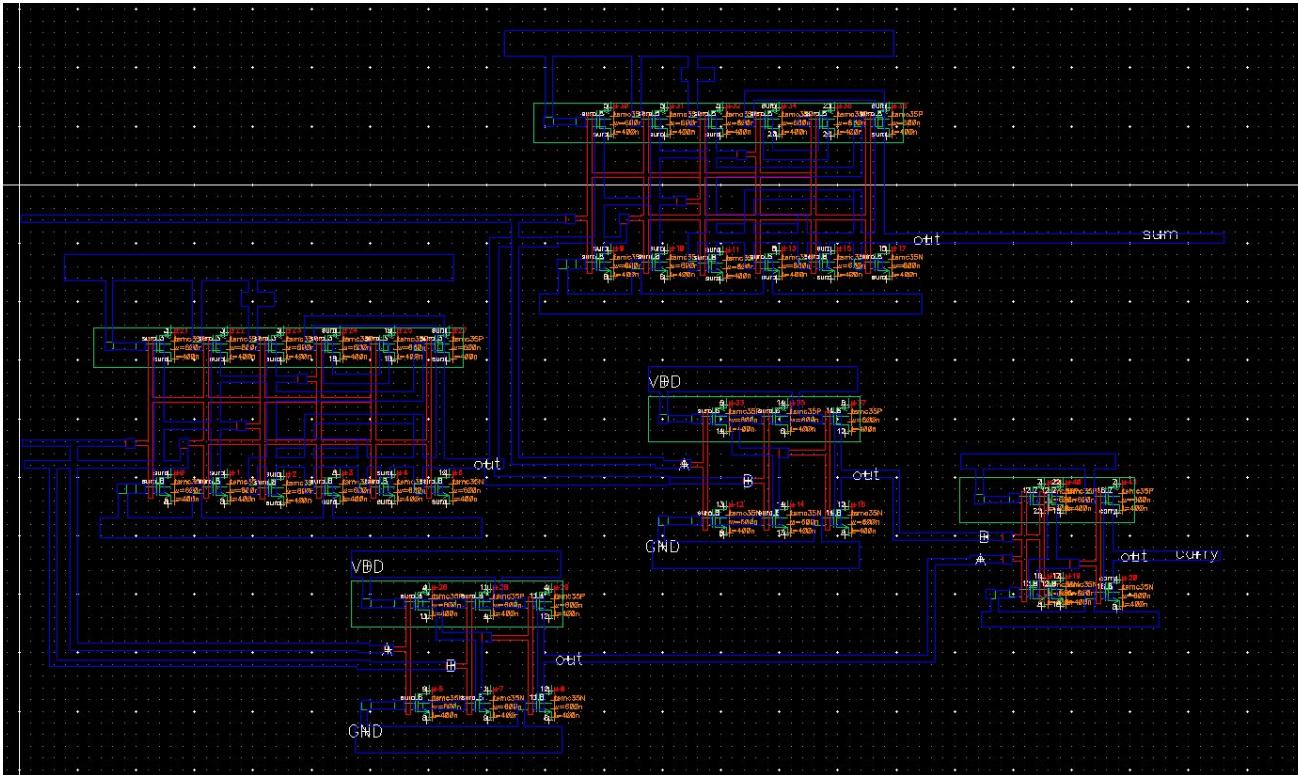
Full Adder

A	B	C	C Out	Sum
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

# FULL ADDER LAYOUT



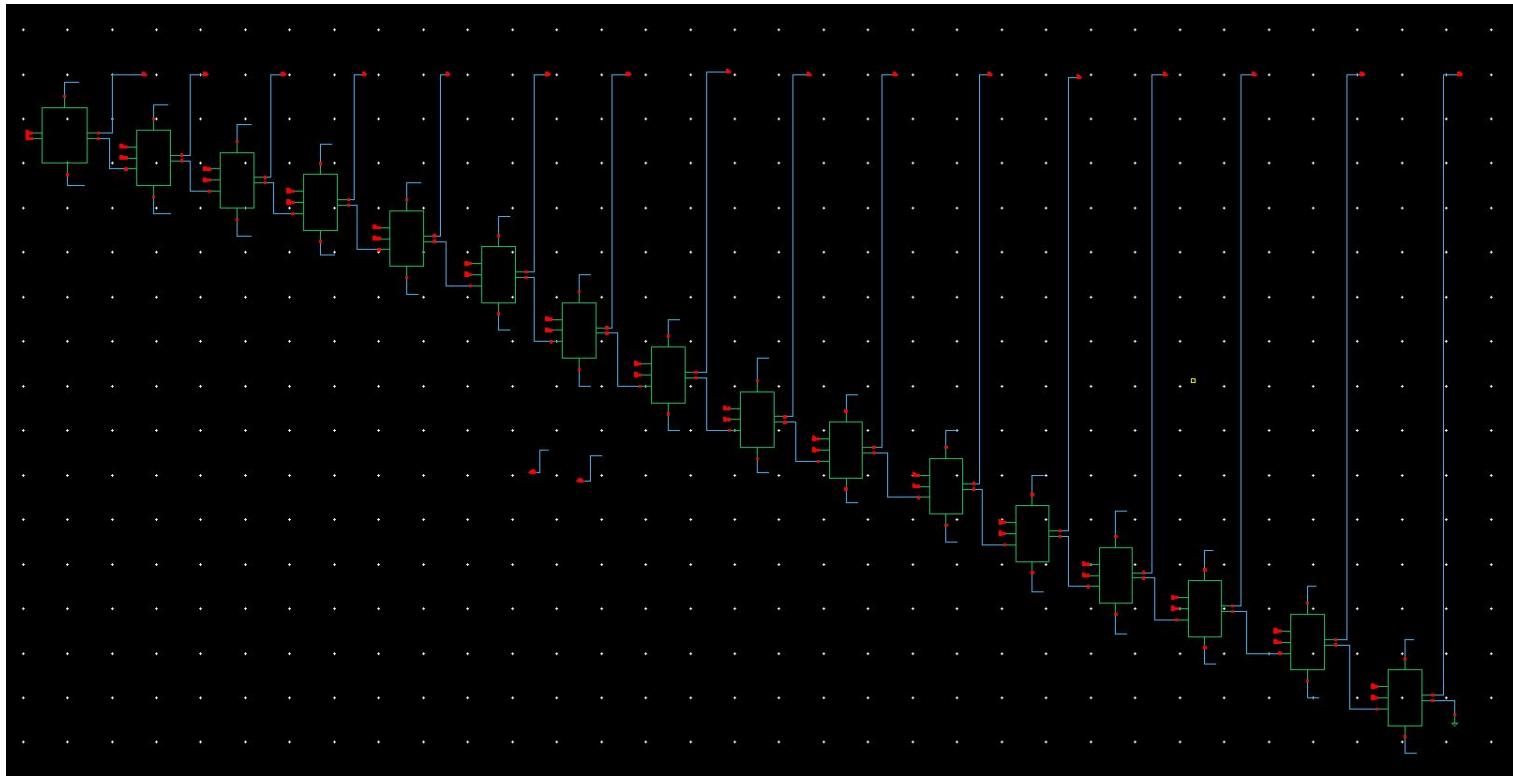
# FULL ADDER EXTRACTED



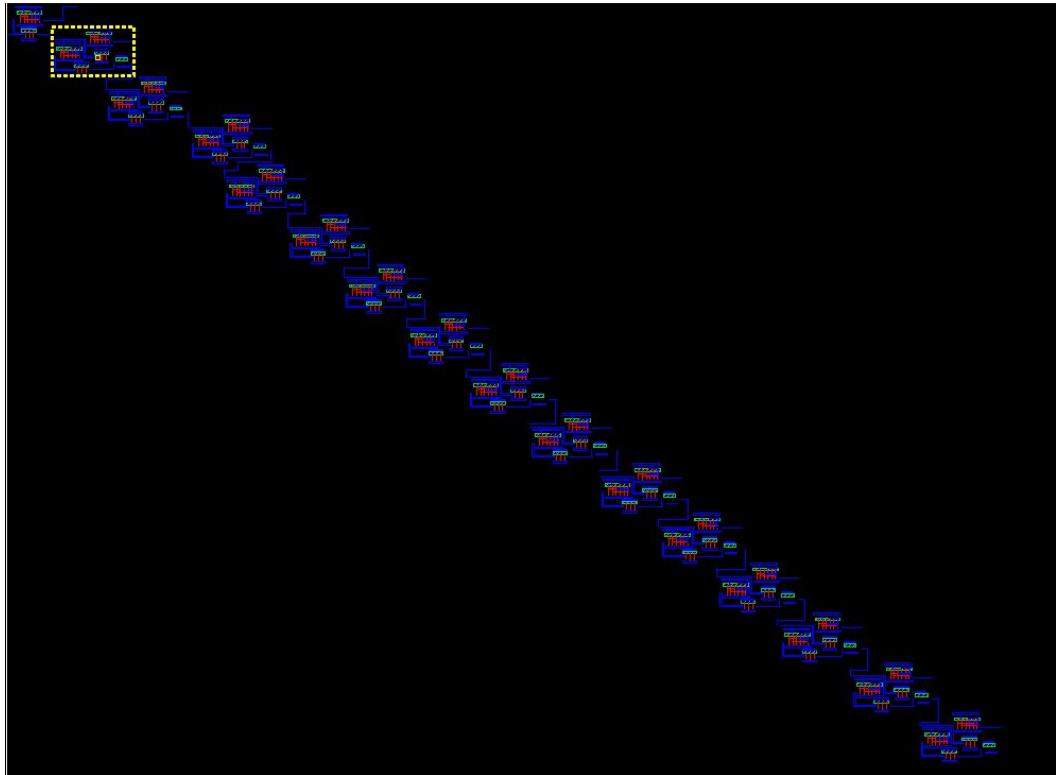
# FULL ADDER VERIFICATION

```
executing: drc(geomGetEdge("elec")) geomGetEdge("metal14") (sep < (lambda * 2.0)) errMsg
executing: saveDerived(geomOverlap(metal14 elec diffNet) errMsg)
executing: drc(geomGetEdge("elec")) geomGetEdge("metal13") (sep < (lambda * 2.0)) errMsg
executing: saveDerived(geomOverlap(metal13 elec diffNet) errMsg)
executing: drc(geomGetEdge("elec")) geomGetEdge("metal12") (sep < (lambda * 2.0)) errMsg
executing: saveDerived(geomOverlap(metal12 elec diffNet) errMsg)
executing: drc(geomGetEdge("elec")) geomGetEdge("metal11") (sep < (lambda * 2.0)) errMsg
executing: saveDerived(geomOverlap(metal11 elec diffNet) errMsg)
executing: saveDerived(geomOverlap(metal10 elec diffNet) errMsg)
executing: drc(TransistorElecEdge (width < (lambda * 2.0)) errMsg)
drc(TransistorElecEdge (sep < (lambda * 3.0)) errMsg)
drc(TransistorElecEdge (notch < (lambda * 3.0)) errMsg)
executing: drc(TransistorElecEdge activeEdge (enc < (lambda * 2.0)) errMsg)
drc(TransistorElecEdge activeEdge (sep < (lambda * 1.0)) errMsg)
executing: drc(TransistorElecEdge polyEdge (sep < (lambda * 2.0)) errMsg)
drc(TransistorElecEdge polyEdge (ovlp < (lambda * 2.0)) errMsg)
executing: drc(TransistorElecEdge cpEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerived(geomAnd(TransistorElec cp) errMsg)
executing: drc(TransistorElecEdge caEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerived(geomAnd(TransistorElec ca) errMsg)
executing: drc(ceEdge (width < (lambda * 2.0)) errMsg)
executing: drc(ceEdge (sep < (lambda * 3.0)) errMsg)
drc(ceEdge (notch < (lambda * 3.0)) errMsg)
drc(ceEdge (sep < (lambda * 3.0)) errMsg)
executing: drc(ceEdge (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1)))) ...)
executing: drc(CapacitorElecEdge ceEdge (enc < (lambda * 3.0)) errMsg)
executing: drc(TransistorElecEdge ceEdge (enc < (lambda * 2.0)) errMsg)
executing: saveDerived(geomAndNot(ce elec) "(SMOS Rules 13.3,13.4) electrode enclosure of cont...")
executing: drc(ceEdge polyEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerived(geomAndNot(ce poly) CapacitorElec) errMsg
executing: drc(ceEdge activeEdge (sep < (lambda * 1.0)) errMsg)
executing: saveDerived(geomAnd(ce active) errMsg)
executing: drc(via12Edge (width < (lambda * 2.0)) errMsg)
drc(via12Edge (sep < (lambda * 3.0)) errMsg)
executing: drc(via12 (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1))))...
executing: drc(metal2Edge via2Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerived(geomAndNot(via2 metal12) errMsg)
executing: drc(metal13Edge (sep < (lambda * 3.0)) errMsg)
drc(metal13Edge (notch < (lambda * 3.0)) errMsg)
executing: drc(metal13Edge via2Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerived(geomAndNot(via2 metal13) errMsg)
executing: drc(via3Edge (width < (lambda * 2.0)) errMsg)
drc(via3Edge (sep < (lambda * 3.0)) errMsg)
executing: drc(via3 (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1))))...
executing: drc(metal13Edge via3Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerived(geomAndNot(metal13) errMsg)
executing: drc(metal14Edge (width < (lambda * 6.0)) errMsg)
drc(metal14Edge (sep < (lambda * 6.0)) errMsg)
drc(metal14Edge (notch < (lambda * 6.0)) errMsg)
executing: drc(metal14Edge via3Edge (enc < (lambda * 2.0)) errMsg)
executing: saveDerived(geomAndNot(via3 metal14) errMsg)
executing: drc(tactiveEdge (sep < (lambda * 4.0)) errMsg)
drc(tactiveEdge (width < (lambda * 4.0)) errMsg)
executing: drc(tactiveEdge (notch < (lambda * 4.0)) errMsg)
executing: drc(tactiveEdge activeEdge (enc < (lambda * 4.0)) errMsg)
executing: drc(geomAnd((tactive geomAnd(geomOr((Not)hmic phNotHnic) poly)) (width < (lambda * 3...))
executing: saveDerived(geomStraddle(active tactive) "(SMOS Rule 24.6) active may not straddle ...
DRC started.....Sun Dec  8 18:55:03 2024
completed ....Sun Dec  8 18:55:03 2024
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "full_adder layout" *****
Total errors found: 0
```

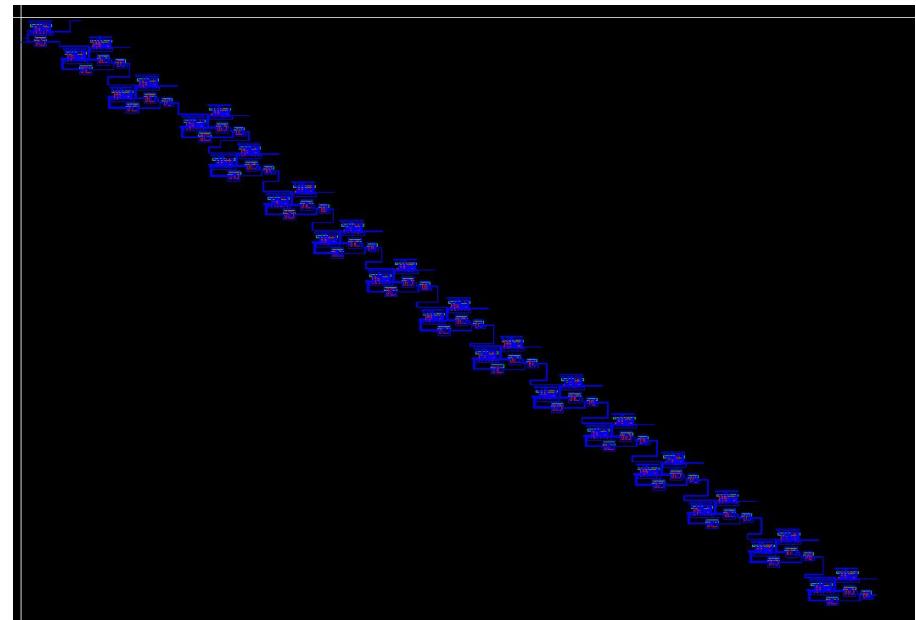
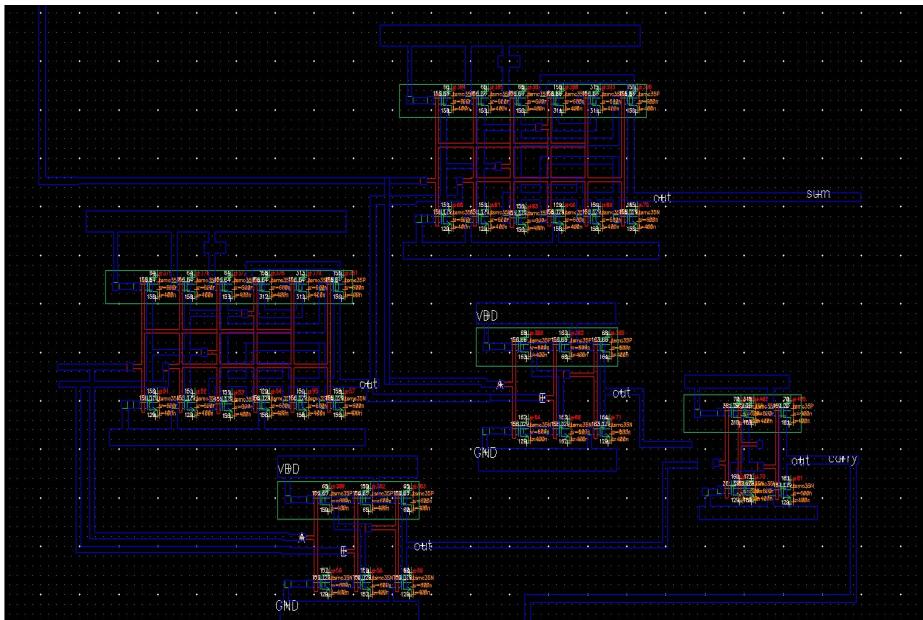
# ADDER BLOCK Schematic



# ADDER LAYOUT



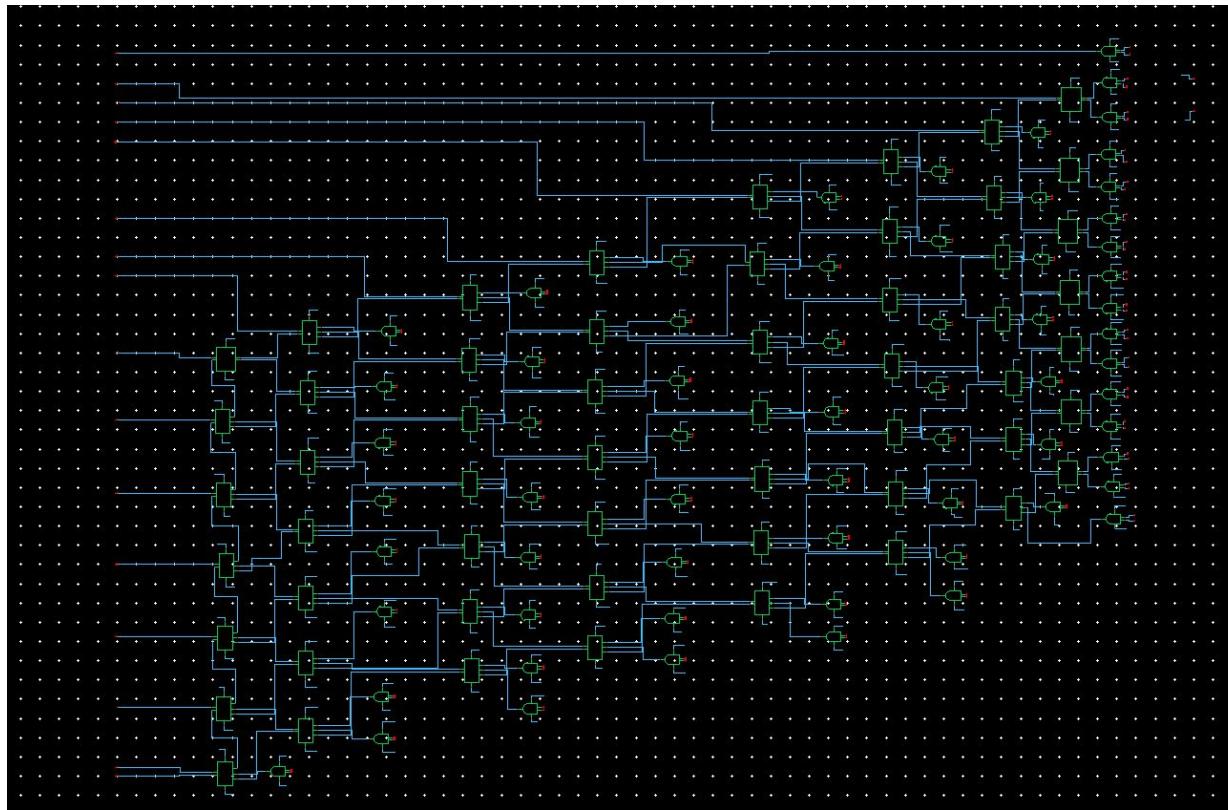
# ADDER EXTRACTED



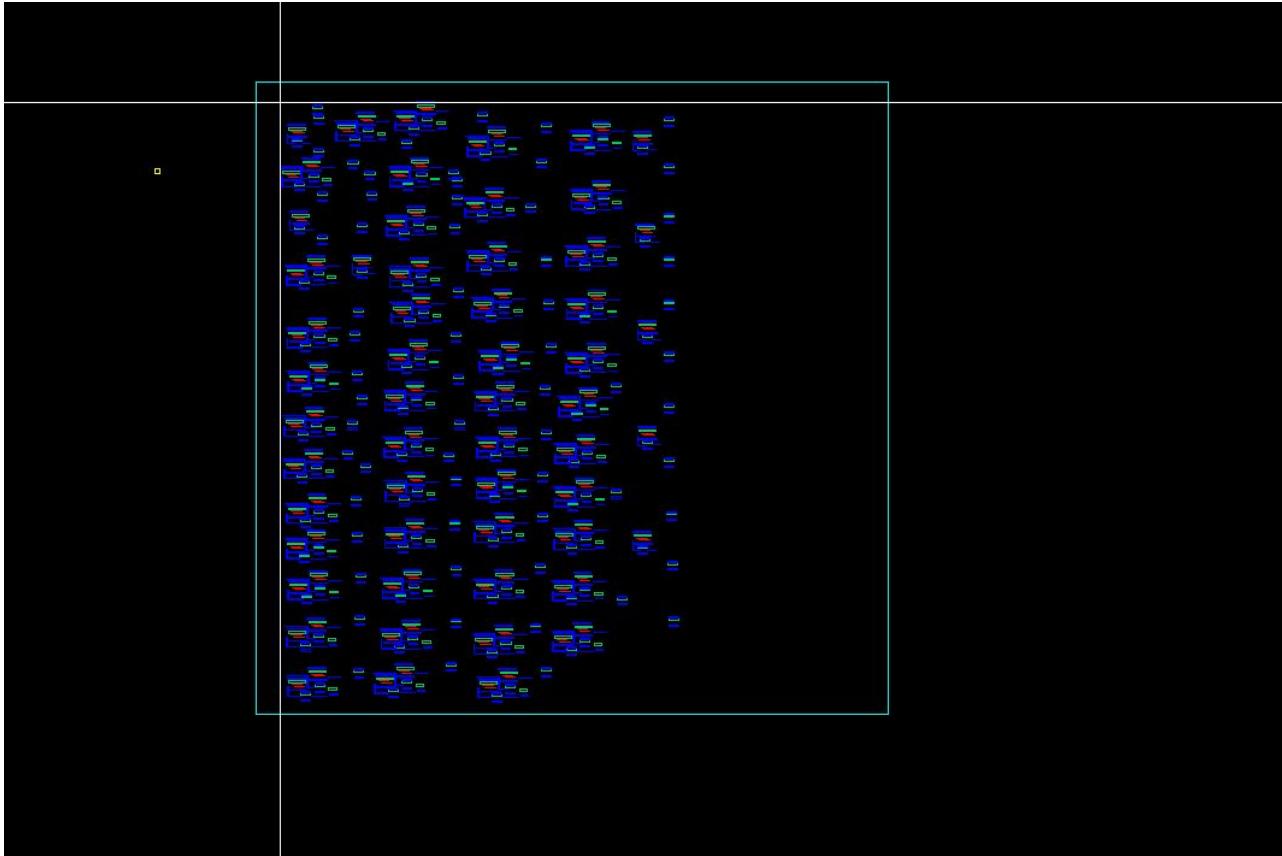
# ADDER VERIFICATION

```
executing: drc(geomGetEdge("elec")) geomGetEdge("metal14") (sep < ((lambda * 2.0)) errMsg)
executing: saveDerivedGeomOverlap(metal14 elec diffNet) errMsg
executing: drc(geomGetEdge("elec")) geomGetEdge("metal13") (sep < ((lambda * 2.0)) errMsg)
executing: saveDerivedGeomOverlap(metal13 elec diffNet) errMsg
executing: drc(geomGetEdge("elec")) geomGetEdge("metal12") (sep < ((lambda * 2.0)) errMsg)
executing: saveDerivedGeomOverlap(metal12 elec diffNet) errMsg
executing: saveDerivedGeomOverlap(metal11 elec diffNet) errMsg
executing: saveDerivedGeomOverlap(metal11 elec diffNet) errMsg
executing: drc(TransistorElecEdge (width < (lambda * 2.0)) errMsg)
drc(TransistorElecEdge (sep < (lambda * 3.0)) errMsg)
executing: drc(TransistorElecEdge (notch < (lambda * 3.0)) errMsg)
executing: drc(TransistorElecEdge activeEdge (enc < (lambda * 2.0)) errMsg)
drc(TransistorElecEdge activeEdge (sep < (lambda * 1.0)) errMsg)
executing: drc(TransistorElecEdge polyEdge (sep < (lambda * 2.0)) errMsg)
executing: drc(TransistorElecEdge polyEdge (oval < (lambda * 2.0)) errMsg)
executing: drc(TransistorElecEdge polyEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerivedGeomAnd(TransistorElec ca) errMsg
executing: drc(cceEdge (sep < (lambda * 2.0)) errMsg)
executing: drc(cceEdge (width < (lambda * 2.0)) errMsg)
drc(cceEdge (sep < (lambda * 3.0)) errMsg)
drc(cceEdge (notch < (lambda * 3.0)) errMsg)
executing: drc(cceEdge (area > ((lambda * 2.0 * ((lambda * 2.0) + (lambda * 0.1 * (lambda * 0.1)))) ...))
executing: drc(cceEdge (area < ((lambda * 2.0 * ((lambda * 2.0) + (lambda * 0.1 * (lambda * 0.1)))) ...))
executing: drc(TransistorElecEdge cedge (enc < (lambda * 3.0)) errMsg)
executing: drc(TransistorElecEdge cedge enc < (lambda * 2.0)) errMsg
executing: saveDerivedGeomAndNot((ce elec) "(SMOS Rule 13.3,13.4) electrode enclosure of cont..."))
executing: drc(cceEdge polyEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerivedGeomOutside(geomAnd((ce poly) CapacitorElec) errMsg)
executing: drc(cceEdge activeEdge (sep < (lambda * 3.0)) errMsg)
executing: saveDerivedGeomAnd((ce active) errMsg)
executing: drc(cvia2Edge (width < (lambda * 2.0)) errMsg)
executing: drc(cvia2Edge (sep < (lambda * 3.0)) errMsg)
executing: drc(cvia2Edge (notch < (lambda * 2.0 * ((lambda * 2.0) + (lambda * 0.1 * (lambda * 0.1)))) ...))
executing: drc(cvia2Edge (notch < (lambda * 2.0 * ((lambda * 2.0) + (lambda * 0.1 * (lambda * 0.1)))) ...))
executing: drc(metal3Edge via2Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerivedGeomAndNot((via2 metal2) errMsg)
executing: drc(metal3Edge width < (lambda * 3.0)) errMsg
executing: drc(metal3Edge (sep < (lambda * 3.0)) errMsg)
executing: drc(metal3Edge (notch < (lambda * 3.0)) errMsg)
executing: drc(metal3Edge via2Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerivedGeomAndNot((via2 metal3) errMsg)
executing: drc(cvia3Edge (width < (lambda * 2.0)) errMsg)
executing: drc(cvia3Edge (sep < (lambda * 3.0)) errMsg)
executing: drc(cvia3Edge (notch < (lambda * 2.0 * ((lambda * 2.0) + (lambda * 0.1 * (lambda * 0.1)))) ...))
executing: drc(cvia3Edge (enc < (lambda * 1.0)) errMsg)
executing: saveDerivedGeomAndNot((via3 metal3) errMsg)
executing: drc(metal4Edge via3Edge (sep < (lambda * 1.0)) errMsg)
executing: drc(metal4Edge via3Edge (enc < (lambda * 1.0)) errMsg)
executing: drc(metal4Edge (width < (lambda * 6.0)) errMsg)
executing: drc(metal4Edge (sep < (lambda * 6.0)) errMsg)
executing: drc(metal4Edge (notch < (lambda * 6.0)) errMsg)
executing: drc(metal4Edge via3Edge (enc < (lambda * 2.0)) errMsg)
executing: saveDerivedGeomAndNot((via3 metal4) errMsg)
executing: drc(activeEdge (width < (lambda * 4.0)) errMsg)
drc(activeEdge (sep < (lambda * 4.0)) errMsg)
drc(activeEdge (notch < (lambda * 4.0)) errMsg)
executing: drc(activeEdge activeEdge (enc < (lambda * 4.0)) errMsg)
drc(activeEdge activeEdge (sep < (lambda * 4.0)) errMsg)
executing: drc(geomAnd(tactive geomOr((geomOr((not0Hmic photoHmic) poly))) (width < (lambda * 3....)))
executing: saveDerivedGeomStraddle(active tactive) "(SMOS Rule 24.6) active may not straddle ..."
DRC started..... Sun Dec 8 18:40:51 2024
Completed..... Sun Dec 8 18:40:52 2024
CPU TIME = 00:00:00 TOTAL TIME = 00:00:01
***** Summary of rule violations for cell "adder layout" *****
Total errors found: 0
```

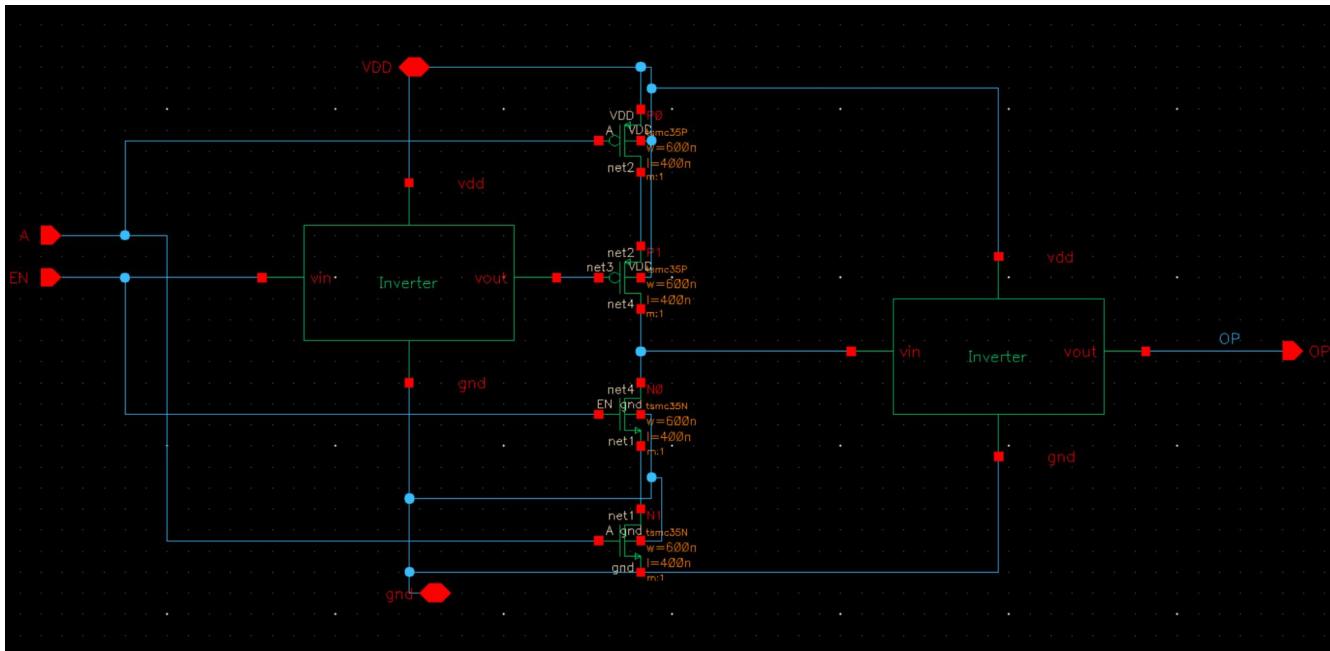
# MULTIPLIER Schematic



# MULTIPLIER LAYOUT



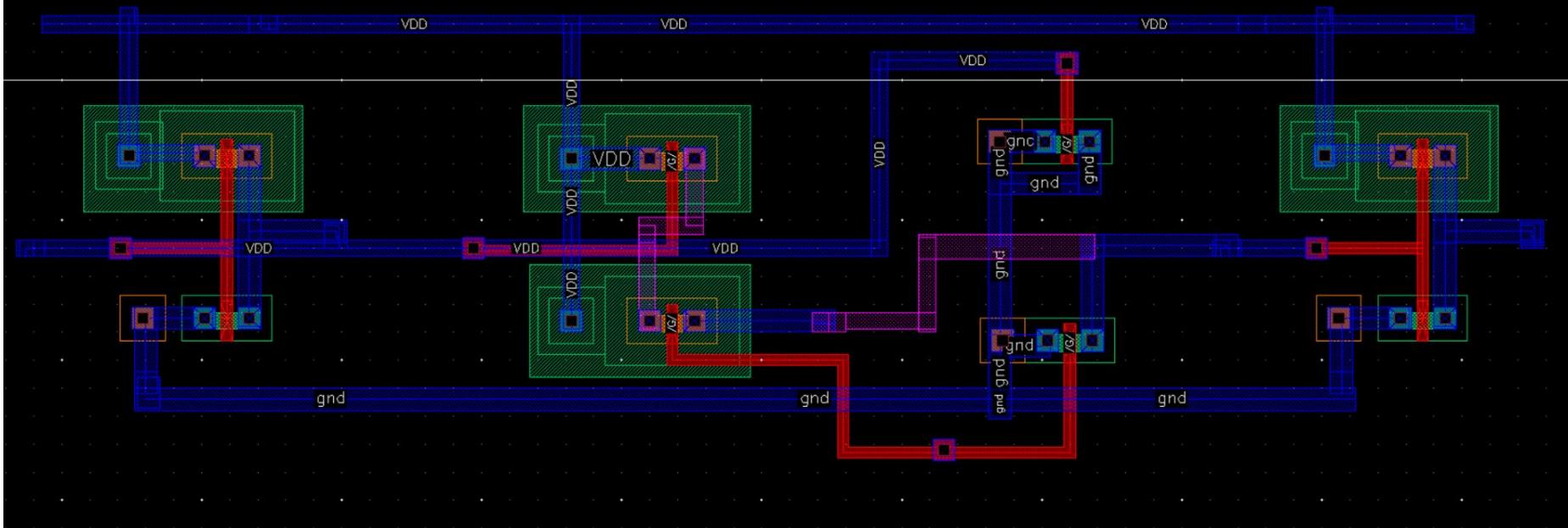
# TRI STATE BLOCK SCHEMATIC



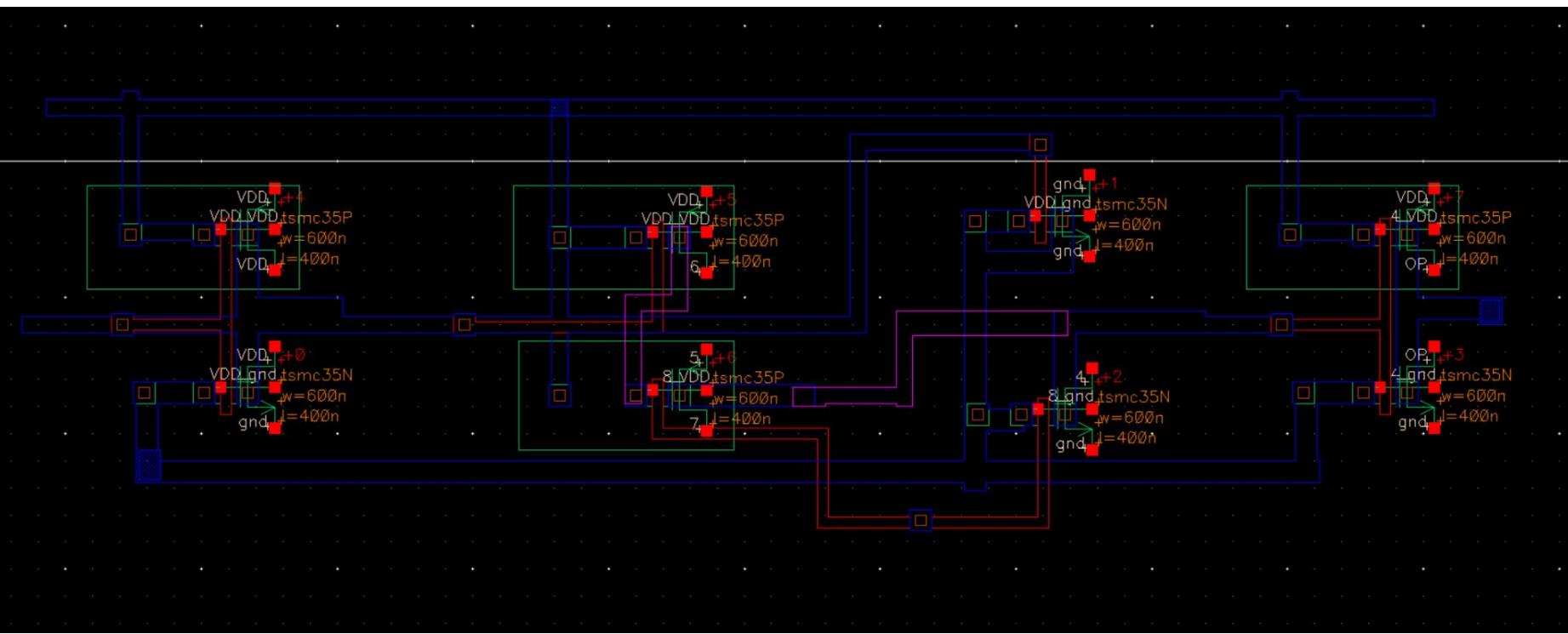
## Truth table

A	B	Output
0	0	High-Z
0	1	0
1	0	High-Z
1	1	1

# TRI STATE LAYOUT



# TRI-STATE EXTRACTED



# TRI-STATE VERIFICATION

```

drc(ceEdge (notch < (lambda * 3.0)) errMesg)
executing: drc(ce (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1)))) ... 
executing: drc(CapacitorElecEdge ceEdge (enc < (lambda * 3.0)) errMesg)
executing: drc(TransistorElecEdge ceEdge (enc < (lambda * 2.0)) errMesg)
executing: saveDerived(geomAndNot(ce elec) "(SCMOS Rules 13.3,13.4) electrode enclosure of cont...
executing: drc(ceEdge polyEdge (sep < (lambda * 3.0)) errMesg)
executing: saveDerived(geomOutside(geomAnd(ce poly) CapacitorElec) errMesg)
executing: drc(ceEdge activeEdge (sep < (lambda * 3.0)) errMesg)
executing: saveDerived(geomAnd(ce active) errMesg)
executing: drc(via2Edge (width < (lambda * 2.0)) errMesg)
drc(via2Edge (sep < (lambda * 3.0)) errMesg)
executing: drc(via2 (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1))))...
executing: drc(metal2Edge via2Edge (enc < (lambda * 1.0)) errMesg)
executing: saveDerived(geomAndNot(via2 metal2) errMesg)
executing: drc(metal3Edge (width < (lambda * 3.0)) errMesg)
drc(metal3Edge (sep < (lambda * 3.0)) errMesg)
drc(metal3Edge via2Edge (enc < (lambda * 1.0)) errMesg)
executing: saveDerived(geomAndNot(via2 metal3) errMesg)
executing: drc(via3Edge (width < (lambda * 2.0)) errMesg)
drc(via3Edge (sep < (lambda * 3.0)) errMesg)
executing: drc(via3 (area > ((lambda * 2.0 * (lambda * 2.0)) + (lambda * 0.1 * (lambda * 0.1))))...
executing: drc(metal3Edge via3Edge (enc < (lambda * 1.0)) errMesg)
executing: saveDerived(geomAndNot(via3 metal3) errMesg)
executing: drc(metal4Edge (width < (lambda * 6.0)) errMesg)
drc(metal4Edge (sep < (lambda * 6.0)) errMesg)
drc(metal4Edge (notch < (lambda * 6.0)) errMesg)
executing: drc(metal4Edge via3Edge (enc < (lambda * 2.0)) errMesg)
executing: saveDerived(geomAndNot(via3 metal4) errMesg)
executing: drc(tactiveEdge (width < (lambda * 4.0)) errMesg)
drc(tactiveEdge (sep < (lambda * 4.0)) errMesg)
drc(tactiveEdge (notch < (lambda * 4.0)) errMesg)
executing: drc(tactiveEdge activeEdge (enc < (lambda * 4.0)) errMesg)
drc(tactiveEdge activeEdge (sep < (lambda * 4.0)) errMesg)
executing: drc(geomAnd(tactive geomAnd(geomOr(nNotOhmic pNotOhmic poly)) (width < (lambda * 3....)
executing: saveDerived(geomStraddle(active tactive) "(SCMOS Rule 24.6) active may not straddle ...
DRC started.....Sun Dec 8 20:10:10 2024
    completed ...Sun Dec 8 20:10:10 2024
    CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "tri-state-buffer layout" *****
Total errors found: 0

```

```

Command line: /export/opt/cadence/install/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/sshaik2680/project/LVS -.
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

```

Net-list summary for /home/sshaik2680/project/LVS/layout/netlist

count	
4	nets
4	terminals
1	pmos
1	nmox

Net-list summary for /home/sshaik2680/project/LVS/schematic/netlist

count	
4	nets
4	terminals
1	pmos
1	nmox

Terminal correspondence points

N2	N3	gnd
N0	N2	vdd
N3	N0	vin
N1	N1	vout

Devices in the rules but not in the netlist:

cap ngef pfet nmox4 pmos4

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	2	2
total	2	2

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	4	4
total	4	4

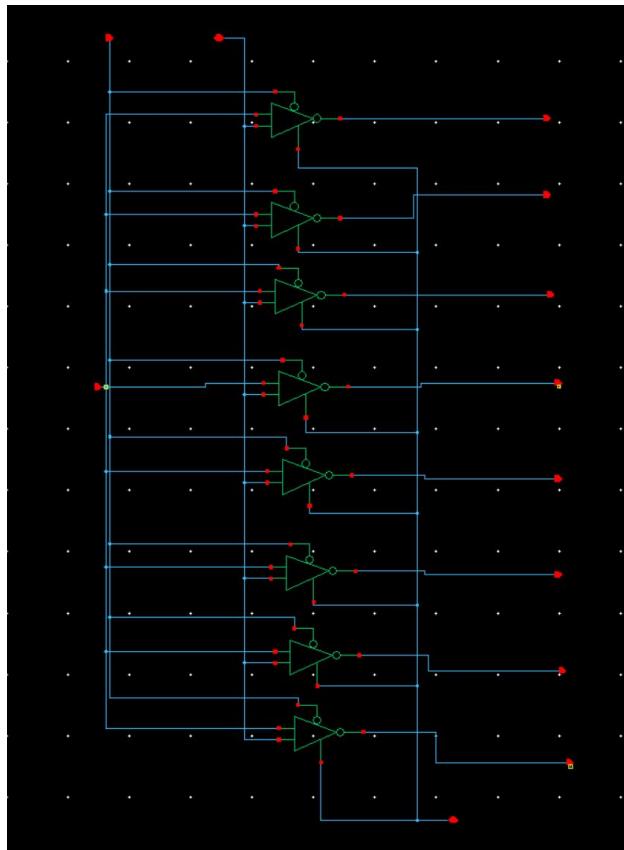
	terminals	
un-matched	0	0
matched but different type	0	0
total	4	4

Probe files from /home/sshaik2680/project/LVS/schematic

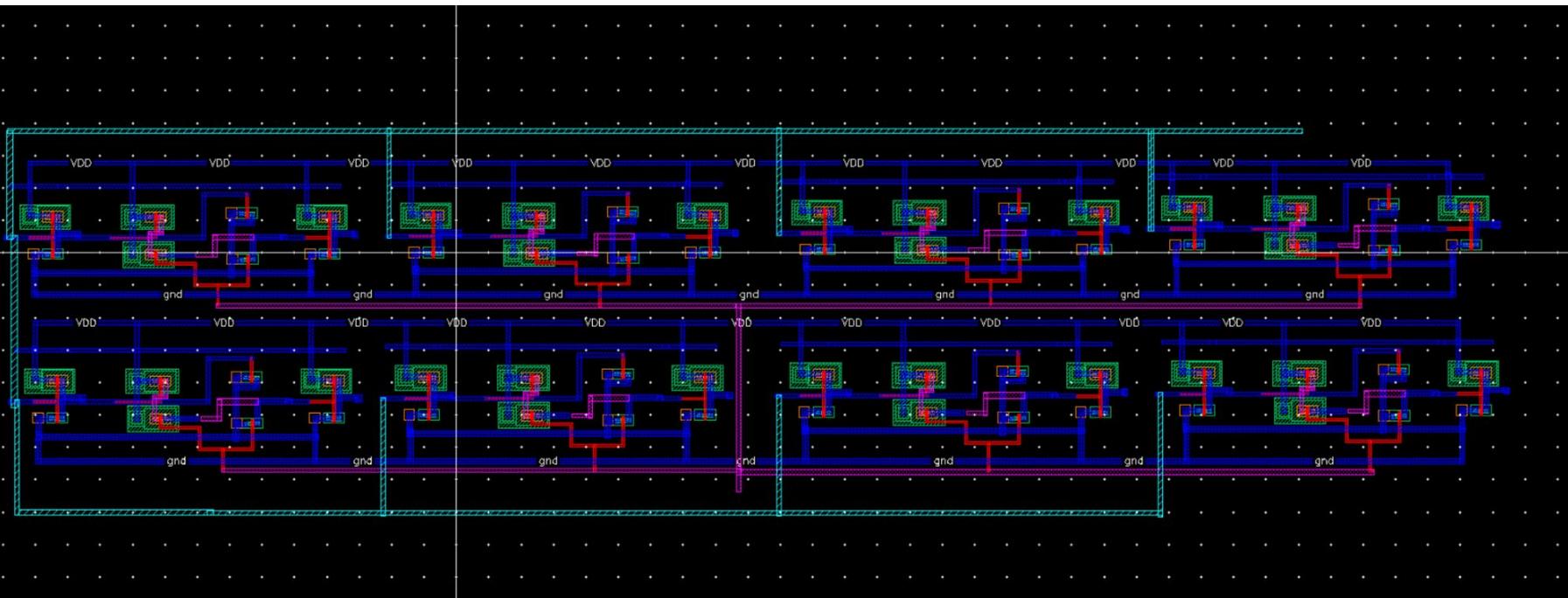
devbad.out:

netbad.out:

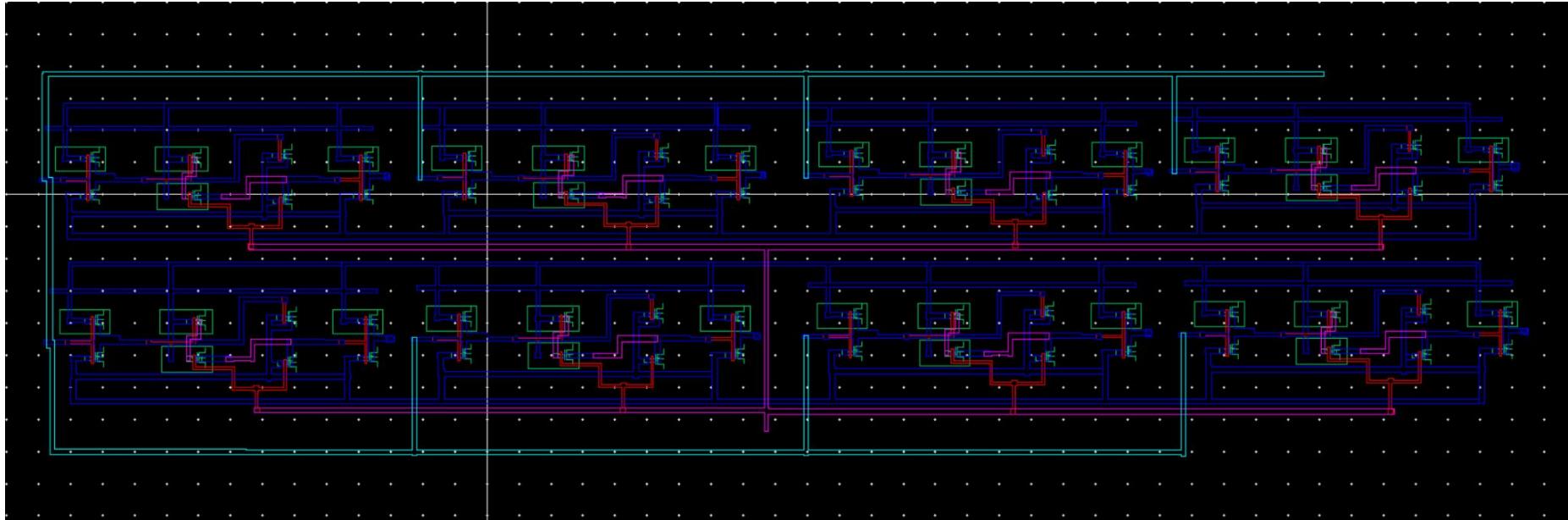
# SINGLE COLOR OUTPUT SCHEMATIC



# SINGLE COLOR OUTPUT LAYOUT



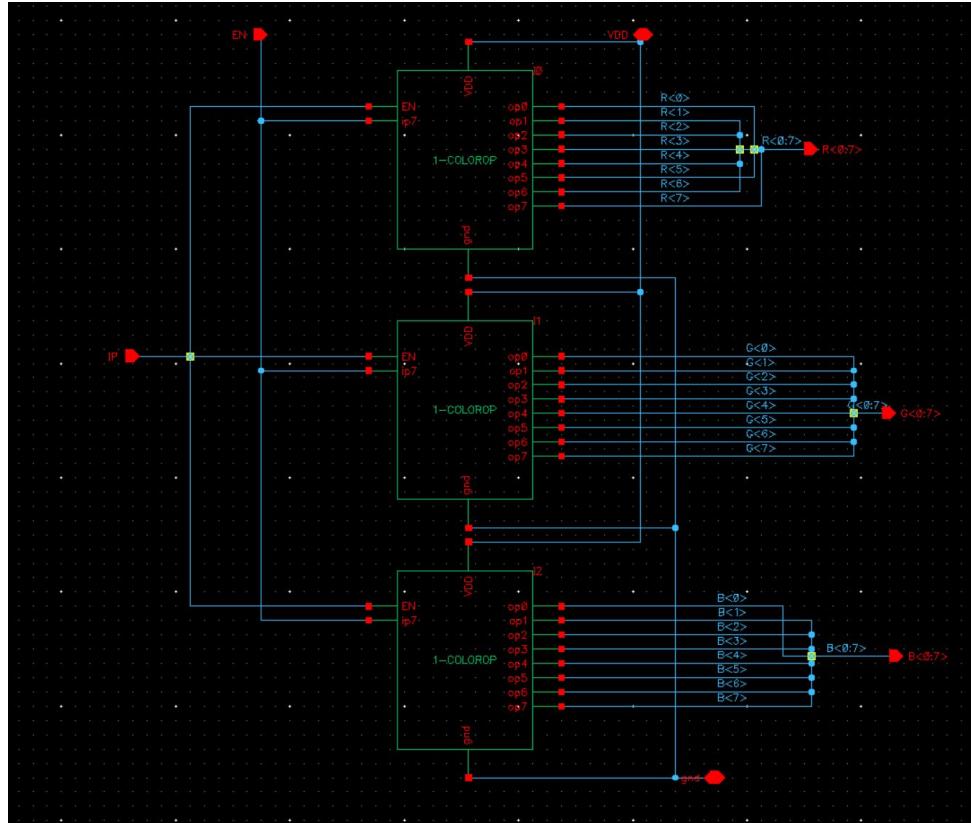
# SINGLE COLOR OUTPUT EXTRACTED



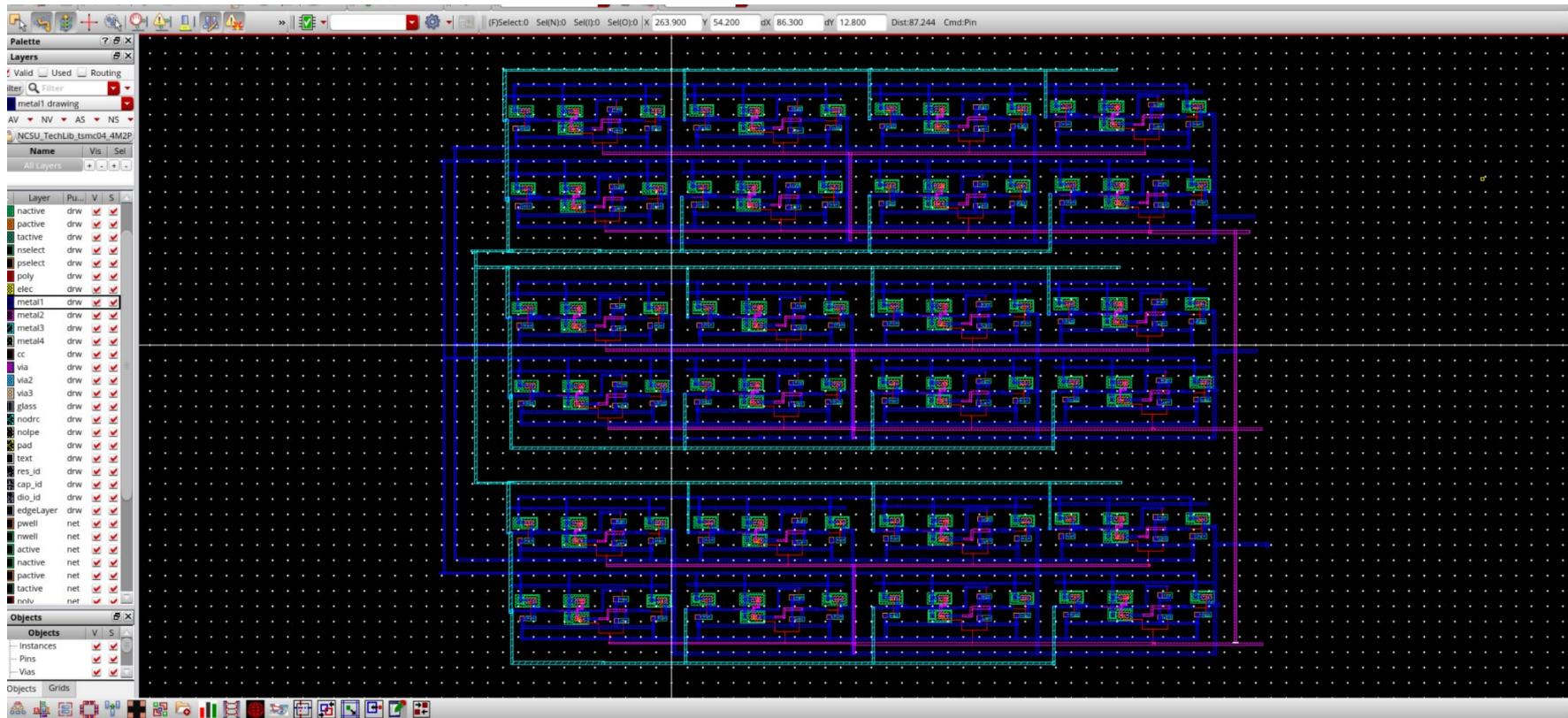
# SINGLE COLOR OUTPUT VERIFICATION

```
@(#) $CDS: LVS version 6.1.8-64b 01/31/2023 19:16 (sjfhw317) $  
Command line: /export/opt/cadence/install/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/sshaik2680/project/LVS -l -s -t /home/sshaik2680/project/LVS/layout /home/sshaik2680/project/LVS/schematic  
Like matching is enabled.  
Net swapping is enabled.  
Using terminal names as correspondence points.  
Compiling Diva LVS rules...  
  
Net-list summary for /home/sshaik2680/project/LVS/layout/netlist  
count  
    4      nets  
    4      terminals  
    1      pmos  
    1      nmos  
  
Net-list summary for /home/sshaik2680/project/LVS/schematic/netlist  
count  
    4      nets  
    4      terminals  
    1      pmos  
    1      nmos  
  
Terminal correspondence points  
N2      N3      gnd  
N0      N2      vdd  
N3      N0      vin  
N1      N1      vout  
  
Devices in the rules but not in the netlist:  
    cap nfet pfet nmos4 pmos4  
  
The net-lists match.  
  
          layout schematic  
          instances  
un-matched      0      0  
rewired         0      0  
size errors     0      0  
pruned          0      0  
active          2      2  
total           2      2  
  
          nets  
un-matched      0      0  
merged          0      0  
pruned          0      0  
active          4      4  
total           4      4  
  
          terminals  
un-matched      0      0  
matched but  
different type   0      0  
total           4      4  
  
Probe files from /home/sshaik2680/project/LVS/schematic  
devbad.out:
```

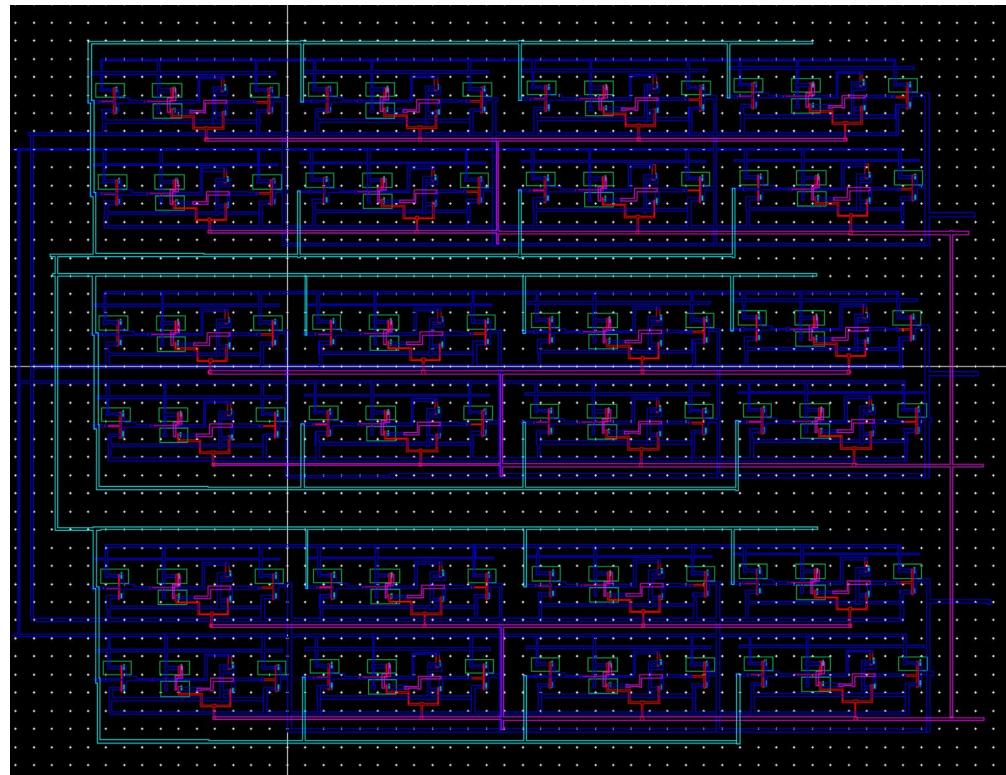
# COLOR DETECTION BLOCK SCHEMATIC



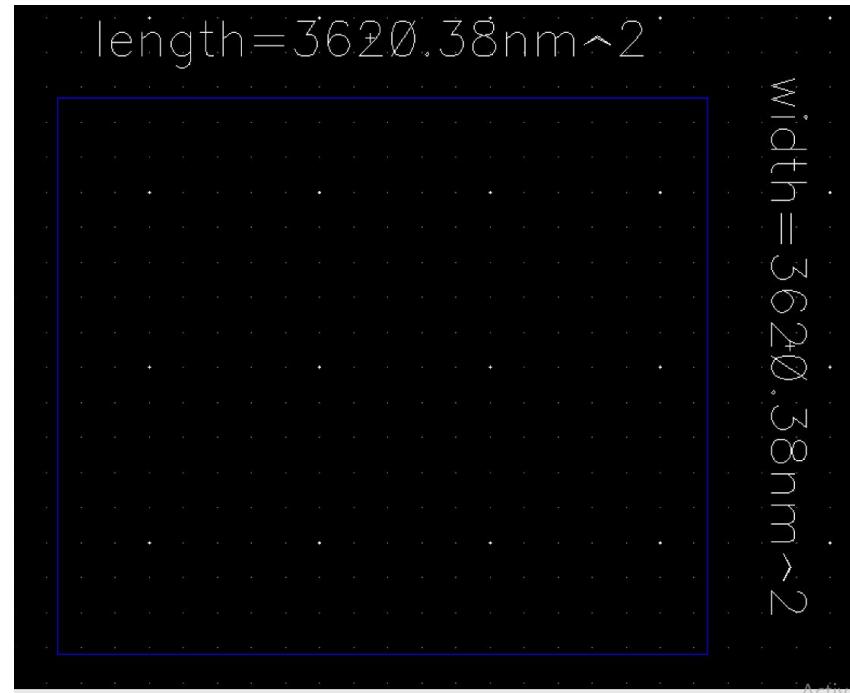
# COLOR DETECTION BLOCK LAYOUT



# COLOR DETECTION BLOCK EXTRACTED



# ROM Layout As Black Box



For layout ROM is implemented as square black box with length=3620.38nm<sup>2</sup> and width=3620.38nm<sup>2</sup> to fit in estimated area of 13107200 nm<sup>2</sup>=13.1μm<sup>2</sup>

# Floor-Planning And Area Estimation Of Tri State Buffer

Each transistor is 600 nm wide and 400 nm long, so each transistor occupies **240,000 nm<sup>2</sup>**. We must find how many total transistors there are to calculate an area estimate.

Each tri-state buffer has **8 transistors**.

You have used **24 tri-state buffers** in your design.

## Total Transistors

Total transistors =  $24 \times 8 = 192$  transistors

## Total Area

Each transistor occupies **240,000 nm<sup>2</sup>**, so:

Total area =  $192 \times 240,000 \text{ nm}^2 = 46,080,000 \text{ nm}^2 = 46.08 \mu\text{m}^2$

# Area Estimation For Neuron

Neuron Area Estimation=3\*Multiplier+1\*Adder+ROM

Adder Area= **198.72  $\mu\text{m}^2$**

Multiplier Area= **748.8  $\mu\text{m}^2$**

ROM Area=**13.1  $\mu\text{m}^2$**

Total Neuron Area Estimation=3\*748.8+198.72+13.1=**2458.22  $\mu\text{m}^2$**

# Area Estimation Of The Video Processing System

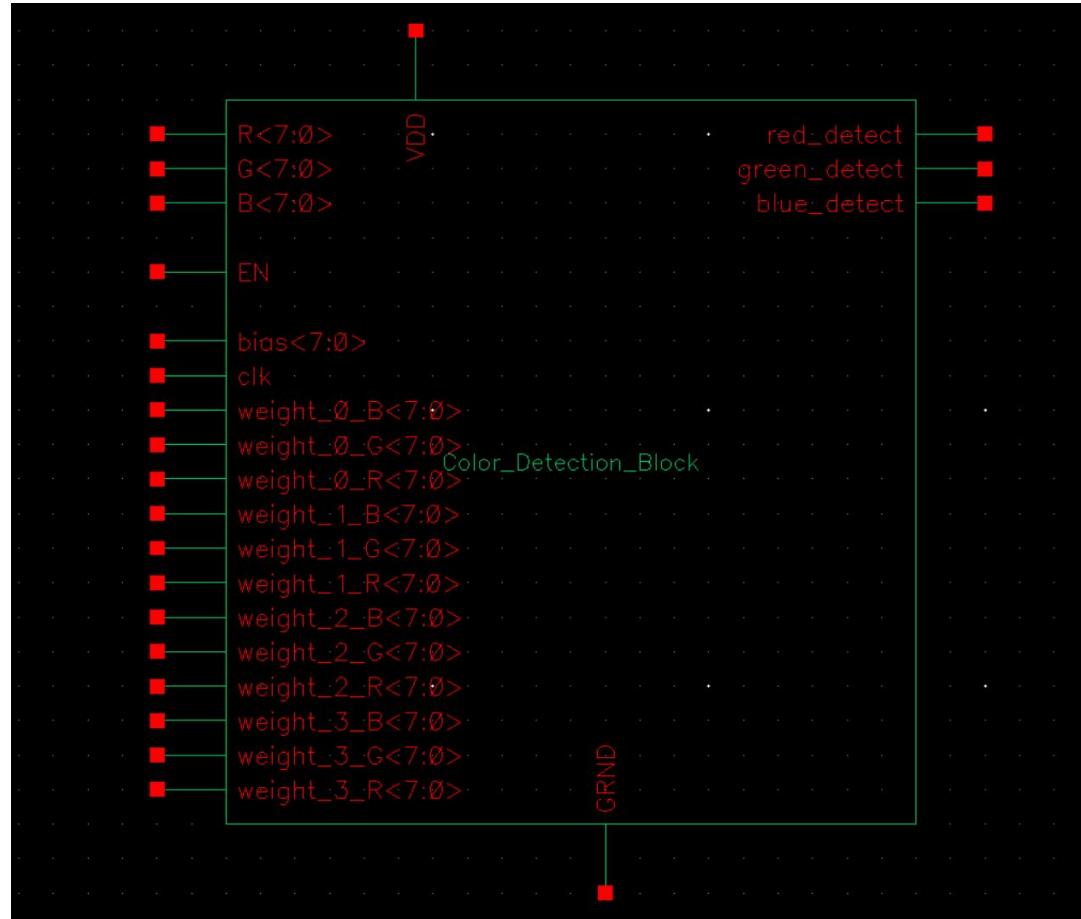
Overall Video Processing System Area Estimation=4\*Neurons+Color Mapping Block

Neuron Block= 2458.22  $\mu\text{m}^2$

Color Mapping Block= 46.08  $\mu\text{m}^2$

**Total Area Estimation=  $4*2458.22+46.08 = 9878.96 \mu\text{m}^2$**

# Overall System I/O And Placement



# Learning Outcomes:

- Gained hands-on experience with Cadence tools for layout design.
- Overcame initial challenges of tool navigation and understanding design flow.
- Developed skills in schematic-to-layout verification and error debugging.
- Learned best practices for adhering to design rules (DRC/LVS).
- Improved understanding of CMOS circuit layout techniques.
- Enhanced ability to troubleshoot and optimize designs for better performance.

# CONCLUSION

- In this project, the design and implementation of key functional blocks, including the **Adder**, **Multiplier**, and **Color Mapping Block**, were successfully completed.
- The layout design, followed by **DRC** and **LVS validations**, ensured compliance with foundry design rules and consistency with the schematic.
- Post-layout simulations revealed minor performance degradations in delay, power, and area, primarily due to parasitic effects introduced during layout.

**THANK YOU**