2024 Digital IC Design

Homework 4: Max-Priority Queue

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Simulation Result								
Functional	Gate-level	Score	Clock	15.0	Gate-level	See below.		
simulation	simulation		width	(ns)	simulation time			
			# output 4f, expect 4f # output 36, expect 36 # output 32, expect 15 # output 05, expect 05 # output 07, expect 07 # output 02, expect 02 # output 09, expect 09 # ** * Congratulations !! ** # ** Simulation PASS !! * / 0.0 # ** * Your score =100 ** / / ^ / ^ # ** Note: \$finish : testfixture.v(180) # output 36, expect 37 # output 36, expect 37 # output 36, expect 37 # output 36, expect 36 # output 37, expect 37 # output 36, expect 37 # output 36, expect 36 # output 37, expect 37 # output 38, expect 38 # output 39, expect 39 # output 31, expect 32 # output 50, expect 05 # output 05, expect 05 # output 07, expect 37 # output 36, expect 37 # output 37, expect 37 # output 38, expect 38 # output 39, expect 39 # output 19, expect 39 # output 10, expect 30 # output 10, expect 30 # output 10, expect 30 # output 31, expect 32 # output 10, expect 36 # output 10, expect 36 # output 07, expect 37 # output 38, expect 38 # output 39, expect 39 # output 39, expect 39 # output 31, expect 39 # output 32, expect 32 # output 33, expect 36 # output 34, expect 35 # output 35, expect 36 # output 36, expect 36 # output 37, expect 37 # output 36, expect 36 # output 37, expect 37 # output 37, expect 37 # output 38, expect 38 # output 39, expect 39 # output 39, expect 30 # output 31, expect 31 # output 31, expect 32 # output 32, expect 32 # output 33, expect 32 # output 34, expect 34 # output 36, expect 36 # output 37, expect 37 # output 36, expect 36 # output 37, expect 37 # output 37, expect 37 # output 38, expect 38 # output 37, expect 37 # output 37, expect 37 # output 38, expect 38 # output 37, expect 37 # output 39, expect 38 # output 39, expect					

```
14,data=06
                                                           # output 37,expect 37
# cycle=
             15,data=4f
                                                           # output 50,expect 50
# output 4f,expect 4f
                                                           # output 36,expect 36
# output 36,expect 36
                                                           # output 06,expect 06
# output 32, expect 32
                                                           # output 45,expect 45
# output 15,expect 15
                                                           # output 34,expect 34
# output 06,expect 06
                                                           # output 15,expect 15
# output 05,expect 05
# output 07,expect 07
                                                           # output 02,expect 02
# output 02,expect 02
                                                           # output 32,expect 32
# output 09,expect 09
   ** Congratulations !!
                                                             ** Congratulations !!
   ** Simulation PASS !! **
                                                             ** Simulation PASS !!
  \m__m_|_|
                                                           # ** Note: $finish : testfixture.v(180)
# Time: 3301806 ps Iteration: 0 Instance: /test
  ** Note: $finish : testfixture.v(180)
     Time: 1630 ns Iteration: 0 Instance: /test
                                                                           P3 (3301.806 ns)
           14,data=06
15,data=4f
# cycle=
                                                           # output 64,expect 64
                                                           # output 37,expect 37
# cycle=
                                                           # output 50,expect 50
# output 50,expect 50
                                                           # output 36,expect 36
# output 37,expect 37
                                                           # output 06,expect 06
# output 45,expect 45
# output 34, expect 34
# output 36, expect 36
# output 06,expect 06
                                                           # output 15.expect 15
# output 05,expect 05
# output 32,expect 32
                                                           # output 02, expect 02
                                                           # output 05,expect 05
# output 15,expect 15
                                                           # output 32,expect 32
# output 02.expect 02
                                                           # output 44,expect 44
   ** Congratulations !!
                                                             ** Congratulations !!
                                                             ** Simulation PASS !!
  ** Simulation PASS !!
                                       / 0.0 |
  ** Your score =100
  \m__m_|_|
                                                           * ** Note: $finish : testfixture.v(180)

# Time: 3301806 ps Iteration: 0 Instance: /test
# ** Note: $finish : testfixture.v(180)
# Time: 1810 ns Iteration: 0 Instance: /test
                                             Synthesis Result
                                                           3,365 / 55,856 (6%)
Total logic elements
                                                           0 / 2,396,160 (0%)
Total memory bit
Embedded multiplier 9-bit element
                                                           0 / 308 (0%)
                    Flow Status
                                                 Successful - Sat May 25 17:07:17 2024
                    Quartus Prime Version
                                                20.1.1 Build 720 11/11/2020 SJ Lite Edition
                    Revision Name
                                                MPO
                    Top-level Entity Name
                                                MPO
                    Family
                                                Cyclone IV E
                                                EP4CE55F23A7
                    Timing Models
                                                Final
                    Total logic elements
                                                3,365 / 55,856 (6%)
                    Total registers
                                                435
                                                50 / 325 (15%)
                    Total virtual pins
                    Total memory bits
                                                0 / 2,396,160 (0%)
                    Embedded Multiplier 9-bit elements 0 / 308 ( 0 % )
                    Total PLLs
                                                0/4(0%)
                                      Description of your design
```

Some of the principles in mind in planning the design are:

- 1. No while or for loops (certainly no recursion). Use state transition to replace.
- 2. In one state, do one job: e.g. a constant-time comparison or value exchange. For example, the core function "MAX_HEAPIFY" is implemented using 3 states: _FIND_LARGEST, _EXCHANGE, DONE_MAX_HEAPIFY. In the first state I compare the index's corresponding value and its left child and right child to get the largest-value index; in _EXCHANGE I change the value, DONE_MAX_HEAPIFY signals the process of MAX_HEAPIFY function is done (resembling the "return to the caller" concept in software; like the recursion call stack is emptied). I ended up designing 14 states for this data structure. See the following state-transition diagram. My design has a clock cycle-width of 15 ns and passes all of the testcases within 1000 cycles.

 $Scoring = (Total\ logic\ elements + total\ memory\ bit + 9*embedded\ multiplier\ 9-bit\ element) \times (Total\ cycle\ used*clock\ width)$

