See other files at:
lab2/lab2.srcs/sources_1/new/light_controller.sv
lab2/lab2.srcs/sources_1/new/register_file.sv
lab2/lab2.srcs/sources_1/new/control_unit.sv
lab2/lab2.srcs/sim_1/new/light_controller_tb.sv
lab2/lab2.srcs/sim_1/new/register_file_tb.sv
lab2/lab2.srcs/sim_1/new/control_unit_tb.sv
Design Exercises submitted separately

Lab 2

I have recreated files several times, as Vivado is not very flexible with renaming files and moving them. I have accidentally created a Verilog file instead of System Verilog, and that copy may still remain in my simulation sources; I only found that out when some syntax wouldn't render.

I found that in design sources, if I put "wire <variable>", I will fail assigning anything to the variable in an "always…" statement. I ended up using reg before each variable with the professor's permission, yet I suppose next time I will just assign a local variable to them outside of always, hope that works.

I referred back to the lecture PPTs on regfiles, and it is very useful. I ended up using some variable names from there, so that things may be more standardized and clearer.

There is some confusion I have over the control unit; if I am to be picky, the words are not the clearest to describe what is wanted. It is especially hard to figure out in what order my orders will be completed, because we are not referencing another module by calls, but by connecting wires.

I also find it extra helpful to use the Message tab to find error messages and figure out debugging. The messages I got from pop-up windows are not helpful at all, but the Message tab gave much more specific instructions. Also, remember to save the file often. Vivado does not update and save automatically.