DIGITAL DESIGN

LAB5 TRUTH-TABLE, SOP,POS, VERILOG(LOOP)

2020 FALL TERM @ CSE . SUSTECH

LAB5

- *Standard form vs SOP*(sum of minterms) vs POS(product of maxterms)
- Verilog
  - repeat, forever, for, while
  - $display, $write, $monitor
- practice

STANDARD FORM VS SOP VS POS

- F(A,B,C)=A+B'C
- F(A,B,C)=AB(C'+C)+AB'(C'+C)+B'C(A'+A)=A'B'C+AB'C'+AB'C+ABC'+ABC
  =m1+m4+m5+m6+m7=∑(1,4,5,6,7)
- F(A,B,C)''=(F(A,B,C)')'=(m0+m2+m3)'=M0.M2.M3 = ∏(0,2,3)

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

```
module lab5(a, b, c, z1, z2, z3);
input a, b, c;
output z1, z2, z3;

assign z1 = a | ((~b) & c);
assign z2 = (a&b&c) | (a&b&(~c)) | (a&(~b)&c) | (a&(~b)&(~c)) | ((~a)&(~b)&c);//m7+m6+m5+m4+m1
assign z3 = (a | b | c) & (a | ~b | c) & (a | ~b | ~c) ;//M0.M2.M3
endmodule
```

TESTBENCH USING LOOP(1)

```
module lab5_tb( );
    reg sa, sb, sc;
    wire sz1, sz2, sz3;
    lab5 ulab5(.a(sa),.b(sb),.c(sc),.z1(sz1),.z3(sz3),.z2(sz2));

    initial
    begin
    {sa, sb, sc} = 3'b000;
    forever
        #100 {sa, sb, sc} = {sa, sb, sc} + 1;
    end
endmodule
```

Tips:

- Select the name of the ports you want to see in group (ctrl + select)
- Right click then choose the “New virtual Bus” to group all the selected ports

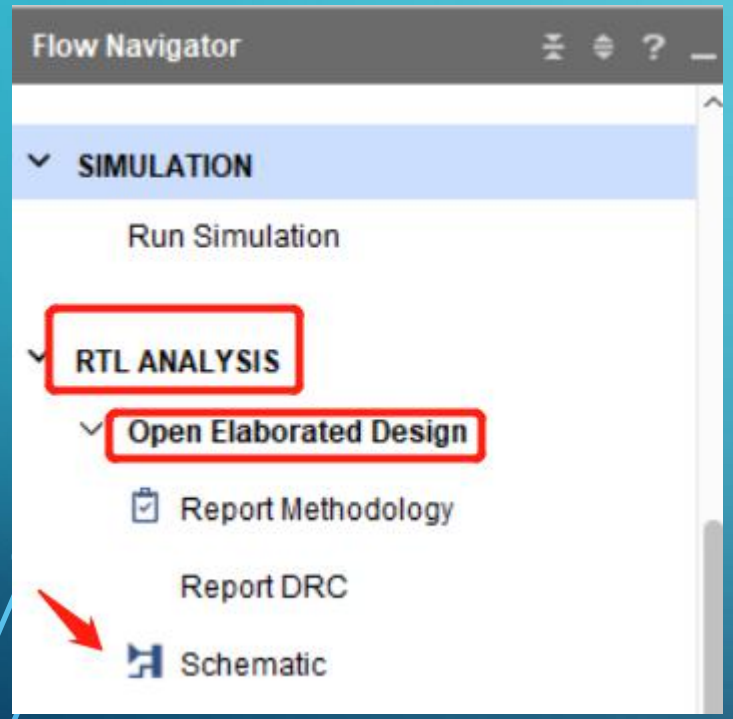
TESTBENCH USING LOOP(2)

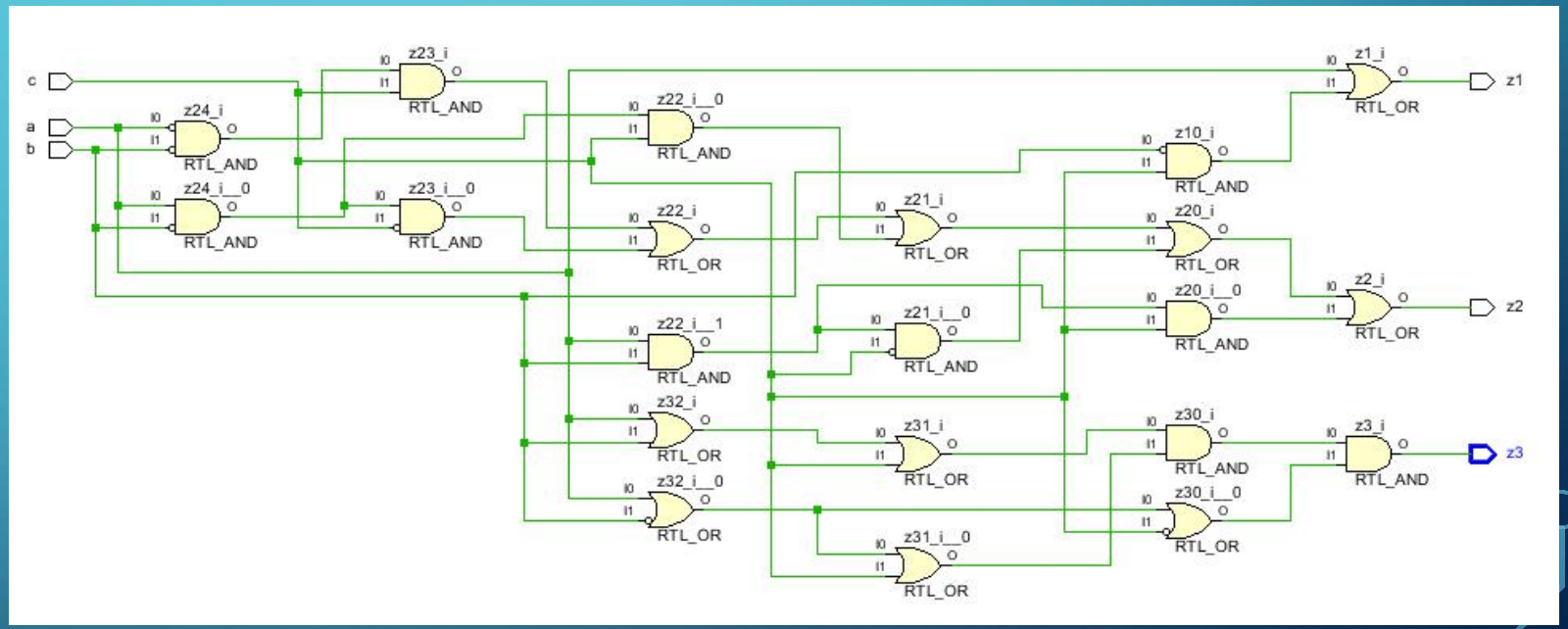
```
initial
begin
    {sa, sb, sc} = 3'b000;
    repeat(7)
    begin
        #100 {sa, sb, sc} = {sa, sb, sc} + 1;
        $display($time, "{sa, sb, sc}:%d", {sa, sb, sc});
    end
    #100 $finish(1);
end
```

```
initial
begin
    {sa, sb, sc} = 3'b000;
    for(integer i=0;i<7;i=i+1)
    begin
        #100 {sa, sb, sc} = {sa, sb, sc} + 1;
    end
    #100 $finish(1);
end
```

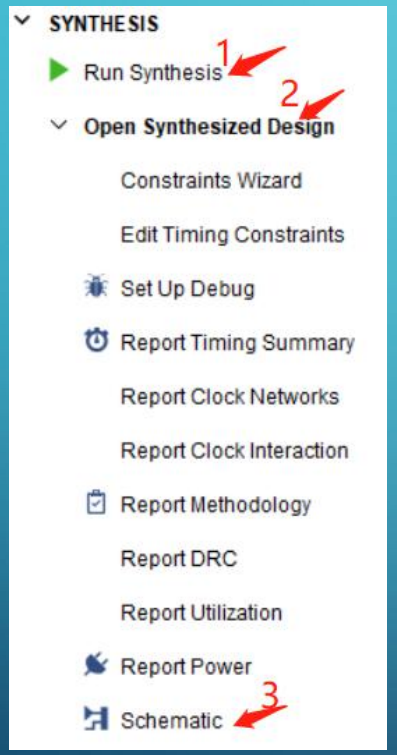
```
initial
begin
    {sa, sb, sc} = 3'b000;
    while({sa, sb, sc}<3'b111)
    begin
        #100 {sa, sb, sc} = {sa, sb, sc} + 1;
    end
    #100 $finish(1);
end
```

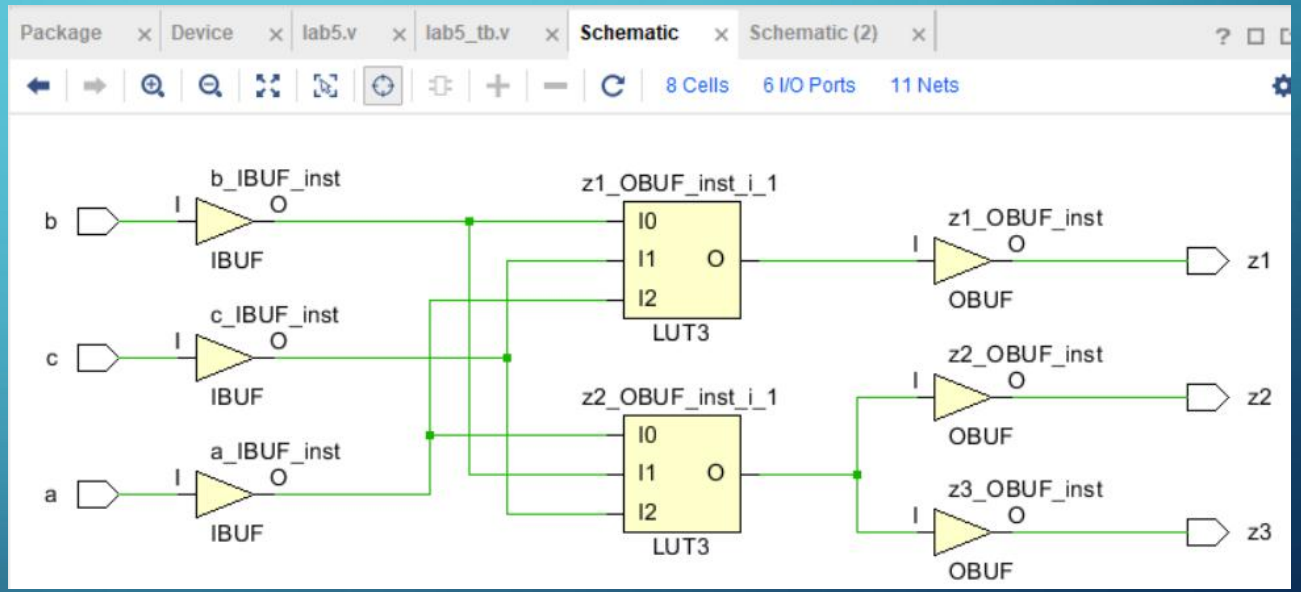
SCHEMATIC IN ‘RTL ANALYSIS’





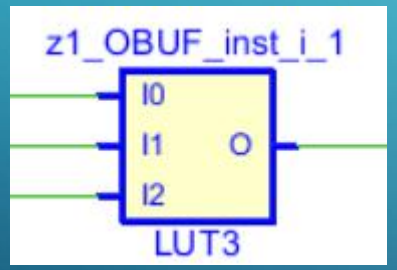
SCHEMATIC OF SYNTHESIZE(1)

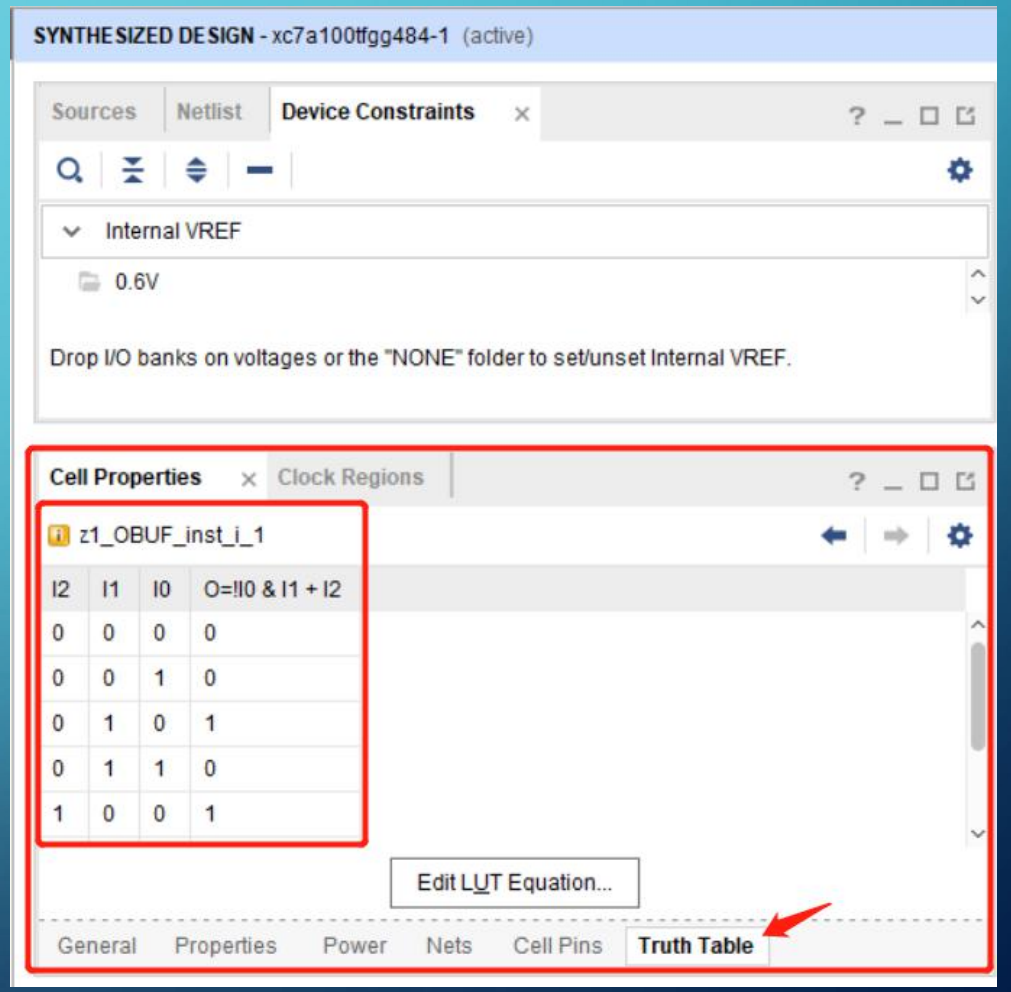




SCHEMATIC OF SYNTHESIZE(2)

- Double click the LUT in schematic window
- In the Cell Properties window , choose “Truth Table” , you can find the truth table of the cell





USING DISPLAY ,WRITE, MONITOR TO DISPLAY THE VALUE

- $display is a system task, not Synthesizable
- Please try $write and $monitor separaterly

```
initial
begin
    {sa, sb, sc} = 3'b000;
    repeat(7)
    begin
        #100 {sa, sb, sc} = {sa, sb, sc} + 1;
        $display($time, "{sa, sb, sc}:%d", {sa, sb, sc});
    end
    $finish(1);
end
```

```
# run 1000ns
100{sa, sb, sc}:1
200{sa, sb, sc}:2
300{sa, sb, sc}:3
400{sa, sb, sc}:4
500{sa, sb, sc}:5
600{sa, sb, sc}:6
700{sa, sb, sc}:7
$finish called at time : 700 ns :
```

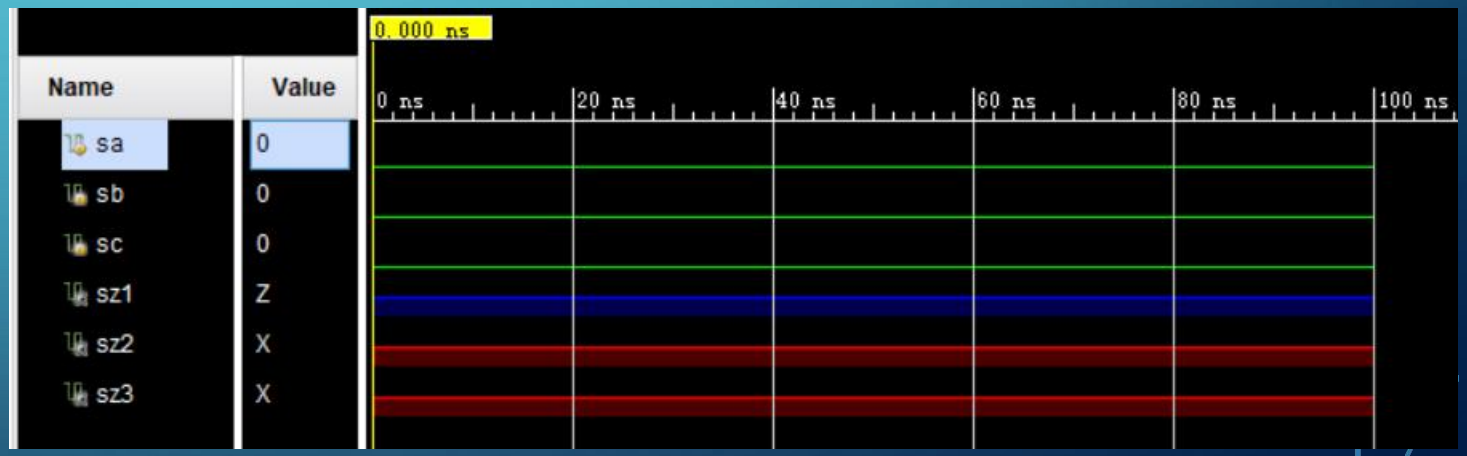
PRACTICES(1)

Do the simulation on lab5Tb which is the testbench of lab5, it is found that the wavefor is not in line with expectations:

1) sa, sb and sc keep 0 in the simulation, why ?
2) sz1 is Z, while the state of sz2 and sz3 is X, why?

modify to make it workable and test the function of module lab5

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////
21  module lab5Tb( );
22  reg sa,sb,sc;
23  wire sz1,sz2,sz3;
24  lab5 ulab5(sa,sb,sz1,sz2,sz3);
25  initial begin
26      {sa,sb,sc}=3'b000;
27      repeat(7);
28      begin
29          #100 {sa,sb,sc} = {sa,sb,sc}+1;
30          $display($time,"sa,sb,sc:%d",{sa,sb,sc});
31      end
32      $finish(100);
33  end
34  endmodule
```



PRACTICES(2)

Implement the digtial logic circuit and test its function: F(x,y,z) = x^y^z

- Using data flow to Realization of circuit design in SOP and POS style respectively
- Write the testbench in Verilog to verify the function of design
- Check the Schematic of synthesize and RTL analysis respectively to see the difference between two schematics
- Generate the bitstream and program the device to test the function