DIGITAL DESIGN

LAB1　USING VIVADO + MINISYS/EGO1

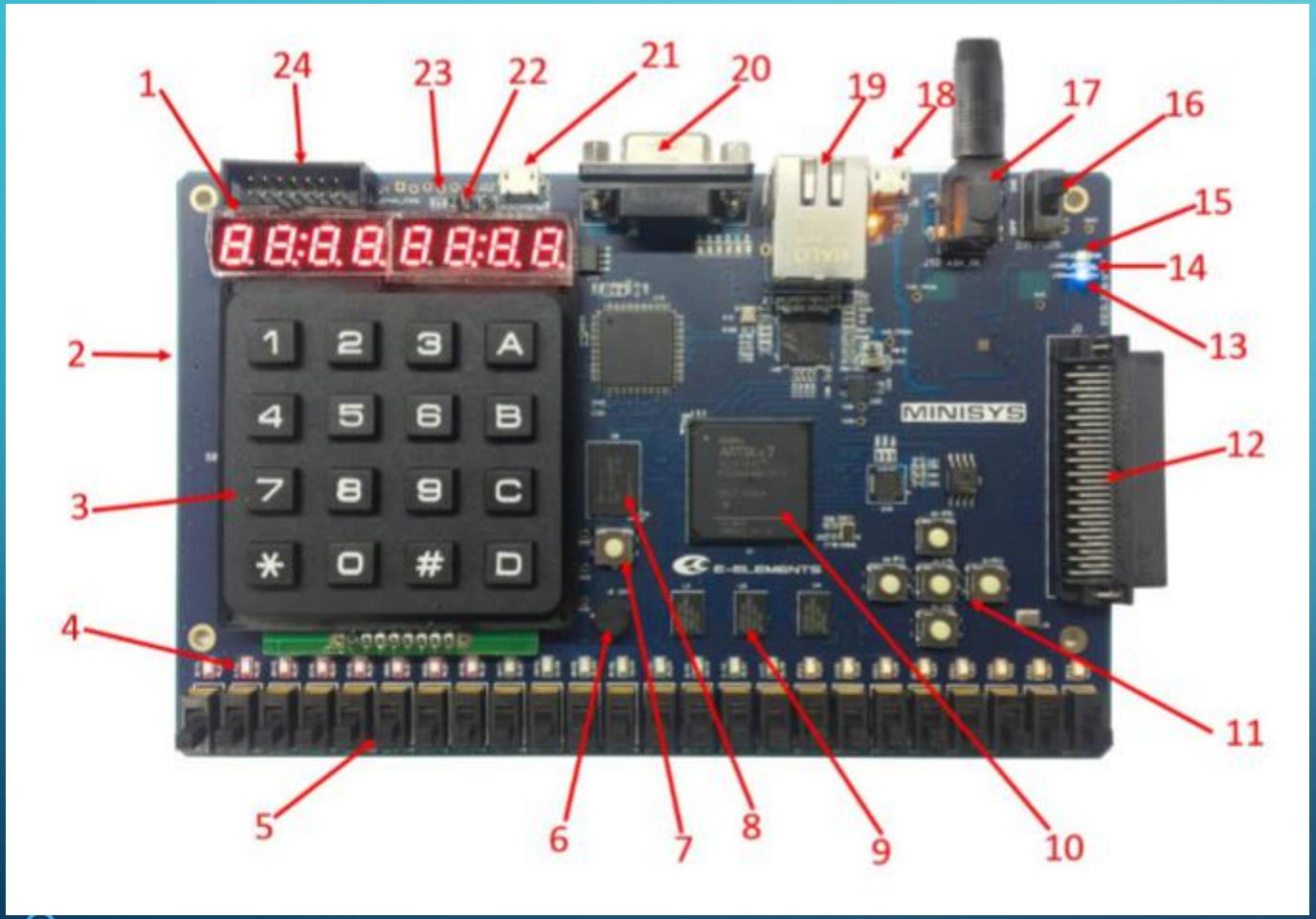
2020 FALL TERM

EXPERIMENTAL SUITE: VIVADO 2017 + MINISYS

- vivado 2017 :
  - Vivado is a design environment for FPGA products from Xilinx, and is tightly-coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors.
  - Vivado enables developers to synthesize (compile) their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.
  - The version we choose is vivado 2017

- Installation of vivado (20 G free hard disk space above is suggested)
  - Attention: the name of the directory which includes installation package MUST NOT containing Chinese character

MINISYS INSIDE



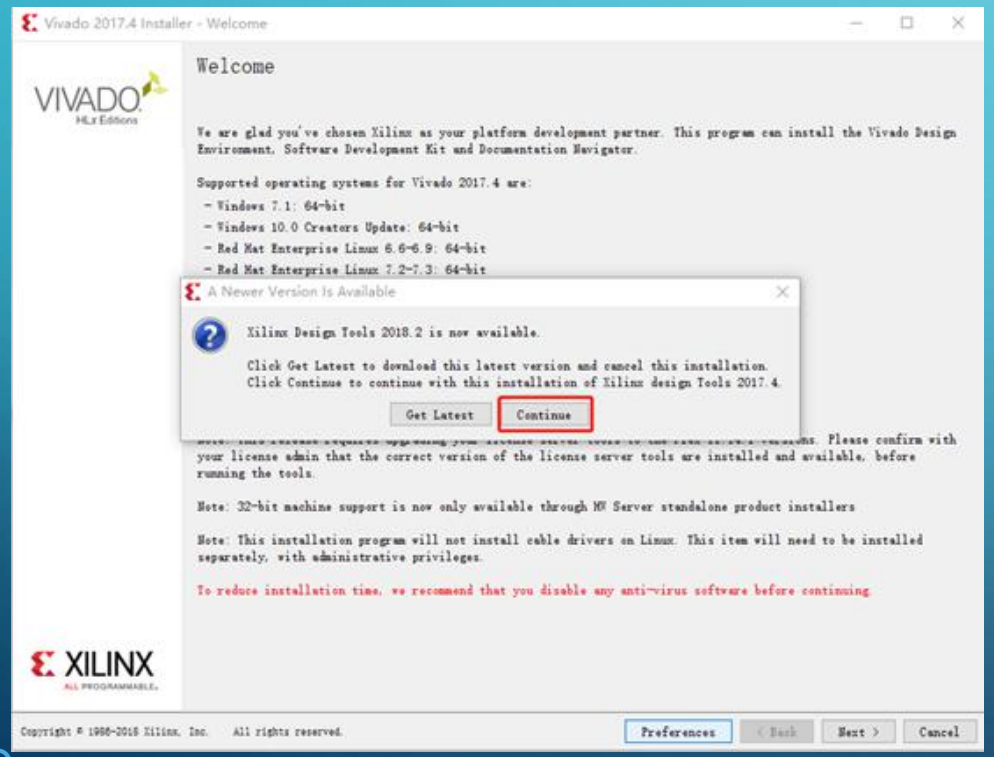
- **Artix 7 fpga chip** (10)
- Minisys soc system inside
- Power interface (17)
- USB-jtag interface (21)
- **Dial switch** *24 (5)
- **LED** *24 (4)
- SRAM (9)
- **Mini keyboard** (3)
- **seven-segment digital tube** (1)

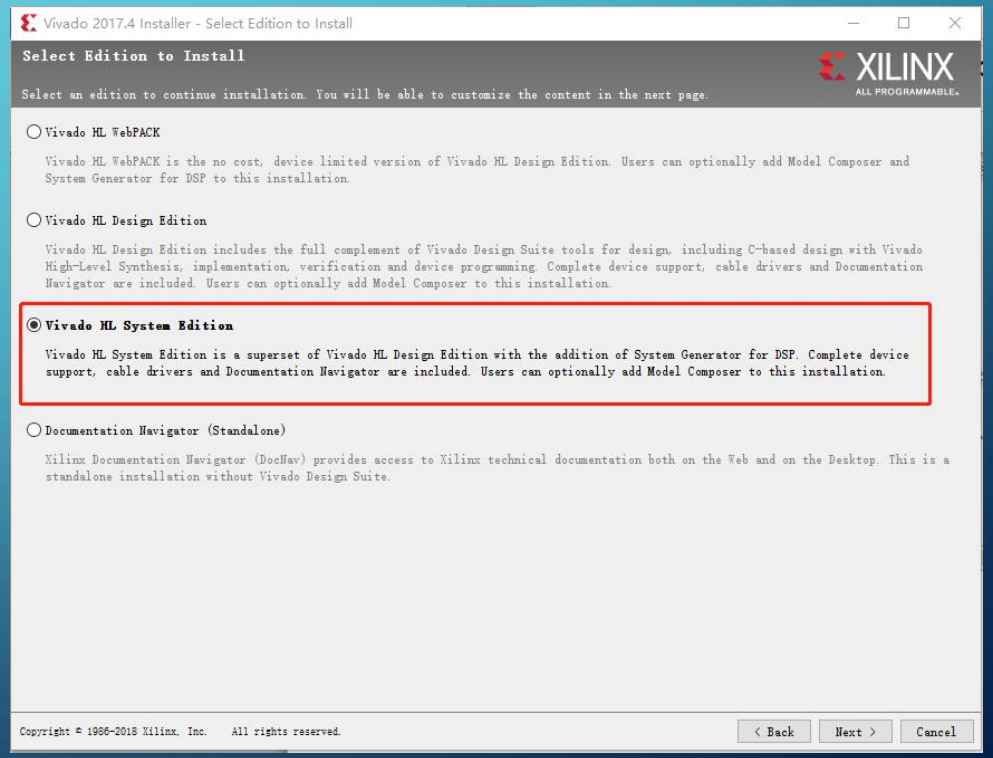
VIVADO(2017.4) INSTALLATION （TIPS1）

https://sustc.hguandl.com/download/Vivado/

ftp://10.20.118.226/ account: ftp-d-logic password: ggsddu

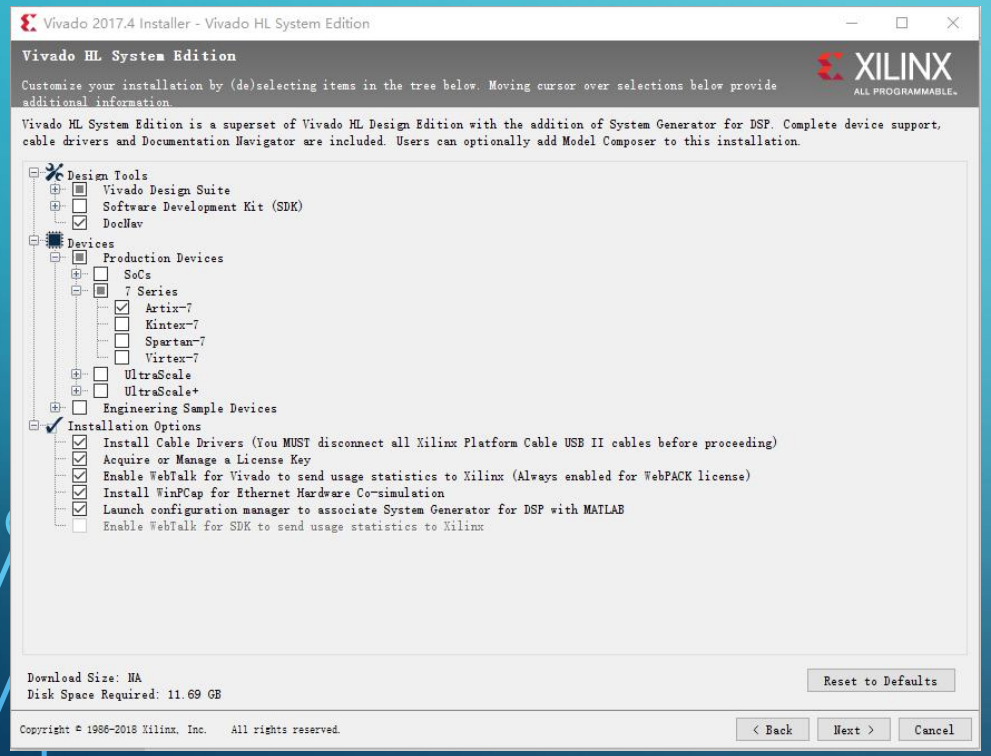
xsetup



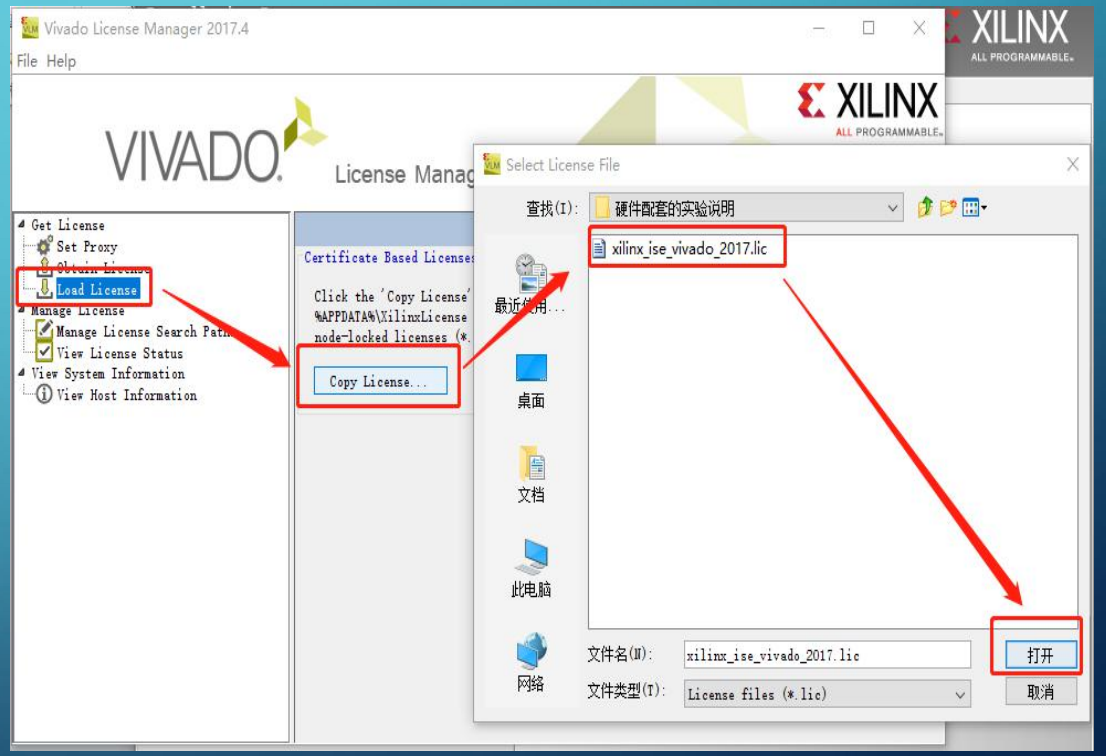


VIVADO INSTALLING （TIPS2）

Select only what is needed

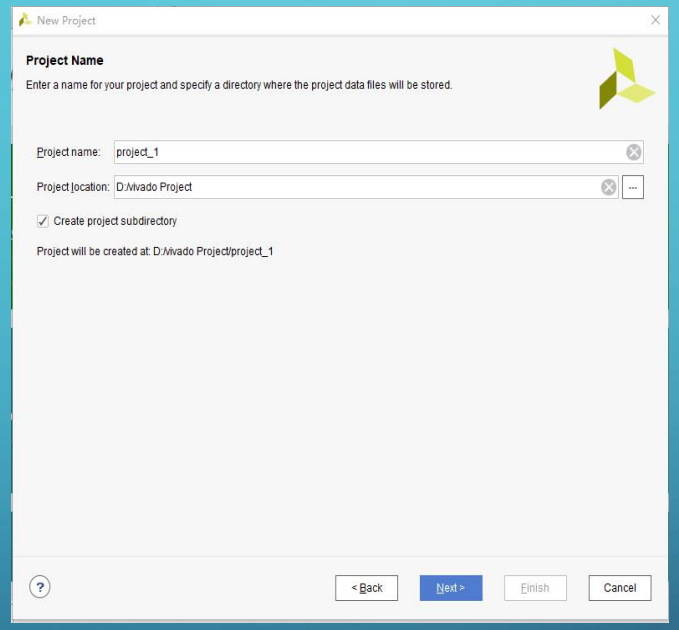


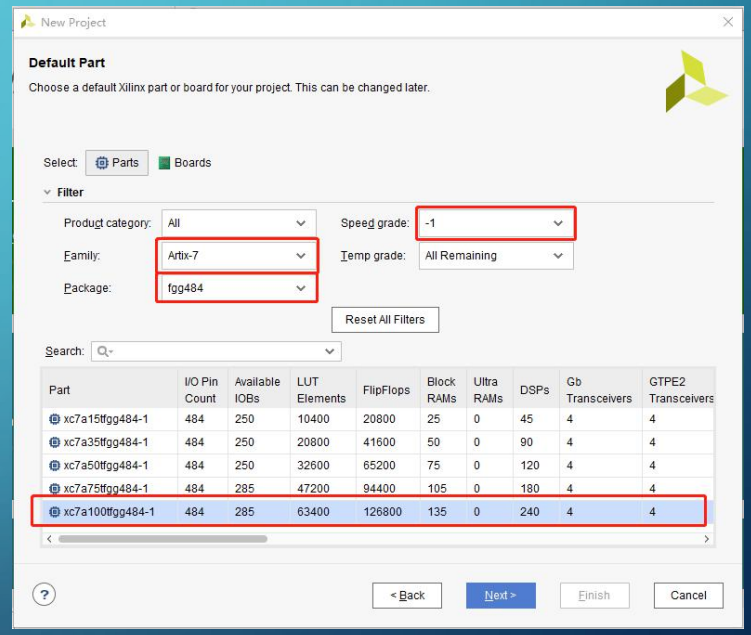
At the end of installing, load license



LAB1 USING VIVADO + MINISYS

1. Create project , select “rtl type” , select the corresponding FPGA chip name



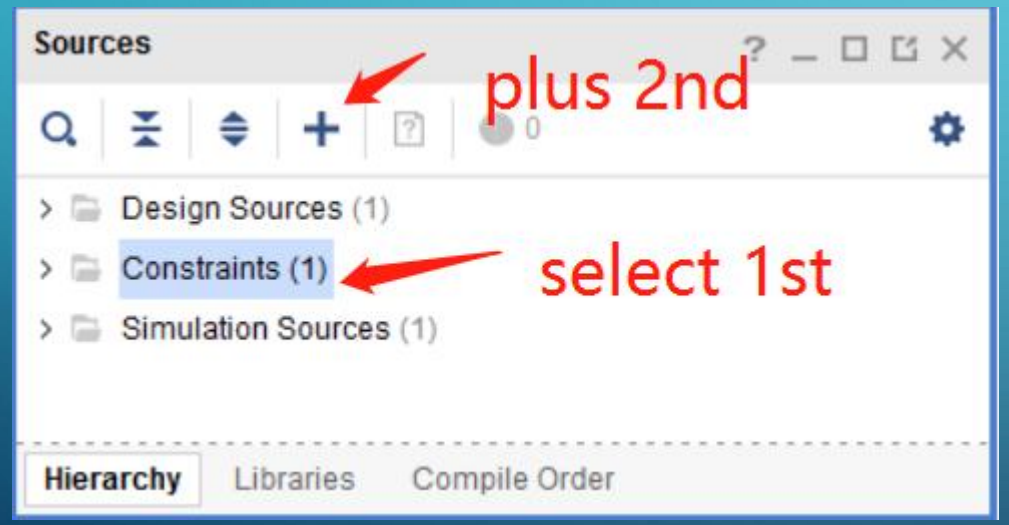


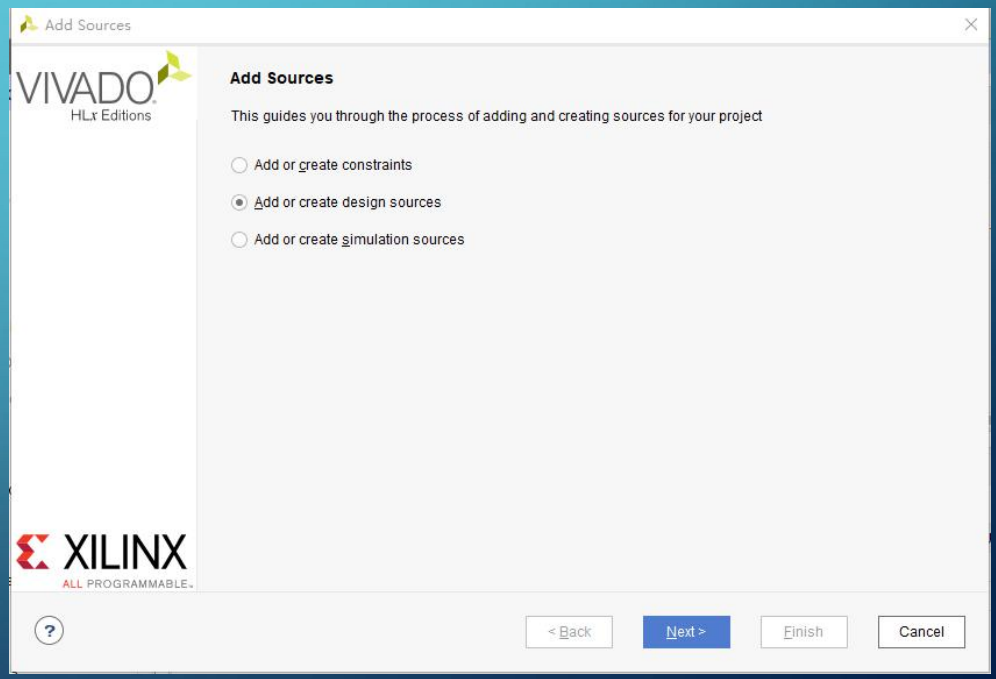
tips: FPGA Chip(Artix 7 xc7a100tfgg484-1) is embedded in Minisys board

FPGA Chip(Artix 7 xc7a35t-1CSG324-1) is embedded in EGO1 board

LAB1 USING VIVADO + MINISYS

2. Adding source file ,simulation file and constraints file





LAB1 USING VIVADO + MINISYS

- 3.following the steps to verify the function and generate bitstream file which is used to program FPGA chip
  - 1）Do the simulation to verify the function of the designed Circuit
  - 2）After simulation ,there will be a waveform which records the states of circuit's input and output signals
  - 3）if the function of circuit is ok , run synthesis ,then run implements
  - 4) after implementation is finished, Generate Bitstream , there will be a .bit file which will be used to program device

LAB1 USING VIVADO + MINISYS

- 4. connect minisys board with PC
  - USB JTAG interface for Minisys new version board
  - USB typeC interface for Minisys new version board/EGO1
- 5. turn on the minisys board
- 6. using the “open target ” to connect the vivado project with minisys board

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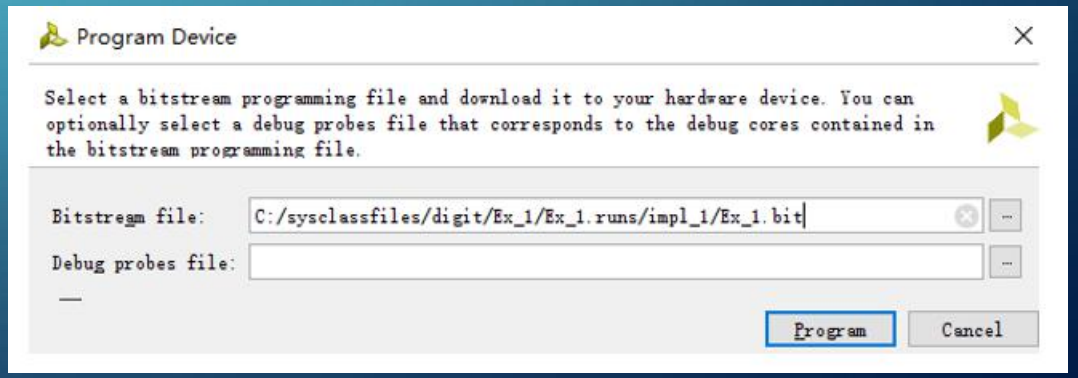
- 7. right click “program device”, then choose the device name.
- 8. select the bitstream file ,click “program” button.
- 9. while the the led of “Done” on minisys is on, it means the bit file is written into the device.
- Do the testing on the minisys board.



TESTING 24 INPUTS AND 24 OUTPUTS CIRCUIT

src1.v

src1_sim.v

ex1.xdc

tips:
while using Minisys **old** version board, connect its USB-Jtag interface to with the computer which run vivado project by typeB USB wire.

whille using Minisys **new** version board, connect its typeC interface to with the computer which run vivado project by typeC USB wire.