DIGITAL DESIGN

ASSIGNMENT 2

Deadline: *22:30, Wednesday 11 November 2019*

Lab sessions & Location:

1. **Lychee Garden 6, Room 406 (Wednesday 16:20-18:10 pm)**
2. **Lychee Garden 6, Room 408 (Wednesday 19:00-20:50 pm)**
3. **Lychee Garden 6, Room 402 (Thursday 8:00-9:50 am)**
4. **Lychee Garden 6, Room 402 (Thursday 10:10~12:10 am)**

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PART 1: DIGITAL DESIGN THEORY

Provide answers to the following questions:

1. Given the Boolean functions F1 and F2, show that
    a. The Boolean function E = F1 + F2 contains the sum of the minterms of F1 and F2
    b. The Boolean function G = F1 · F2 contains only the minterms that are common to F1 and F2 .
2. Convert each of the following to the other canonical form.
    a. F(x, y, z) = ∑(1, 3, 7)
    b. F(A, B, C, D) = ∏(1, 3, 5, 8, 11, 13, 15)
3. Write the following Boolean expressions in:
    a. (b’ + d)(a’+ b’+ c)(a + c) SOP form
    b. ab + a’c’+ bc POS form
4. Determine whether the following Boolean equation is true or false. Show your process.
    a. y’z’ + yz’ + x’z = x’z’
    b. x’y’+ x’z’+ yz = x’y + x’z
5. Simplify the following Boolean functions and expressions, using four-variable maps:
    a. F (A, B, C, D) = ∑ (0, 2, 5, 7, 8, 10, 13, 15)
    b. F (w, x, y, z) = ∑ (1, 3, 4, 5, 6, 7, 9, 11, 13, 15)
    c. A’BCD + ABC + CD + B’D
    d. A’B’C’D’ + BC’D + A’C’D + A’BCD + ACD
6. Implement the following logical functions with two-level NOR gate circuits. Write down the simplification process, then draw the circuit diagram.
    a. F(A, B, C, D) = AD + BC’D+ ABC + A’BC’D
    b. F(A, B, C, D)= (A’+ C’+ D’)(A’+ C’)(C’+ D’)
7. Simplify the following Boolean function F, together with the don’t-care conditions d, and then express the simplified function in sum-of-minterms form:
    a. F(x, y, z) = ∑(0, 1, 4, 5, 6) with d(x, y, z)= ∑(2, 3, 7)
    b. F(A, B, C, D) = ∑(5, 6, 7, 12, 14) with d(x, y, z)= ∑(3, 9, 11)

8. Implement the following Boolean expression with exclusive-OR and AND gates, draw the circuit diagram: F = AB'CD' + A'BCD' + AB'C'D + A'BC'D

PART 2: DIGITAL DESIGN LAB

INTRODUCTION

In this lab, you are required to use Vivado 2017.4 and Minisys Practice platform (xilinx FPGA chip artix 7 inside) to design a combinational logic circuit and test it.

PREAMBLE

Before working on the coursework itself, you should master the following material.

1.'Ch2-Boolean Algrebra-ICs-SUSTC.ppt' and 'CH3-Minimisation-SUSTC' in Sakai site.

2. 'Digital design lab5', 'Digital design lab6' and 'Digital design lab7' in Sakai site.

3. Verilog: http://www.verilog.com

EXERCISE SPECIFICATION

TASK1:

There are 16 wards, which are numbered from 0 to F respectively, among which the #0 ward has the lowest priority, and the #F has the highest priority (Priority increases as the number increases). Each room has a call bell, it can be turn on and turn off. In the main control room there is a 7-seg tube which shows the ID of the room whose bell is on with the highest priority.

Write a circuit to realize this function and test.

The circuit should get the info of wards whose call bell is on and light One 7-seg tube to show the ID of room whose bell is on with the highest priority.

- Do the design.
- Create the constraint file.

- Do the synthetic and implementation, generate the bitstream file and program the device, then test on the Minisys develop board.
- While Testing the circuit, at least three test scenarios need to be considered:
    i. Only one ward's call bell is turned on
    ii. Two or more wards whose call bell is turned on
    iii. There is no ward whose call bell is turned on //NOTICE: This test scenarios should be distinguished from #0 ward's call bell is turned on.

TASK2:

Implement the circuit and test its function: F(a,b,c,d) = a^b^c^d

- Write its true-table and K-map, using K-map to simplified the circuit if possible.
- Using data flow to Realization of circuit design in SOP and POS style respectively
- Write testbench in Verilog and do the simulation to verify the function of design

SUBMISSION

Submit your assignment report to the Sakai on *Corresponding site* "CS207-Prof.G" by the deadline.

ASSESSEMENT

The full marks for this exercise is 100 and they are distributed as follows:

Theory: 40%

Question 1	4
Question 2	4
Question 3	4
Question 4	4

Question 5	8
Question 6	8
Question 7	4
Question 8	4
Total	40 marks

Lab: 60%

Task 1: Design in Verilog	5 marks
Task 1: Constrains file	5 marks
Task 1: photos about test result on Minisys practice board and description on inputs and outputs. 3 test at least	5*3 marks
Task 2: truth-table and K-map of the circuit	5*2 marks
Task 2: Design in Verilog in data flow style with SOP and POS in one module	5*2
Task 2: Test bench in Verilog, simulation result and its description	5*2 marks
Problem and solution. if there is no problem, suggestions or solutions is asked.	5 marks
Total	60 marks