
# DIGITAL DESIGN

# ASSIGNMENTREPORT

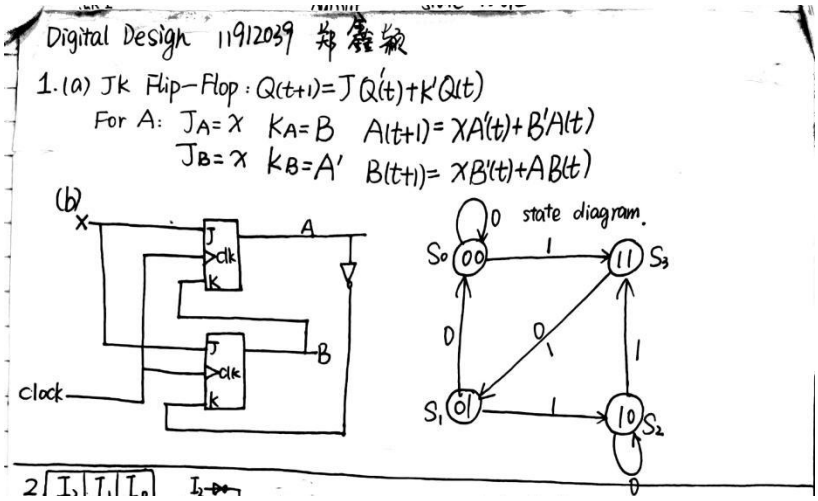
# ASSIGNMENT ID : IV

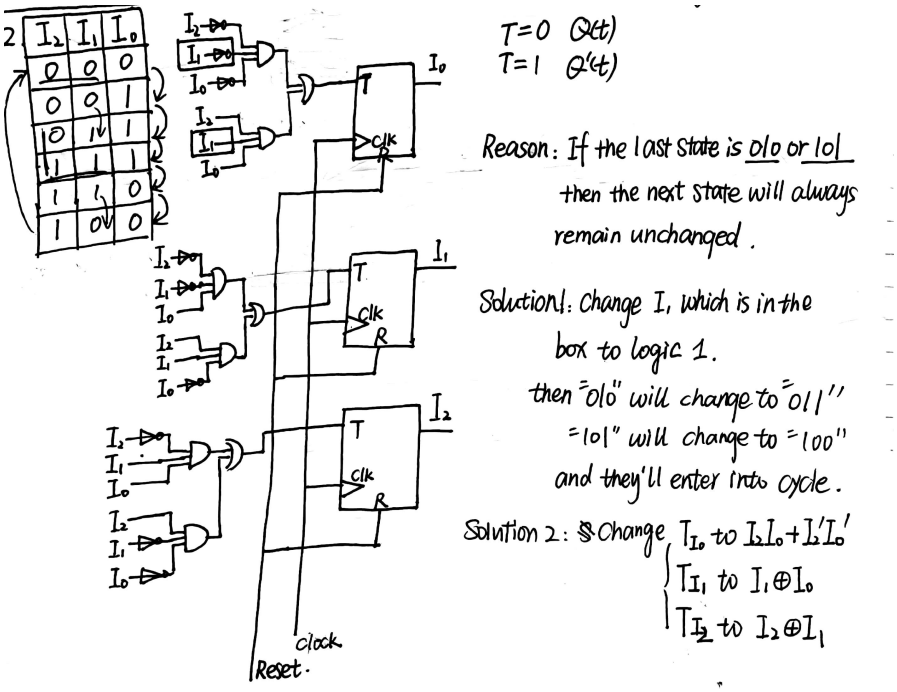
**Student Name:**郑鑫颖

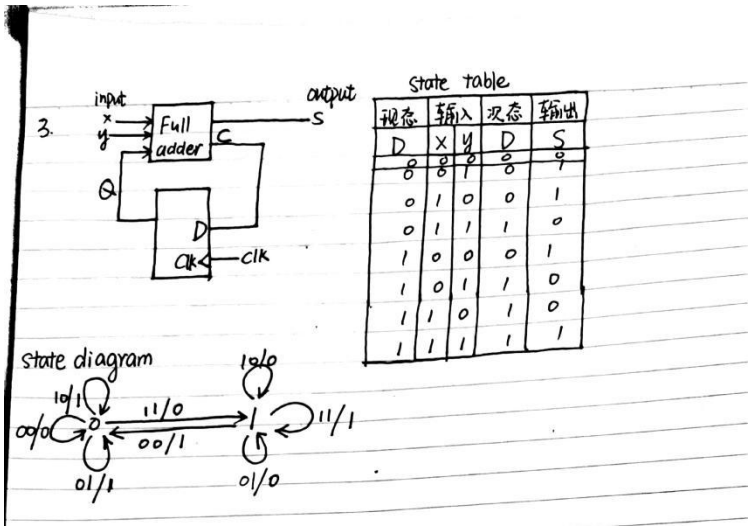
**Student ID: 11912039**

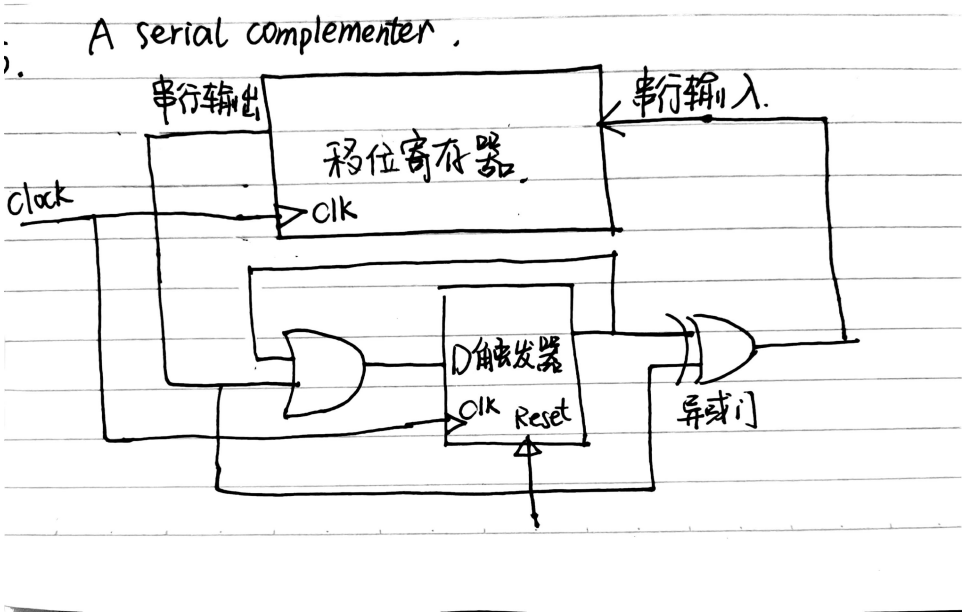
## PART 1: DIGITAL DESIGN THEORY

Provide your answers here:






## PART 2: DIGITAL DESIGN LAB (TASK1)

### DESIGN

*Describe the design of your system by providing the following information:*

- *Verilog design (provide the Verilog code)*
- *Truth-table*

### SIMULATION

*Describe how you build the test bench and do the simulation.*

- *Using Verilog(provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation.*

## CONSTRAINT FILE AND THE TESTING

*Describe how you test your design on the Minisys Practice platform.*

- *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
- *The testing result (provide the screen shots (at least 3 testing scene) to show state of inputs and outputs along with the related descriptions.*

## THE DESCRIPTION OF OPERATION

*Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.*

- *Problems and solutions*

# PART 2: DIGITAL DESIGN LAB (TASK2)

## DESIGN

*Describe the design of your system by providing the following information:*

- *Verilog design while using data flow (provide the Verilog code)*
- *Verilog design while using structured design (provide the Verilog code)*
- *Block design (provide screen shots)*
- *Truth-table*

## SIMULATION

*Describe how you build the test bench and do the simulation.*

- *Using Verilog (provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation*

## CONSTRAINT FILE AND THE TESTING

*Describe how you test your design on the Minisys Practice platform.*

- *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
- *The testing result (provide the screen shots (at least 3 testing scene)) to show state of inputs and outputs along with the related descriptions.*

## THE DESCRIPTION OF OPERATION

*Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.*

- *Problems and solutions*