
# DIGITAL DESIGN

# ASSIGNMENTREPORT

# ASSIGNMENT ID : II

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## PART 1: DIGITAL DESIGN THEORY

Provide your answers here:

Part I:

~~1. a: E = F1 + F2 is true when F1~~

1. a: assume that $F_1 = m_{i1} + m_{i2} + m_{i3}$, $m_i$ denote the minterm of $F_1$

$F_2 = m_{j1} + m_{j2} + m_{j3}$, $m_j$ denote the minterm of $F_2$

a: $E = F_1 + F_2 = (m_{i1} + m_{i2} + m_{i3}) + (m_{j1} + m_{j2} + m_{j3})$

b.

b: $G = F_1 \cdot F_2 = (m_{i1} + m_{i2} + m_{i3})(m_{j1} + m_{j2} + m_{j3})$

$= \sum m_{ix} m_{jy}$

if $m_{ix} = m_{jy}$ then $m_{ix} m_{jy} = m_{ix}$

if $m_{ix} \neq m_{jy}$ then $m_{ix} m_{jy} = 0$

So $G = F_1 \cdot F_2 = \sum m_{ix}$, when $m_{ix}$ is the common minterm of $F_1, F_2$.

2. a: $F(x,y,z) = \Sigma(1,3,7) = \pi(0,2,4,5,6)$.

$F(A,B,C,D) = \pi(1,3,5,8,11,13,15) = \Sigma(0,2,4,6,7,9,10,12,14)$

3. a: $(b'+d)(a'+b'+c)(a+c)$

$= (a+b'+c+d)(a'+b'+c+d)(a+b'+c'+d)(a'+b'+c'+d)$
$(a'+b'+c+d)(a'+b'+c+d')(a+b+c+d)(a+b'+c+d)$
$(a+b+c+d')(a+b'+c+d')$

$= (a+b'+c+d)(a'+b'+c+d)(a+b'+c'+d)(a'+b'+c'+d)$
$(a'+b'+c+d')(a+b+c+d)(a+b+c+d')(a+b'+c+d')$

$= \pi(4,12,6,14,13,0,1,5)$

$= \pi(0,1,4,5,6,12,13,14) = \Sigma(2,3,7,8,9,10,11,15)$

$= a'b'cd' + a'b'cd + a'bcd + ab'c'd' + ab'c'd + ab'cd' + ab'cd$
$+ a'b'c'd' + abcd = cd + ab' + b'cd' = cd + ab' + b'c$

b.

| a | b | c | F |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 ← |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 ← |
| 1 | 0 | 1 | 0 ← |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

$F = ab + a'c' + bc$

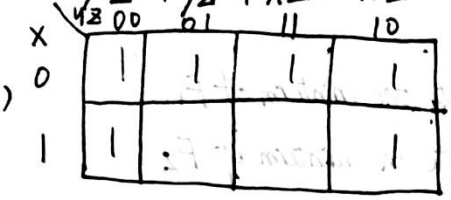
$= \pi(M_1, M_4, M_5)$

$= (a+b+c')(a'+b+c)(a'+b+c')$

$= (a+b+c')(a'+b)$

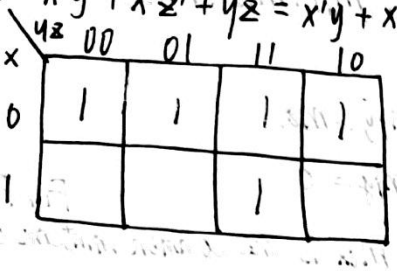
4: $y'z' + yz' + x'z = x'z'$

(a)



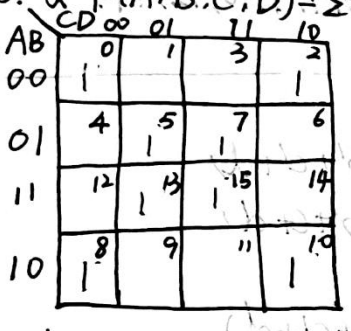

from the karnaugh Map
we know that
$y'z' + yz' + x'z = z' + x' \neq x'z'$
So the Boolean equation is False.

(b) $x'y' + x'z' + yz = x'y + x'z$

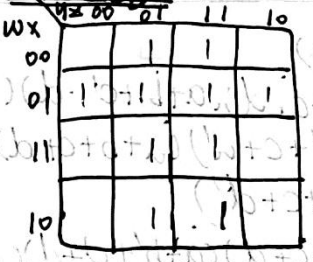



From the karnaugh Map
we know that
$x'y' + x'z' + yz = x' + yz$
$= (x' + y)(x' + z) \neq x'y + x'z$
So the Boolean equation is False.

5. a. $F(A,B,C,D) = \Sigma(0,2,5,7,8,10,13,15)$




$= BD + B'D'$

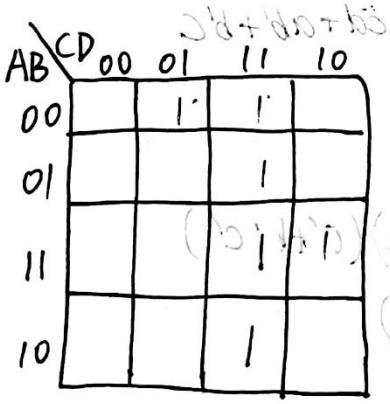


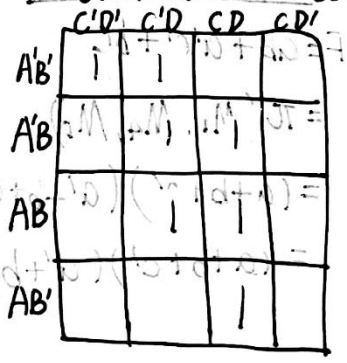

b. ~~$F(x,y,z,w)$~~ $F(w,x,y,z) = \Sigma(1,3,4,5,6,7,9,11,13,15)$

$= z + w'x$

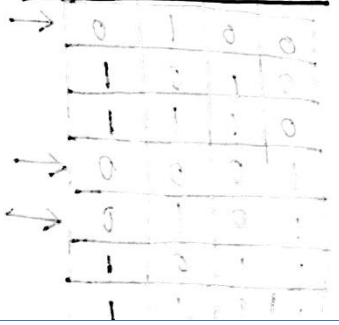
c. $A'BCD + ABC + CD + B'D = CD + B'D + ABC$

d: $A'B'C'D' + BC'D + A'C'D + A'BCD + ACD$



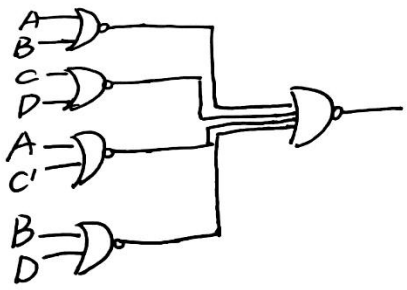




$= BD + A'B'C' + ACD$

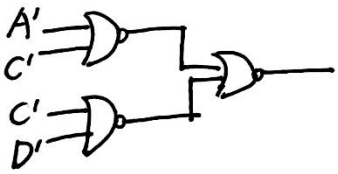


6. (a) $F(A,B,C,D) = AD + BC'D + ABC + A'BC'D$

$= (A+B)(C+D)(A+C')(B+D)$




(b) $F(A,B,C,D) = (A'+C')(C'+D')$




7. 2: $F(x,y,z) = \Sigma(0,1,4,5,6)$ $d(x,y,z) = \Sigma(2,3,7)$

| x \ yz | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 (0) | 1 (1) | x (3) | x (2) |
| 1 | 1 (4) | 1 (5) | x (7) | 1 (6) |

$\therefore F(x,y,z) = 1$ (with don't care condition)

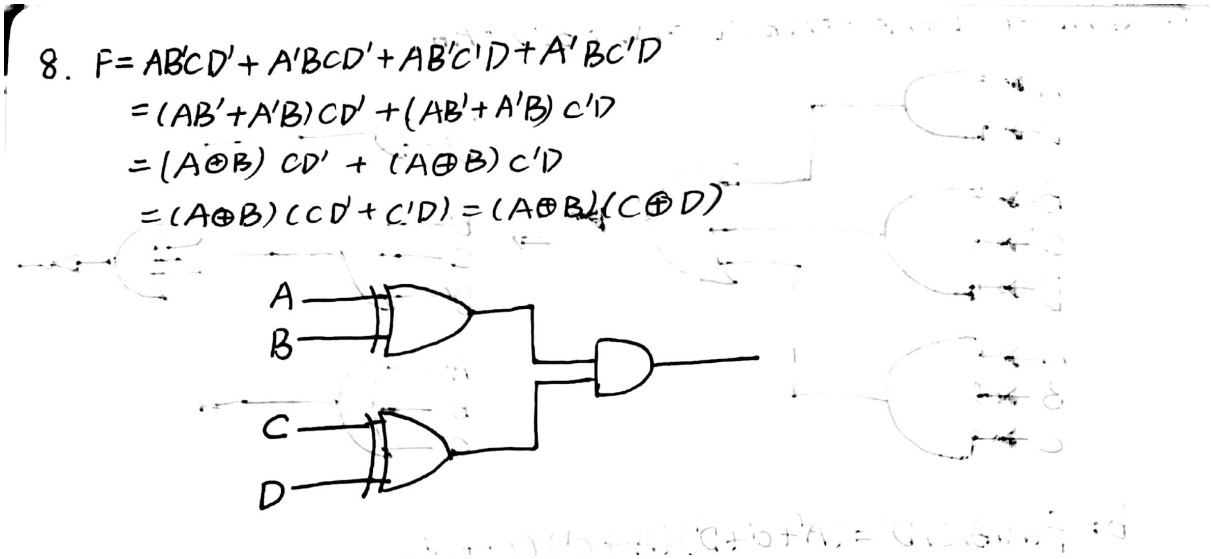
$= \Sigma(0,1,2,3,4,5,6,7)$

b: $F(A,B,C,D) = \Sigma(5,6,7,12,14)$ with $d^{A,B,C,D}_{(x,y,z)} = \Sigma(3,9,11)$

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | X (3) | 2 |
| 01 | 4 | 1 (5) | 1 (7) | 1 (6) |
| 11 | 1 (12) | 13 | 15 | 1 (14) |
| 10 | 8 | X (9) | X (11) | 10 |

$F(A,B,C,D) = A'BD + A'BC + BCD' + ABD'$

$= \Sigma(5,6,7,12,14)$




## PART 2: DIGITAL DESIGN LAB (TASK1)（已完成检查）

### DESIGN

*Describe the design of your system by providing the following information:*

- *Verilog design (provide the Verilog code)*
- *Truth-table*

### SIMULATION

*Describe how you build the test bench and do the simulation.*

- *Using Verilog (provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation.*

### CONSTRAINT FILE AND THE TESTING

*Describe how you test your design on the Minisys Practice platform.*

- *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
- *The testing result (provide the screen shots (at least 3 testing scene) to show state of inputs and outputs along with the related descriptions.*

### THE DESCRIPTION OF OPERATION

*Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.*

- *Problems and solutions*

## PART 2: DIGITAL DESIGN LAB (TASK2)

### DESIGN

*Describe the design of your system by providing the following information:*

- *Verilog design while using data flow (provide the Verilog code)*
- *Verilog design while using structured design (provide the Verilog code)*
- *Block design (provide screen shots)*
- *Truth-table*

### SIMULATION

*Describe how you build the test bench and do the simulation.*

- *Using Verilog (provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation*

### CONSTRAINT FILE AND THE TESTING

*Describe how you test your design on the Minisys Practice platform.*

- *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
- *The testing result (provide the screen shots (at least 3 testing scene)) to show state of inputs and outputs along with the related descriptions.*

## THE DESCRIPTION OF OPERATION

*Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.*

- *Problems and solutions*