

**DIGITAL DESIGN**

**ASSIGNMENTREPORT**

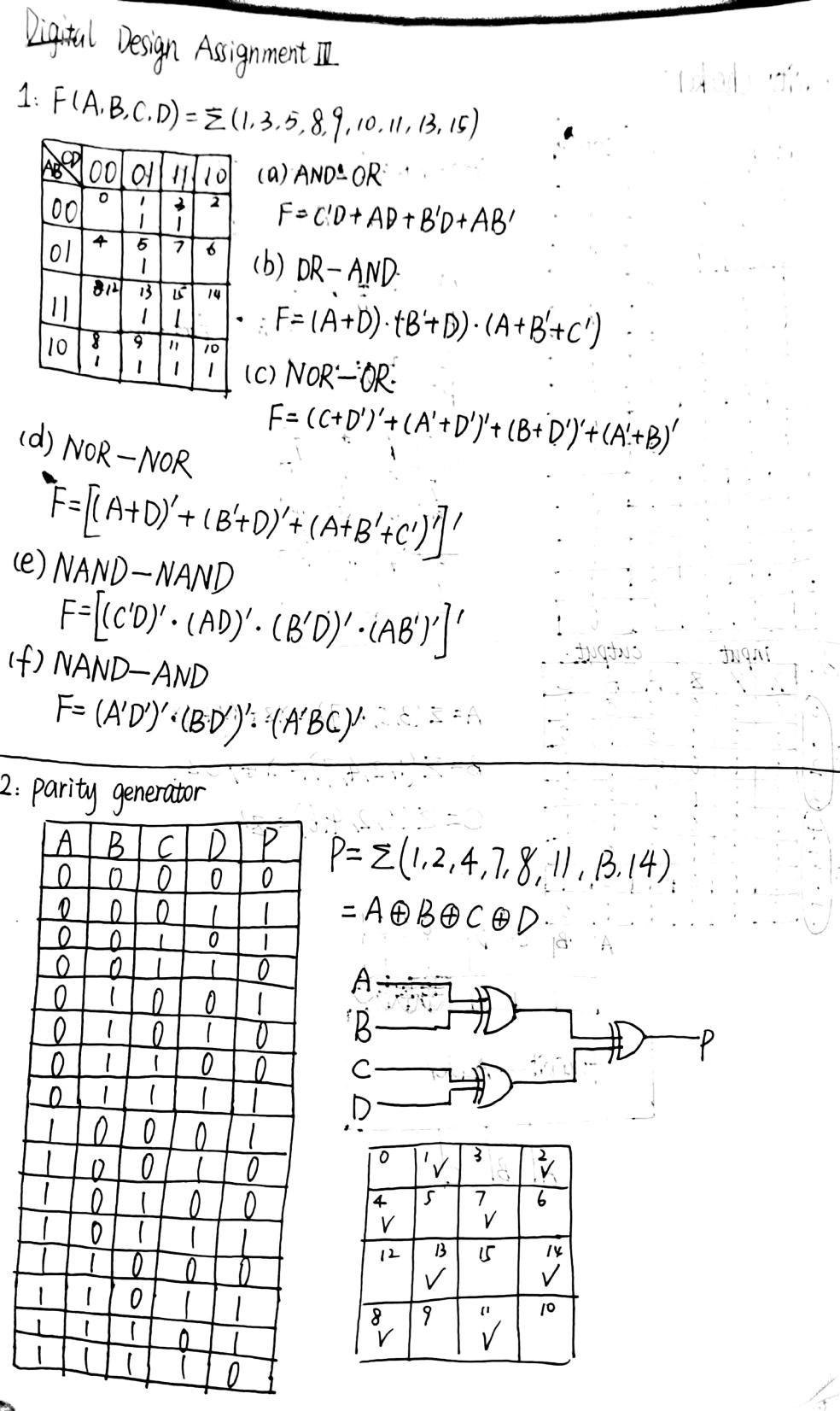
**ASSIGNMENT ID : III**

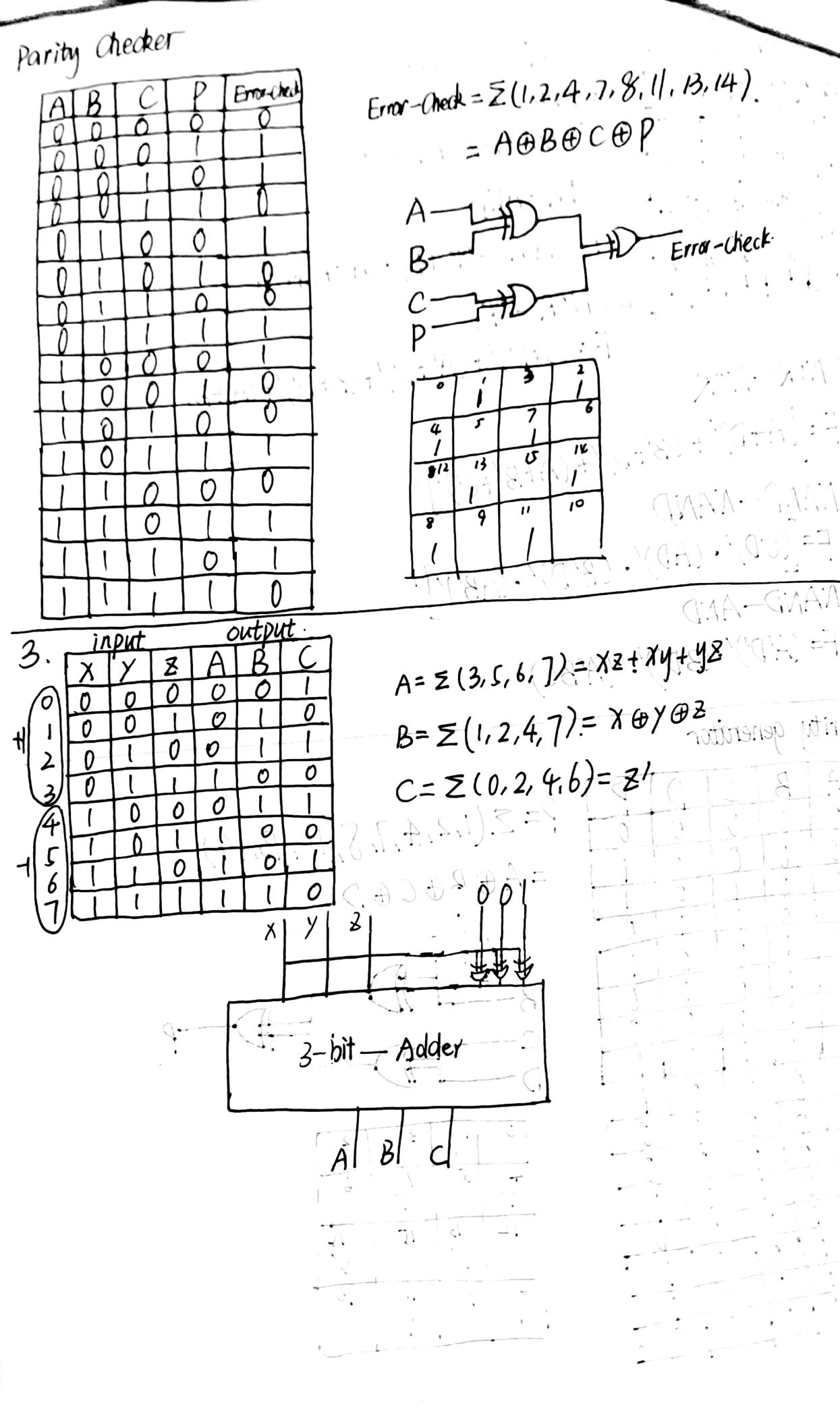
**Student Name: 郑鑫颖**

**Student ID: 11912039**

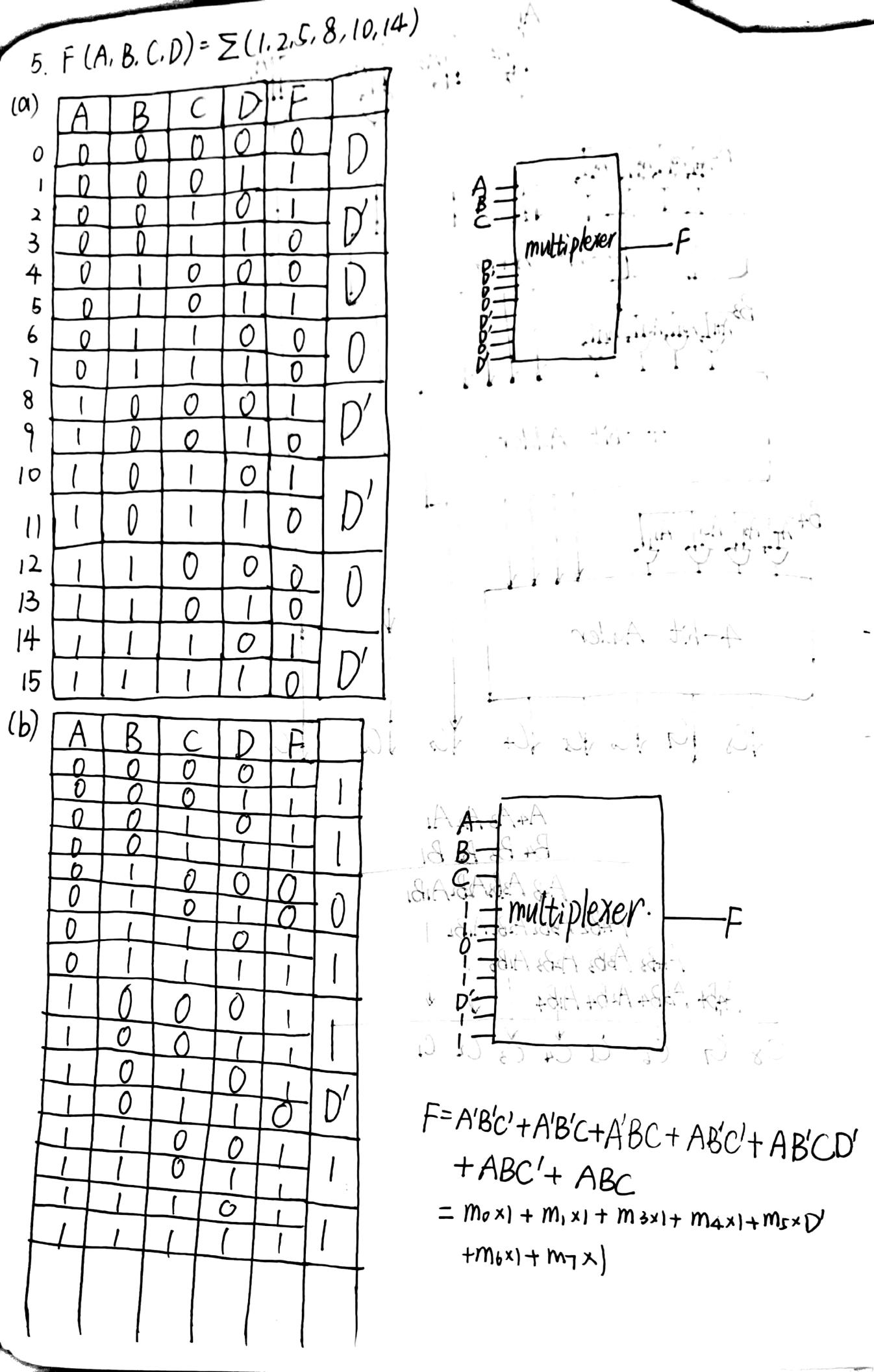
PART 1: DIGITAL design THEORY

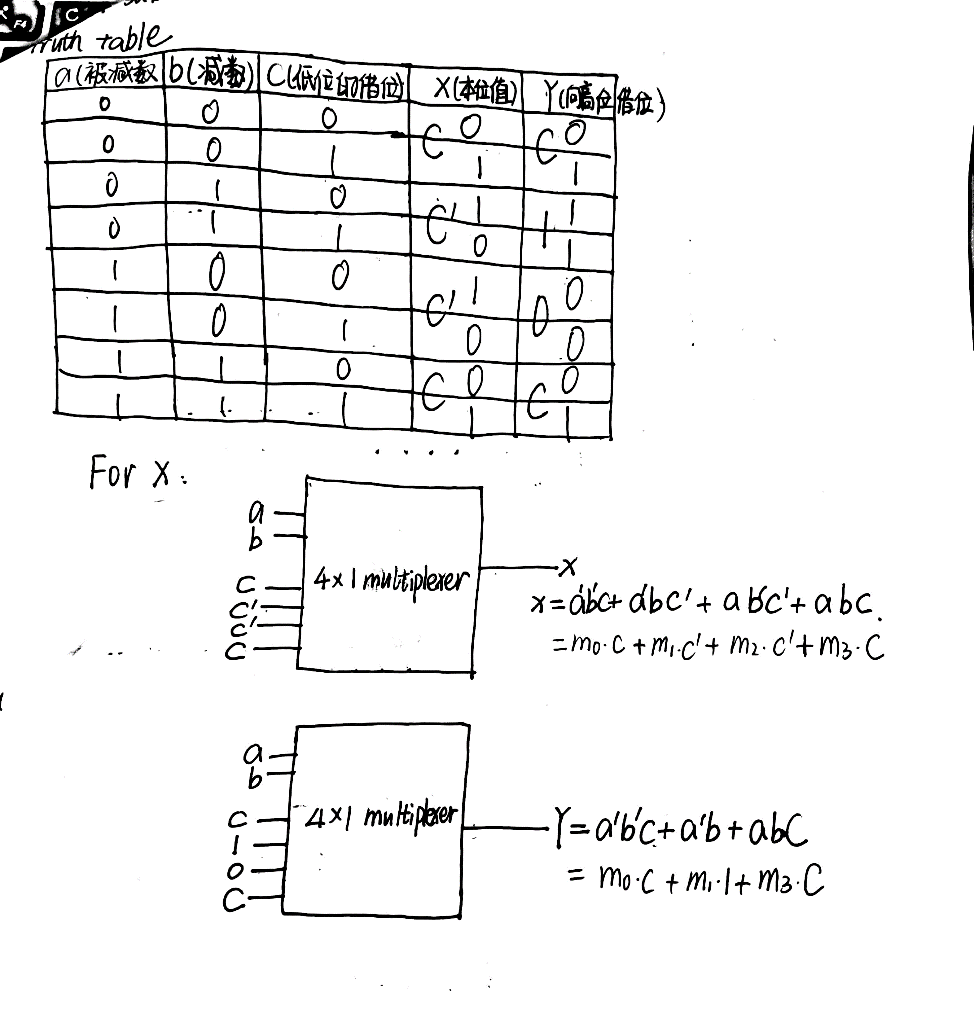
Provide your answers here:





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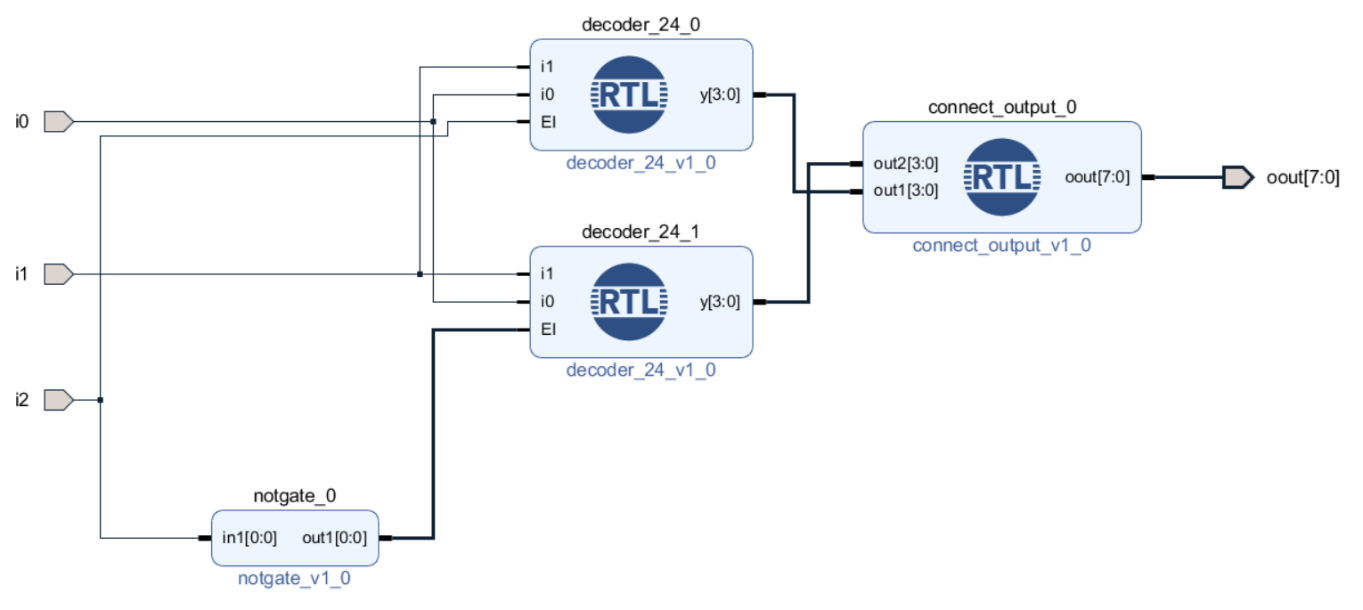
PART 2: DIGITAL design LAB (Task1)

##### Design

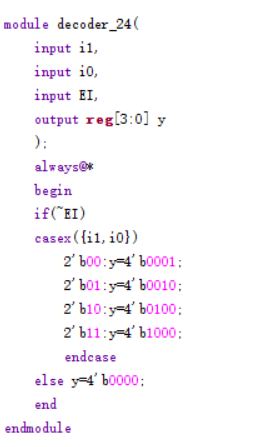
*Describe the design of your system by providing the following information:*

***3-8 decoder***

* *Verilog design (provide the Verilog code)*



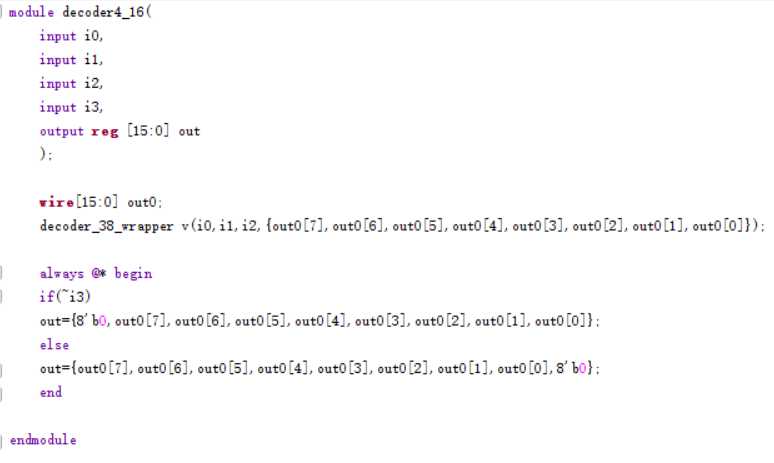
*2-4 decoder*



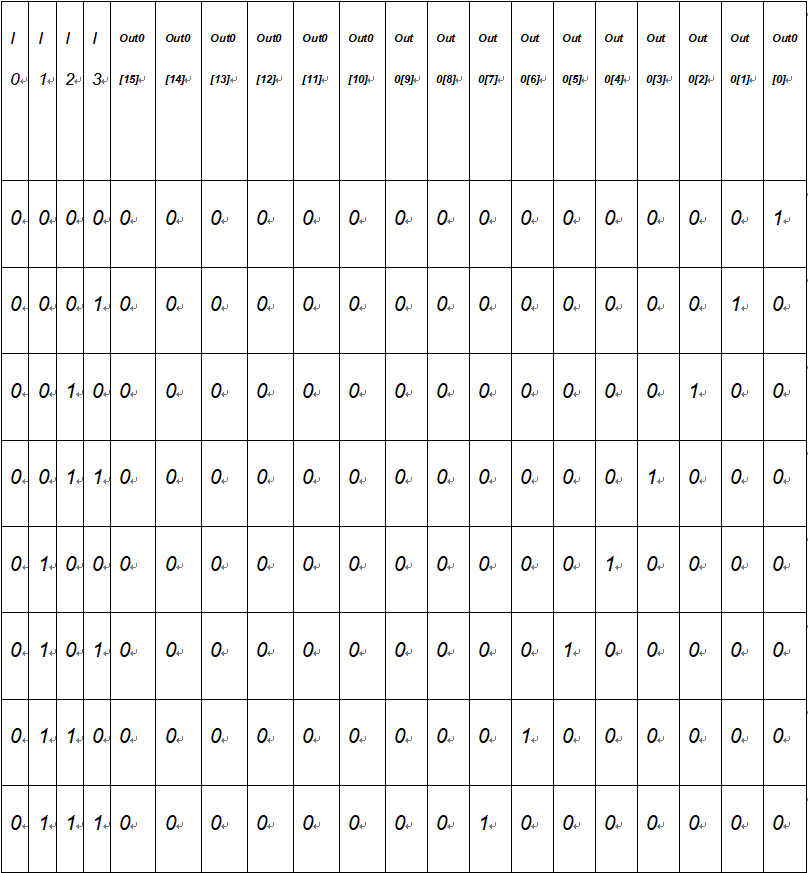
* *Truth-table for*

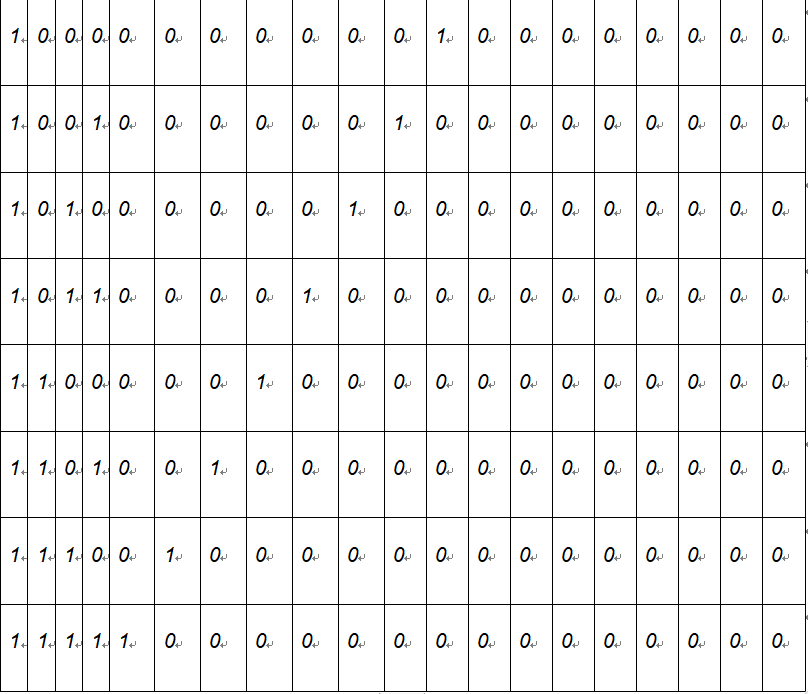
|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| *i2* | *i1* | *i0* | *oout[7]* | *oout[6]* | *oout[5]* | *oout[4]* | *oout[3]* | *oout[2]* | *oout[1]* | *oout[0]* |
| *0* | *0* | *0* | *0* | *0* | *0* | *0* | *0* | *0* | *0* | *1* |
| *0* | *0* | *1* | *0* | *0* | *0* | *0* | *0* | *0* | *1* | *0* |
| *0* | *1* | *0* | *0* | *0* | *0* | *0* | *0* | *1* | *0* | *0* |
| *0* | *1* | *1* | *0* | *0* | *0* | *0* | *1* | *0* | *0* | *0* |
| *1* | *0* | *0* | *0* | *0* | *0* | *1* | *0* | *0* | *0* | *0* |
| *1* | *0* | *1* | *0* | *0* | *1* | *0* | *0* | *0* | *0* | *0* |
| *1* | *1* | *0* | *0* | *1* | *0* | *0* | *0* | *0* | *0* | *0* |
| *1* | *1* | *1* | *1* | *0* | *0* | *0* | *0* | *0* | *0* | *0* |

*4-16 decoder*



*Truth-table for4-16*

**

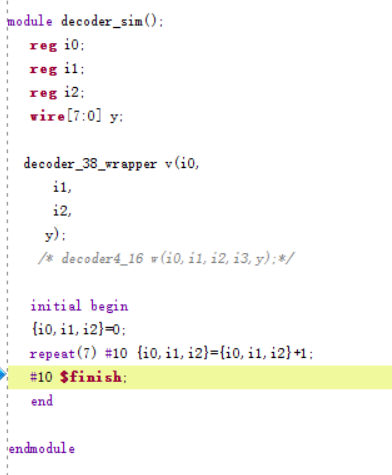
**

##### simulation

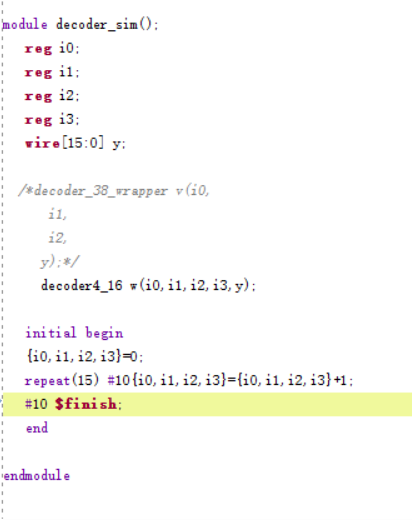
*Describe how you build the test bench and do the simulation.*

* *Using Verilog (provide the Verilog code)*

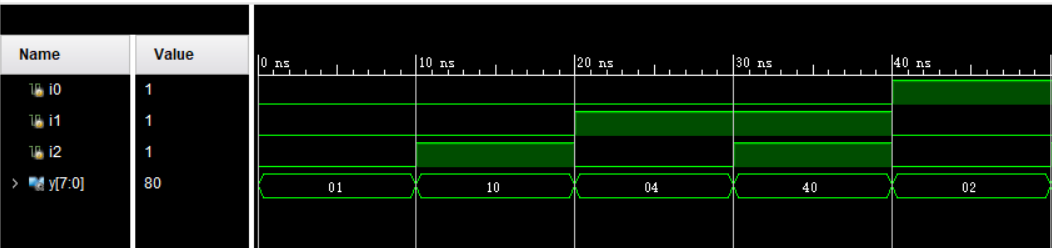
***3-8decoder***

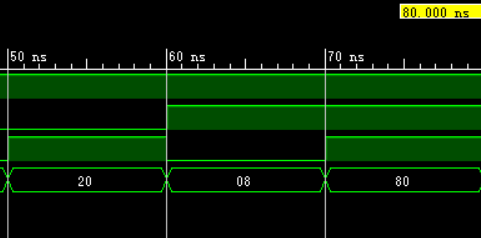


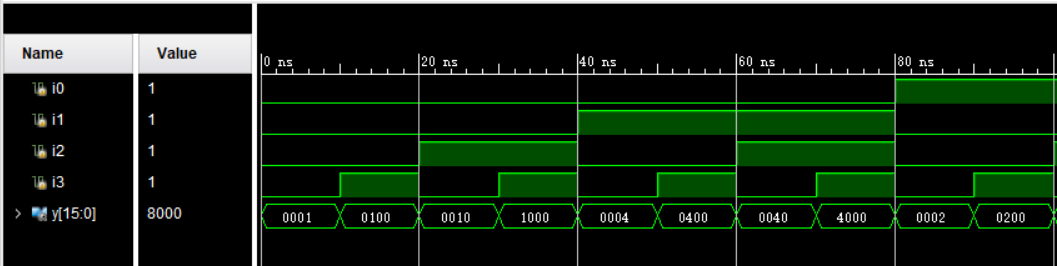
***4-16decoder***

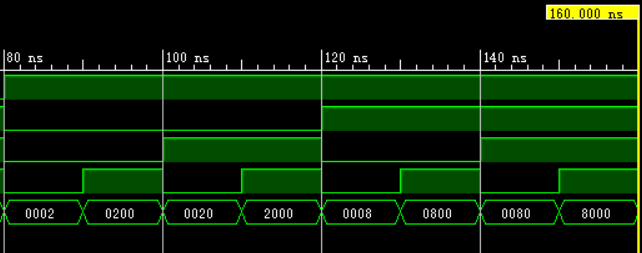


* *Wave form of simulation result (provide screen shots)*
* *3-8decoder*





* *4-16decoder*



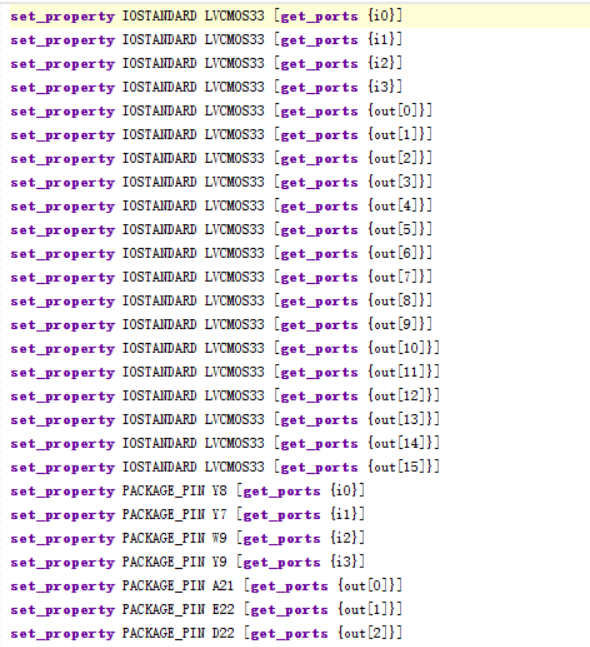
* *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation.*

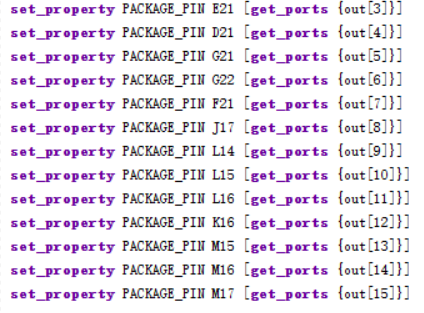
**the simulation result is same as the truth-table and meet the expectation**

##### Constraint file and the testing

*Describe how you test your design on the Minisys Practice platform.*

* *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*





* *The testing result (provide the screen shots (at least 3 testing scene) to show state of inputs and outputs along with the related descriptions.*

*15 0*

* *

*3 7*

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##### the description of operation

*Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.*

* *Problems and solutions*

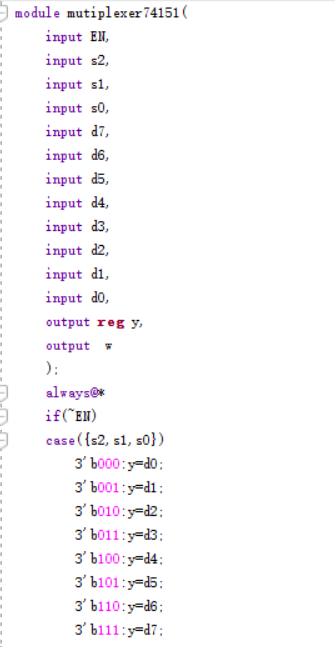
PART 2: DIGITAL design LAB (Task2)

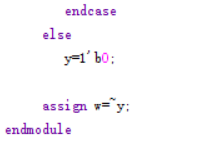
##### Design

*Describe the design of your system by providing the following information:*

* *Verilog design while using data flow (provide the Verilog code)*

***Design of 74151***





**Truth table**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **EN** | **S2** | **S1** | **S0** | **y** |
| **0** | **0** | **0** | **0** | **d0** |
| **0** | **0** | **0** | **1** | **d1** |
| **0** | **0** | **1** | **0** | **d2** |
| **0** | **0** | **1** | **1** | **d3** |
| **0** | **1** | **0** | **0** | **d4** |
| **0** | **1** | **0** | **1** | **d5** |
| **0** | **1** | **1** | **0** | **d6** |
| **0** | **1** | **1** | **1** | **d7** |
| **1** | **0** | **0** | **0** | **0** |
| **1** | **0** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **0** |
| **1** | **0** | **1** | **1** | **0** |
| **1** | **1** | **0** | **0** | **0** |
| **1** | **1** | **0** | **1** | **0** |
| **1** | **1** | **1** | **0** | **0** |
| **1** | **1** | **1** | **1** | **0** |

**Function design**

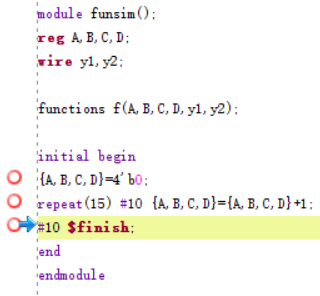
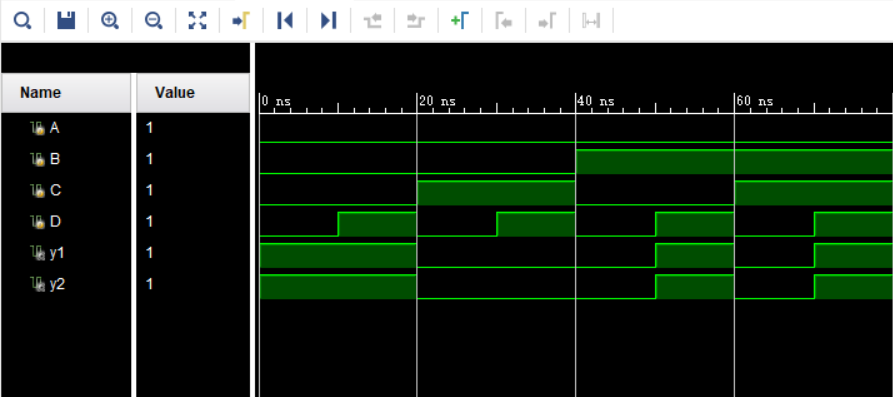
##### 

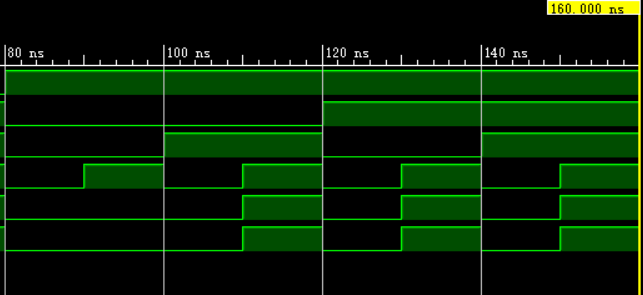
**Truth-table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **Y1** | **Y2** |
| **0** | **0** | **0** | **0** | **1** | **1** |
| **0** | **0** | **0** | **1** | **1** | **1** |
| **0** | **0** | **1** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** | **0** | **0** |
| **0** | **1** | **0** | **0** | **0** | **0** |
| **0** | **1** | **0** | **1** | **1** | **1** |
| **0** | **1** | **1** | **0** | **0** | **0** |
| **0** | **1** | **1** | **1** | **1** | **1** |
| **1** | **0** | **0** | **0** | **0** | **0** |
| **1** | **0** | **0** | **1** | **0** | **0** |
| **1** | **0** | **1** | **0** | **0** | **0** |
| **1** | **0** | **1** | **1** | **1** | **1** |
| **1** | **1** | **0** | **0** | **0** | **0** |
| **1** | **1** | **0** | **1** | **1** | **1** |
| **1** | **1** | **1** | **0** | **0** | **0** |
| **1** | **1** | **1** | **1** | **1** | **1** |

##### simulation

*Describe how you build the test bench and do the simulation.*

* *Using Verilog (provide the Verilog code)*
* 
* *Wave form of simulation result (provide screen shots)*
* 



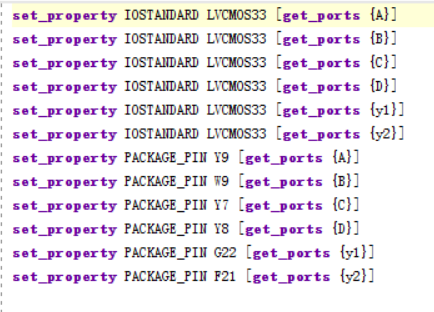
* *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation*

**the simulation result is same as the truth-table, the function of the design meet the expectation.**

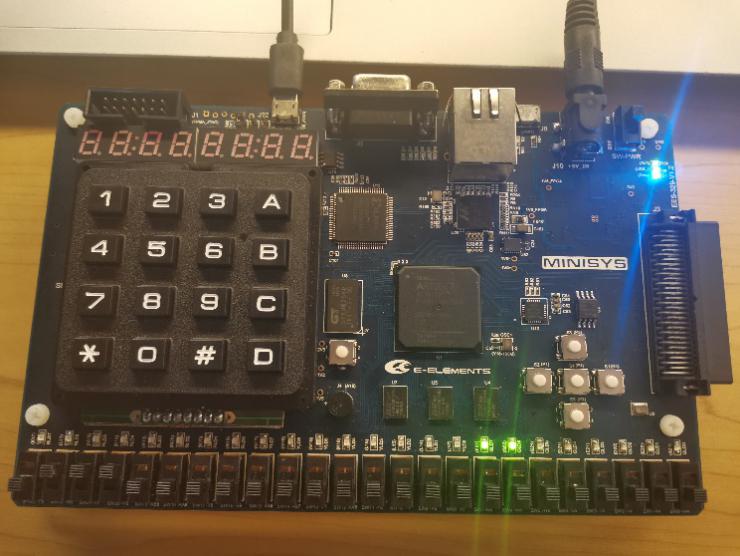
##### Constraint file and the testing

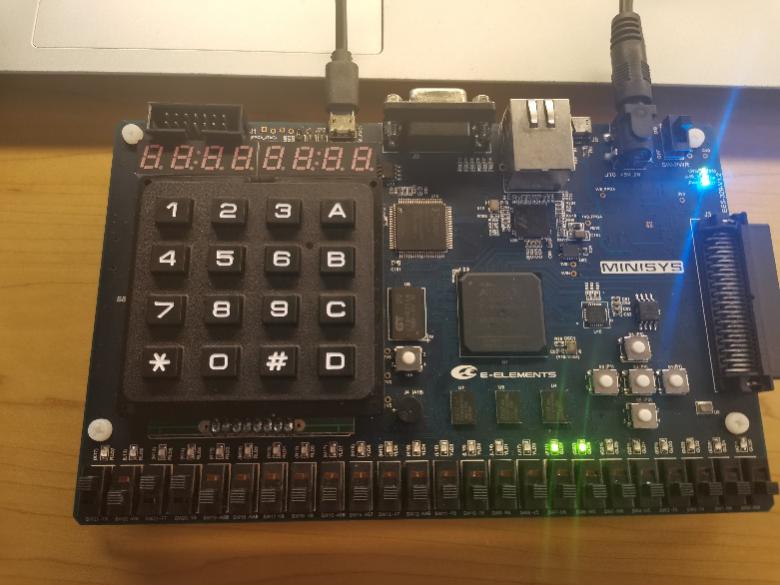
*Describe how you test your design on the Minisys Practice platform.*

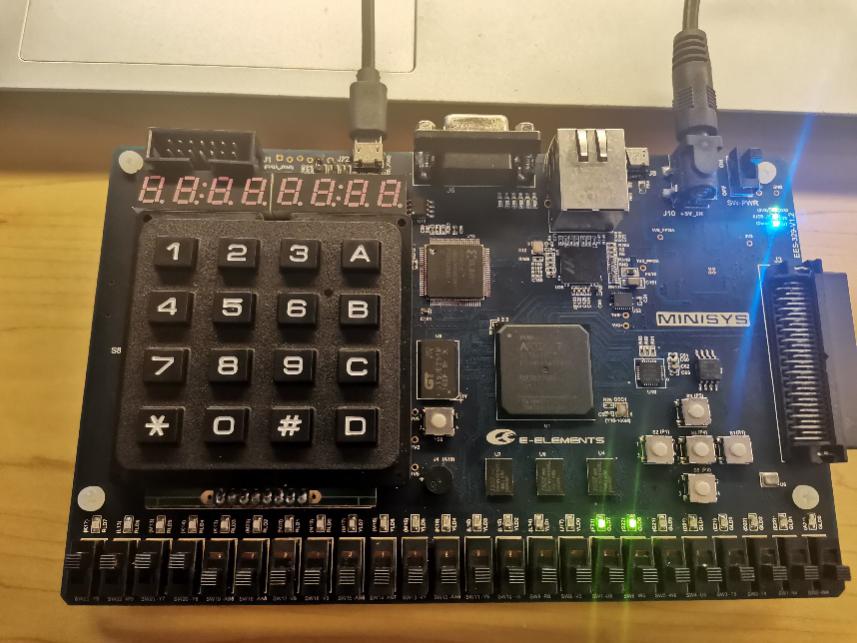
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* *

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