

**DIGITAL DESIGN**

**ASSIGNMENT REPORT**

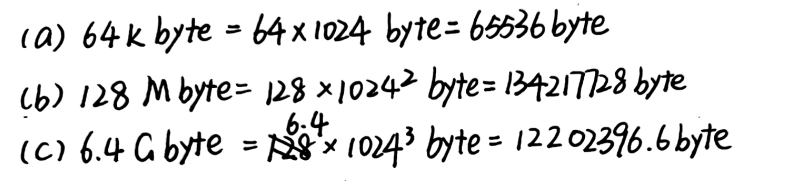
**ASSIGNMENT ID : I**

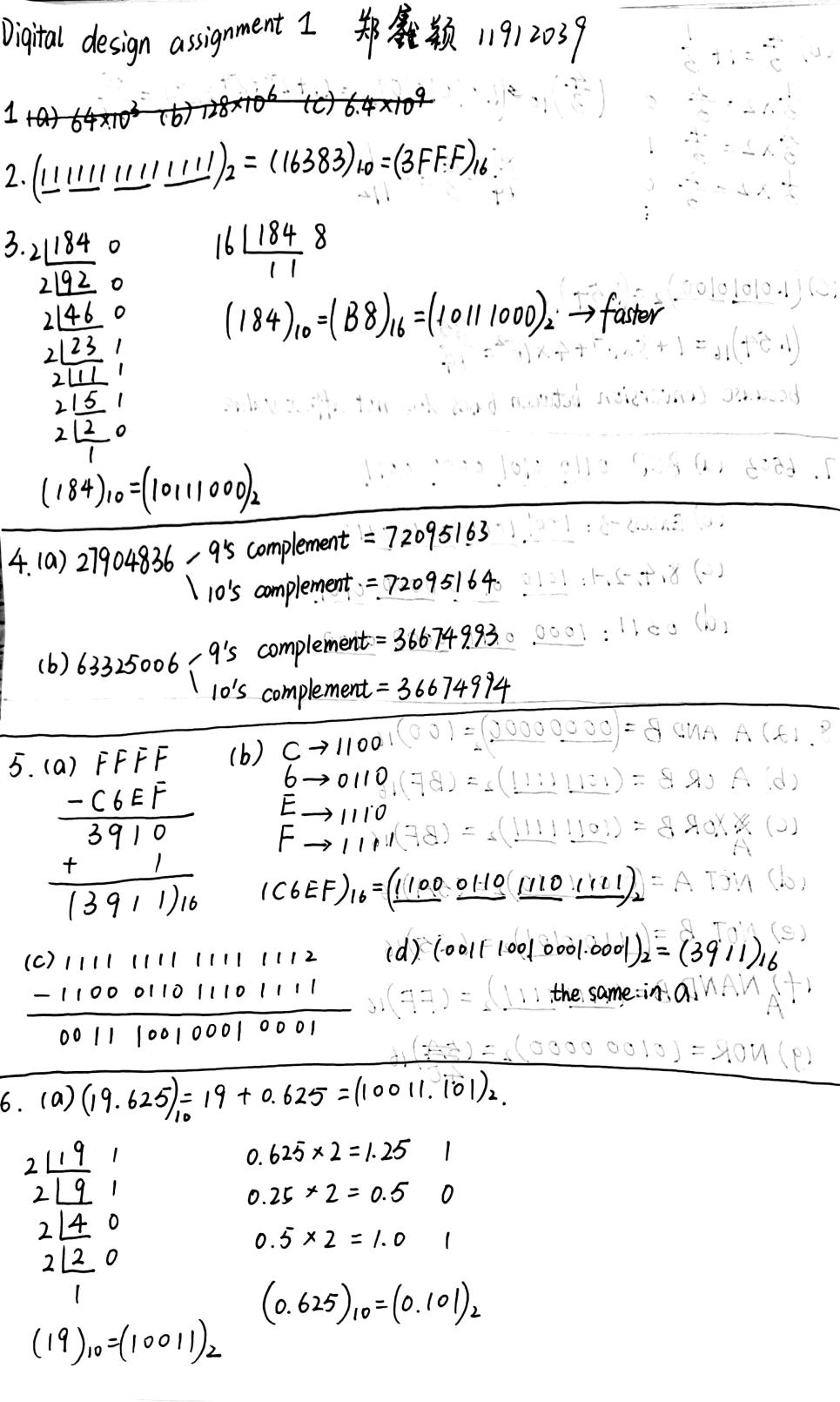
**Student Name: 郑鑫颖**

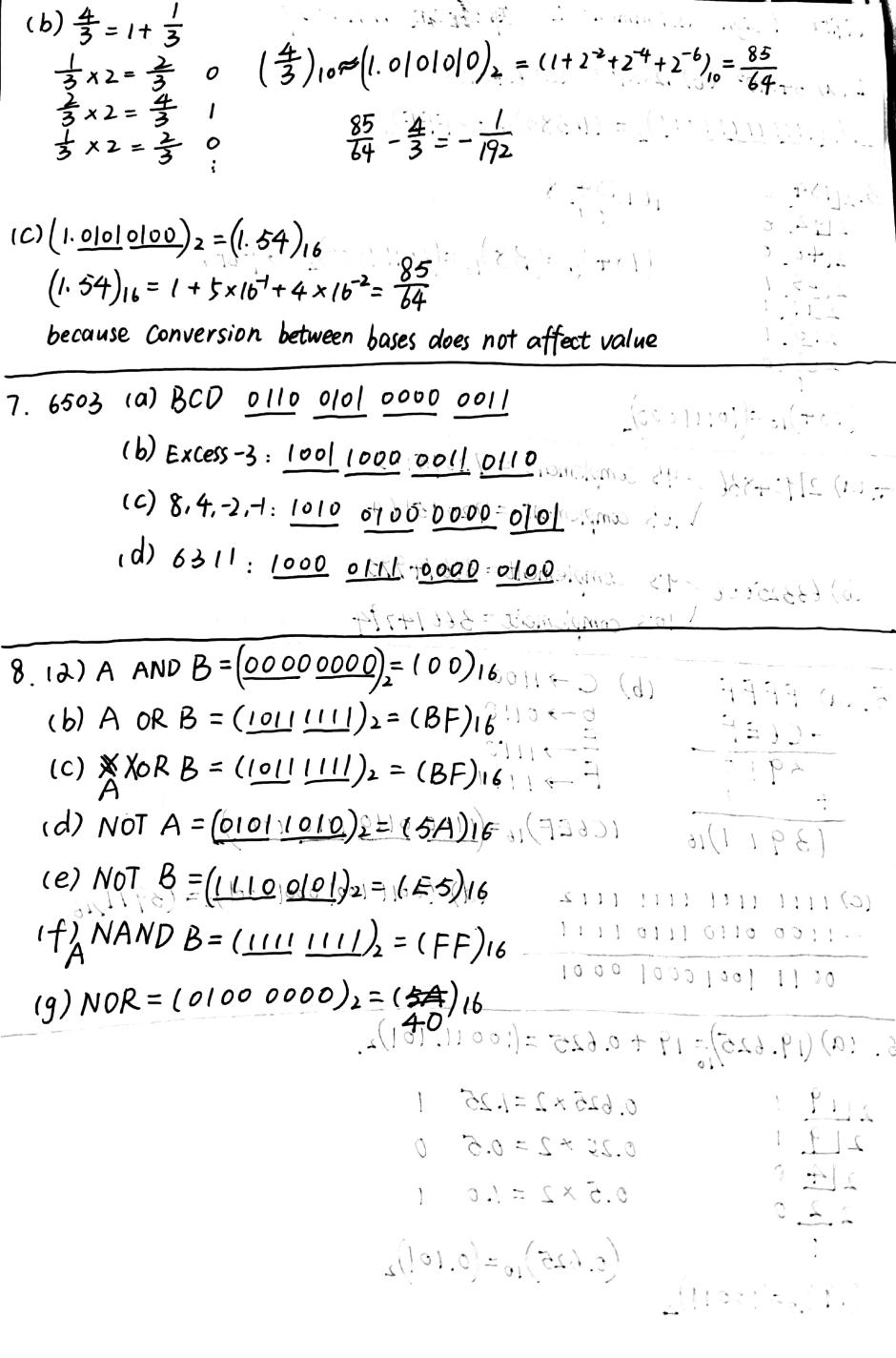
**Student ID: 11912039**

PART 1: DIGITAL design THEORY

Provide your answers here:





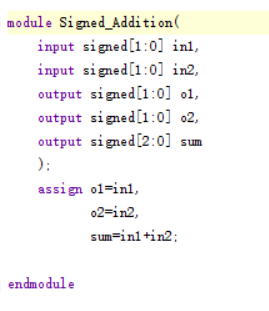


PART 2: DIGITAL design LAB (Task1)

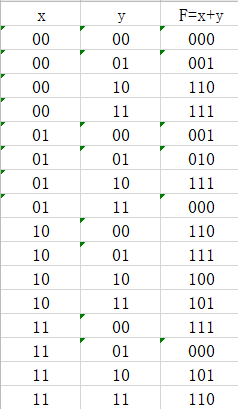
##### Design

*Describe the design of your system by providing the following information:*

* *Verilog design (provide the Verilog code)*



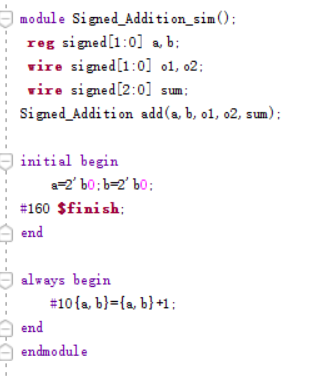
* *Truth-table*



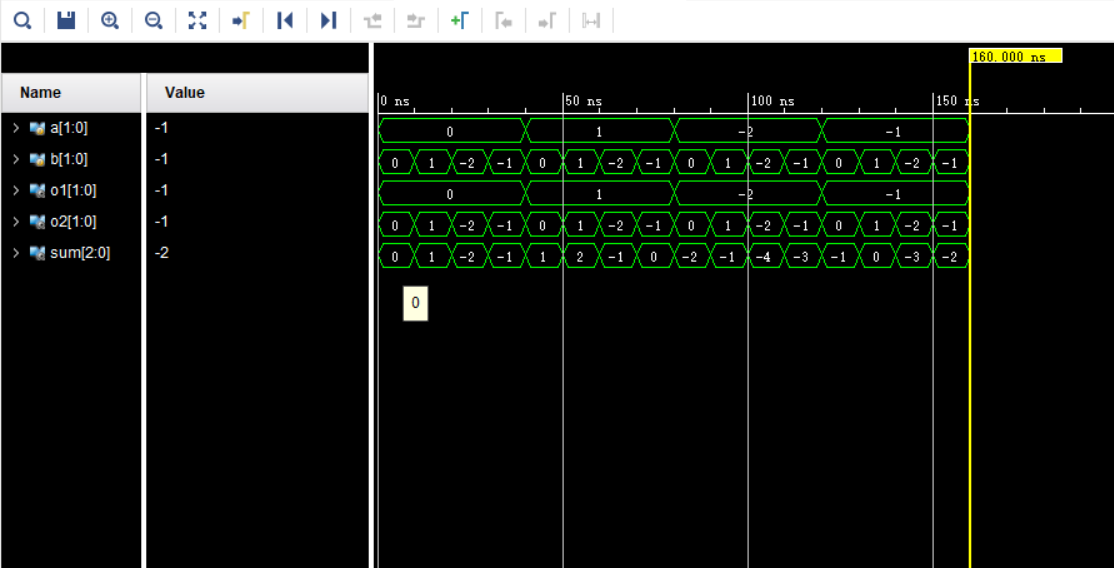
##### simulation

*Describe how you build the test bench and do the simulation.*

* *Using Verilog(provide the Verilog code)*



* *Wave form of simulation result (provide screen shots)*

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* *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation.*

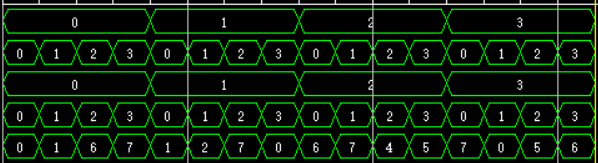
*By check the truth table and the result of the simulation result, I can fine that they are the same.*

##### the description of operation

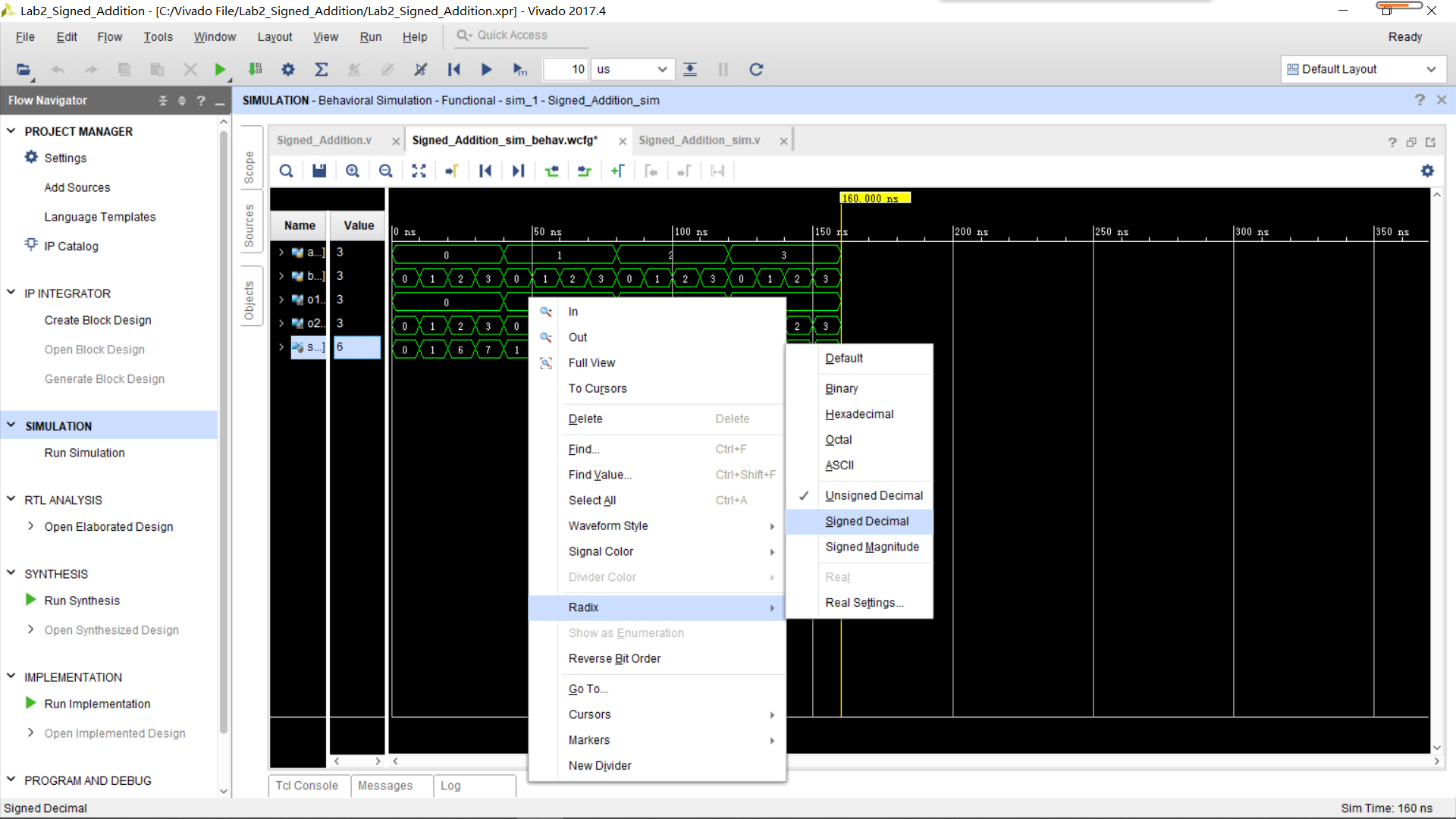
*Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.*

* *Problems and solutions*

*Problem1:while doing the simulation, I find that although I have made my input and output “signed”, it still displays unsigned data. Like the picture shows below.*

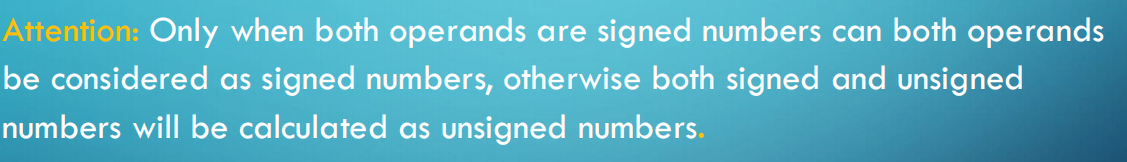


*Solution:*



*Problem2：I was wondering whether I can omit the “signed” before the output “sum”, since it is made by adding two signed numbers. it's a signed number by default*

*Solution:TA told me it’s better to add that “signed” to avoid mistakes, and I also find in the PPT that :*

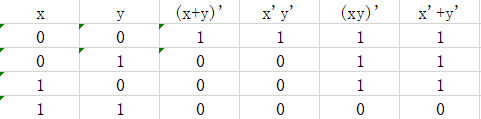


PART 2: DIGITAL design LAB (Task2)

##### Design

*Describe the design of your system by providing the following information:*

* *Verilog design while using data flow (provide the Verilog code)*
* *Verilog design while using structured design (provide the Verilog code.*
* *Truth-table*



##### simulation

*Describe how you build the test bench and do the simulation.*

* *Using Verilog (provide the Verilog code)*
* *Wave form of simulation result (provide screen shots)*
* *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation*

##### Constraint file and the testing

*Describe how you test your design on the Minisys Practice platform.*

* *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
* *The testing result (provide the screen shots (at least 3 testing scene)) to show state of inputs and outputs along with the related descriptions.*

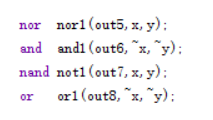
##### the description of operation

*Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.*

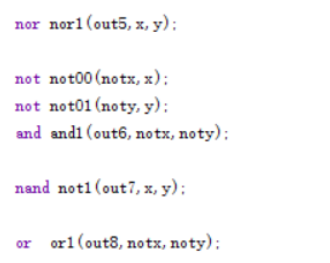
* *Problems and solutions*

*Problem1:Firstly, I did the structure design in the way as the following picture shows,*

*To use ~x and~y rather the not gate. And teacher told me the result is right but somehow don’t satisfy the requirement.*

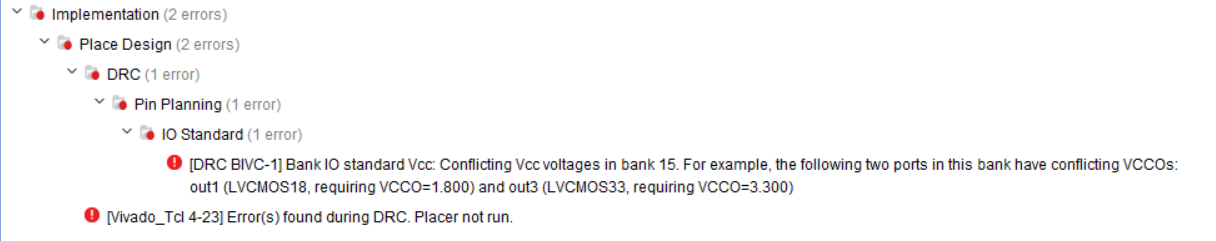


*Solution: Then I modified my design.*



*Problem2: while* editing a constraints file, I using out1[0] to represent the first bit of out1(out1 and out2 are both 1 bit long), as the following picture shows Then my implementation failed.

IMG_256

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*Solution: Then I ask teacher, she told me that if the port is one bit long , there’s no need to add that[0].*

