



## **PES University, Bangalore**

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**August 2022: Edmodo Assignment**

**UE21CS251A**

**DDCO Lab**

**Week 2 Assignment**

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**Branch : CSE**

**Semester & Section : Third Semester(Section B).**

## Half Adder:

### Code for Source file halfadd.v:

```
module halfadder(input wire a, b, output wire sum, carry);
xor1 a1(a,b,sum);
and1 a2(a,b,carry);
endmodule
```

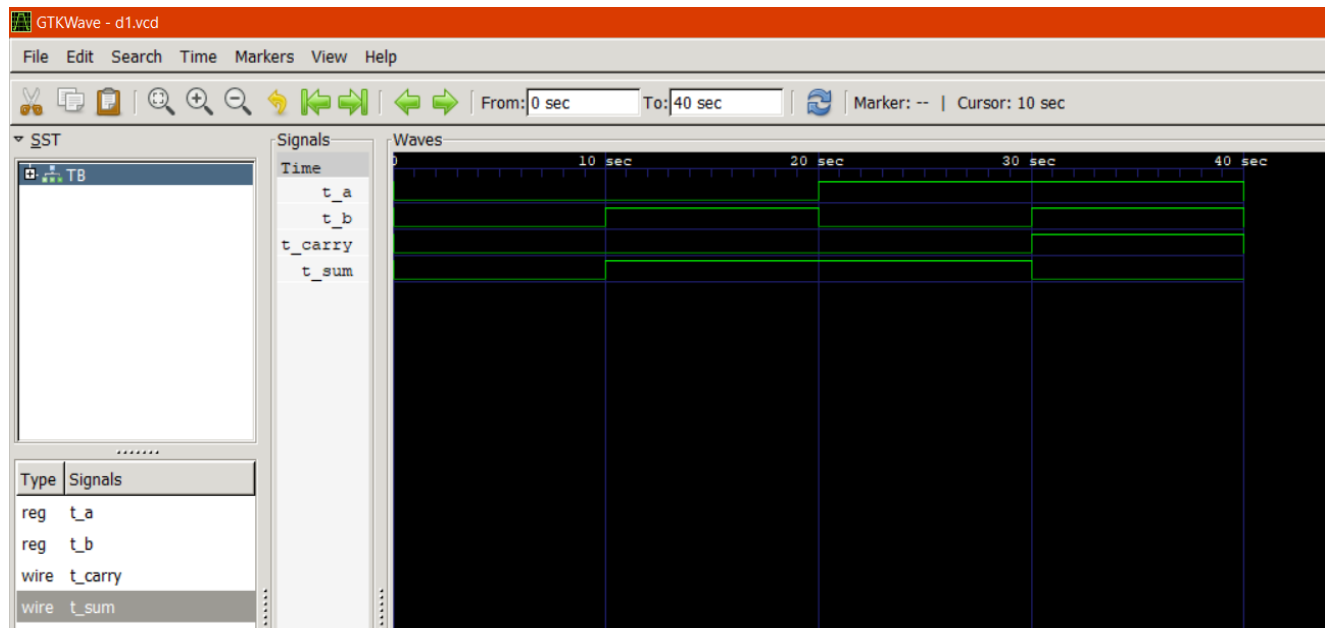
### Code for Testbench file halfadd\_tb.v:

```
module TB;
reg t_a;
reg t_b;
wire t_sum,t_carry;
halfadder a3(.a(t_a),.b(t_b),.sum(t_sum),.carry(t_carry));
initial
begin
    $dumpfile("d1.vcd"); //value change dump
    $dumpvars(0,TB);
end
initial
begin
    $monitor(t_a,t_b,t_sum,t_carry);
    t_a=1'b0;
    t_b=1'b0;
    #10
    t_a=1'b0;
    t_b=1'b1;
    #10
    t_a=1'b1;
    t_b=1'b0;
    #10
    t_a=1'b1;
    t_b=1'b1;
    #10
    t_a=1'b0;
    t_b=1'b0;
end
endmodule
```

## Snapshot output for half adder:

```
PS C:\iverilog\bin\week2> iverilog -o halfadder test.v halfadd.v halfadd_tb.v
PS C:\iverilog\bin\week2> vvp halfadder
VCD info: dumpfile d1.vcd opened for output.
0000
0110
1010
1101
0000
PS C:\iverilog\bin\week2> |
```

## Snapshot for GTK Waveform for half adder:



## Full Adder:

### Code for Source file fulladd.v:

```
module fulladd(input wire a,b,c, output wire sum, carry);
    wire [4:0] t;
    xor1 a1(a,b,t[0]);
    xor1 a2(t[0],c,sum);
    and1 a3(a,c,t[1]);
    and1 a4(b,c,t[2]);
    and1 a5(a,b,t[3]);
    or1 a6(t[1],t[2],t[4]);
    or1 a7(t[3],t[4],carry);
endmodule
```

### Code for Testbench file fulladd\_tb.v:

```
module TB;
reg t_a;
reg t_b;
reg t_c;
wire t_sum,t_carry;
fulladd a8(.a(t_a),.b(t_b),.c(t_c),.sum(t_sum),.carry(t_carry));
initial
begin
    $dumpfile("d1.vcd"); //value change dump
    $dumpvars(0,TB);
end
initial
begin
    $monitor(t_a,t_b,t_c,t_sum,t_carry);
    t_a=1'b0;
    t_b=1'b0;
    t_c=1'b0;
    #10
    t_a=1'b0;
    t_b=1'b0;
    t_c=1'b1;
    #10
    t_a=1'b0;
    t_b=1'b1;
    t_c=1'b0;
    #10
    t_a=1'b0;
    t_b=1'b1;
    t_c=1'b1;
    #10
end
```

```

t_a=1'b1;
t_b=1'b0;
t_c=1'b0;
#10
t_a=1'b1;
t_b=1'b0;
t_c=1'b1;
#10
t_a=1'b1;
t_b=1'b1;
t_c=1'b0;
#10
t_a=1'b1;
t_b=1'b1;
t_c=1'b1;
end
endmodule

```

## Snapshots of code output and GTK waveform for full adder:

```

PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL JUPYTER
PS C:\iverilog\bin\week2> iverilog -o fulladder test.v fulladd.v fulladd_tb.v
PS C:\iverilog\bin\week2> vvp fulladder
VCD info: dumpfile d1.vcd opened for output.
00000
00110
01010
01101
10010
10101
11001
11111
PS C:\iverilog\bin\week2>

```

