Digital Design and Computer Organization Laboratory

UE21CS251A

3rd Semester, Academic Year 2021-22

ASSIGNMENT 1

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4:1 MUX AND DEMUX

Code:

2:1 MUX

Testbench :

```
module tb;
reg t_d0,t_d1,t_s;
wire t_sum;
twomux t1(.d0(t_d0),.d1(t_d1),.s(t_s),.Y(t_sum));
initial begin $dumpfile("dump.vcd");
$dumpvars(0,tb);
end
initial begin $monitor(t_d0,t_d1,t_s,t_sum);
t_d0 = 1'b0;
t_d1 = 1'b0;
t_s = 1'b0;
```

```
#10
t_d0 = 1'b0;
t_d1 = 1'b1;
t_s = 1'b0;
#10
t_d0 = 1'b1;
t_d1 = 1'b0;
t_s = 1'b0;
#10
t_d0 = 1'b1;
t_d1 = 1'b1;
t_s = 1'b0;
#10
t_d0 = 1'b0;
t_d1 = 1'b0;
t_s = 1'b1;
#10
t_d0 = 1'b0;
t_d1 = 1'b1;
t_s = 1'b1;
#10
t_d0 = 1'b1;
t_d1 = 1'b0;
t_s = 1'b1;
#20
t_d0 = 1'b1;
t_d1 = 1'b1;
```

```
t_s = 1'b1;
end
endmodule
```

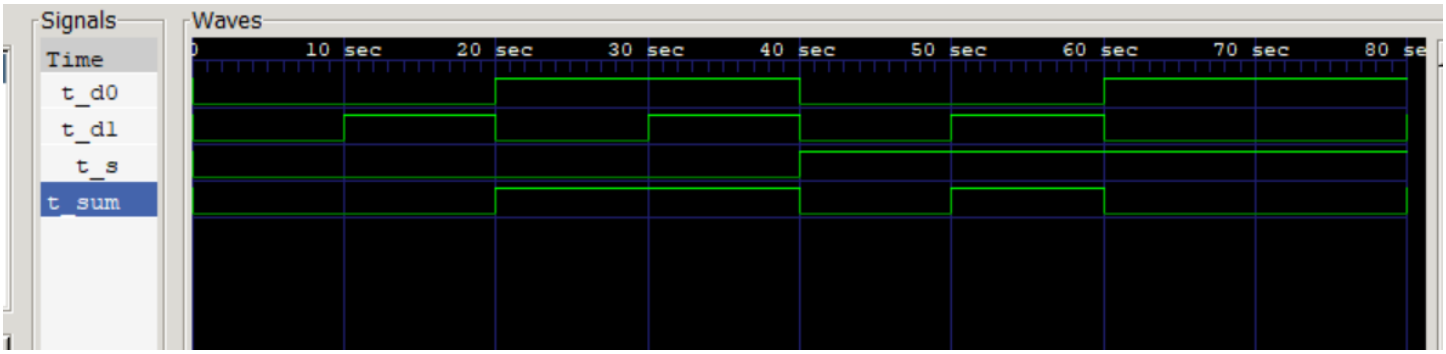
module file :

```
module twomux(input wire d0,d1,s,output wire Y);
wire sum1,sum2,sbar;
invert n1(s,sbar);
and2 a1(sbar,d0,sum1);
and2 a2(s,d1,sum2);
or2 o1(sum1,sum2,Y);
endmodule
```

compiling files :

```
C:\Users\suraj>cd C:\iverilog\bin

C:\iverilog\bin>iverilog -o xyz lib.v mux2.v mux2tb.v

C:\iverilog\bin>vvp xyz
VCD info: dumpfile dump.vcd opened for output.
0000
0100
1001
1101
0010
0111
1010
1111

C:\iverilog\bin>gtkwave dump.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[80] end time.
```

OUTPUT WAVEFORM :



4:1 MUX USING 2:1 MUX :

Code:

Module file :

```
module fourmux(input wire d0,d1,d2,d3,s0,s1,output wire Y);
wire w1,w2;
twomux t1(d0,d1,s0,w1);
twomux t2(d2,d3,s0,w2);
twomux t3(w1,w2,s1,Y);
endmodule
```

Testbench :

```
module tb;
reg t_d0,t_d1,t_d2,t_d3,t_s0,t_s1;
wire t_sum;
fourmux f1(.d0(t_d0),.d1(t_d1),.d2(t_d2),.d3(t_d3),.s0(t_s0),.s1(t_s1),.Y(t_sum));
initial begin $dumpfile("dump.vcd");
$dumpvars(0,tb);
end
initial begin $monitor(t_d0,t_d1,t_d2,t_d3,t_s1,t_s0,t_sum);
t_d0 = 1'b0;
t_d1 = 1'b0;
t_d2 = 1'b0;
t_d3 = 1'b0;
t_s0 = 1'b0;
t_s1 = 1'b0;
#10
t_d0 = 1'b0;
```

```
t_d1 = 1'b0;
t_d2 = 1'b0;
t_d3 = 1'b1;
t_s0 = 1'b0;
t_s1 = 1'b0;
#10
t_d0 = 1'b0;
t_d1 = 1'b0;
t_d2 = 1'b1;
t_d3 = 1'b0;
t_s0 = 1'b0;
t_s1 = 1'b0;
#10
t_d0 = 1'b0;
t_d1 = 1'b0;
t_d2 = 1'b1;
t_d3 = 1'b1;
t_s0 = 1'b0;
t_s1 = 1'b0;
#10
t_d0 = 1'b0;
t_d1 = 1'b1;
t_d2 = 1'b0;
t_d3 = 1'b0;
t_s0 = 1'b1;
t_s1 = 1'b0;
#10
```

```
t_d0 = 1'b0;
t_d1 = 1'b1;
t_d2 = 1'b0;
t_d3 = 1'b1;
t_s0 = 1'b1;
t_s1 = 1'b0;
#10
t_d0 = 1'b0;
t_d1 = 1'b1;
t_d2 = 1'b1;
t_d3 = 1'b0;
t_s0 = 1'b1;
t_s1 = 1'b0;
#10
t_d0 = 1'b0;
t_d1 = 1'b1;
t_d2 = 1'b1;
t_d3 = 1'b1;
t_s0 = 1'b1;
t_s1 = 1'b0;
#10
t_d0 = 1'b1;
t_d1 = 1'b0;
t_d2 = 1'b0;
t_d3 = 1'b0;
t_s0 = 1'b0;
t_s1 = 1'b1;
```

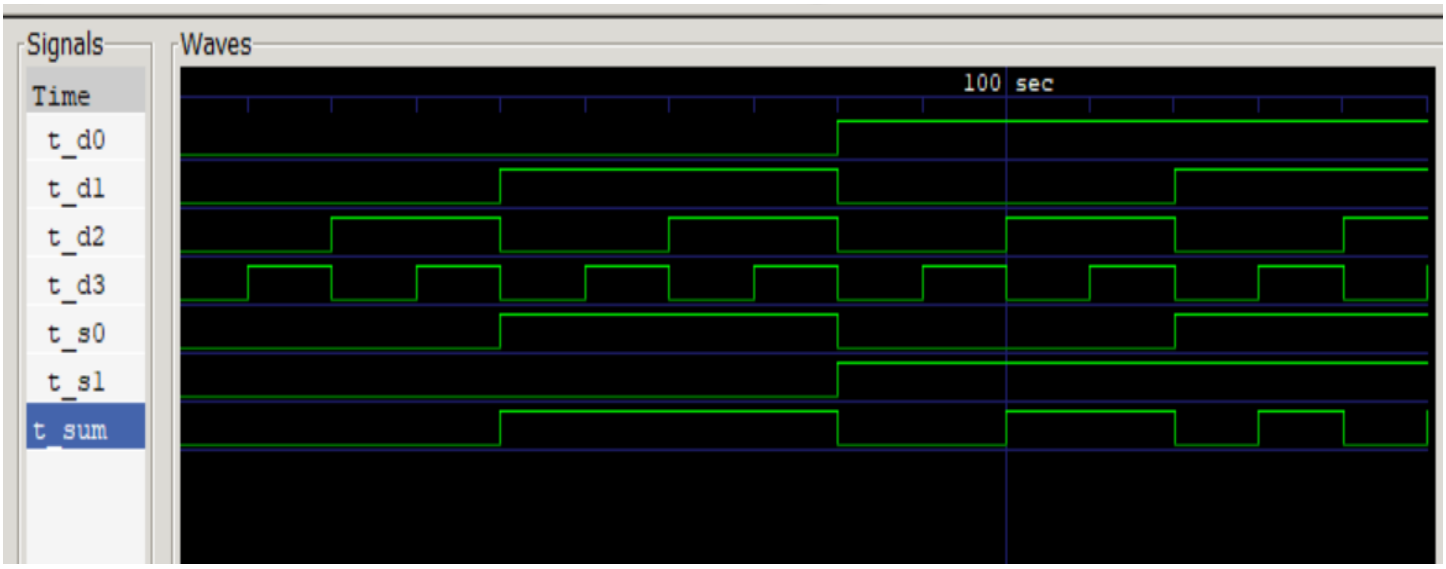
```
#10
t_d0 = 1'b1;
t_d1 = 1'b0;
t_d2 = 1'b0;
t_d3 = 1'b1;
t_s0 = 1'b0;
t_s1 = 1'b1;
#10
t_d0 = 1'b1;
t_d1 = 1'b0;
t_d2 = 1'b1;
t_d3 = 1'b0;
t_s0 = 1'b0;
t_s1 = 1'b1;
#10
t_d0 = 1'b1;
t_d1 = 1'b0;
t_d2 = 1'b1;
t_d3 = 1'b1;
t_s0 = 1'b0;
t_s1 = 1'b1;
#10
t_d0 = 1'b1;
t_d1 = 1'b1;
t_d2 = 1'b0;
t_d3 = 1'b0;
t_s0 = 1'b1;
```

```
t_s1 = 1'b1;
#10
t_d0 = 1'b1;
t_d1 = 1'b1;
t_d2 = 1'b0;
t_d3 = 1'b1;
t_s0 = 1'b1;
t_s1 = 1'b1;
#10
t_d0 = 1'b1;
t_d1 = 1'b1;
t_d2 = 1'b1;
t_d3 = 1'b0;
t_s0 = 1'b1;
t_s1 = 1'b1;
#10
t_d0 = 1'b1;
t_d1 = 1'b1;
t_d2 = 1'b1;
t_d3 = 1'b1;
t_s0 = 1'b1;
t_s1 = 1'b1;
end
endmodule
```

compiling files :

```
C:\iverilog\bin>iverilog -o xyz lib.v mux2.v mux4.v mux4tb.v

C:\iverilog\bin>vvp xyz
VCD info: dumpfile dump.vcd opened for output.
0000000
0001000
0010000
0011000
0100011
0101011
0110011
0111011
1000100
1001100
1010101
1011101
1100110
1101111
1110110
1111111

C:\iverilog\bin>gtkwave dump.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[150] end time.
WM Destroy
```

OUTPUT WAVEFORM :



4:1 DEMUX

Code :

Testbench :

```
module Demux;
wire [3:0] Y;
reg [1:0] A;
reg din;
Demux I0 (Y, A, din);
initial begin
din = 1;
A[1] = 0; A[0] = 0;
 #1 A[1] = 0; A[0] = 1;
 #1 A[1] = 1; A[0] = 0;
 #1 A[1] = 1; A[0] = 1;
end
initial begin
 $monitor("%t| Din = %d| A[1] = %d| A[0] = %d| Y[0] = %d| Y[1] = %d| Y[2] = %d| Y[3] = %d",
 $time, din, A[1], A[0], Y[0], Y[1], Y[2], Y[3]);
end
endmodule
```

Module file :

```
module Demux(output [3:0] Y, input [1:0] A, input din);
assign Y[0] = din & (~A[0]) & (~A[1]);
assign Y[1] = din & (~A[1]) & A[0];
assign Y[2] = din & A[1] & (~A[0]);
assign Y[3] = din & A[1] & A[0];
```

endmodule

compiling files :

```
C:\iverilog\bin>iverilog -o xyz lib.v demux.v demuxtb.v

C:\iverilog\bin>vvp xyz
                  0| Din = 1| A[1] = 0| A[0] = 0| Y[0] = 1| Y[1] = 0| Y[2] = 0| Y[3] = 0
                  1| Din = 1| A[1] = 0| A[0] = 1| Y[0] = 0| Y[1] = 1| Y[2] = 0| Y[3] = 0
                  2| Din = 1| A[1] = 1| A[0] = 0| Y[0] = 0| Y[1] = 0| Y[2] = 1| Y[3] = 0
                  3| Din = 1| A[1] = 1| A[0] = 1| Y[0] = 0| Y[1] = 0| Y[2] = 0| Y[3] = 1

C:\iverilog\bin>gtkwave xyz

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI
```

OUTPUT WAVEFORM :