DDCO LAB 9 : PROGRAM COUNTER(PC)

SRN : PES1UG21CS355

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IVERILOG CODE :

```
module fa(input wire i0, i1, cin, output wire sum, cout);
wire t0, t1, t2;
   xor3 _i0 (i0, i1, cin, sum);
   and2 _i1 (i0, i1, t0);
   and2 _i2 (i1, cin, t1);
   and2 _i3 (cin, i0, t2);
   or3 _i4 (t0, t1, t2, cout);
endmodule

module addsub(input wire addsub, i0, i1, cin, output wire sumdiff, cout);
wire t;
fa _i0 (i0, t, cin, sumdiff, cout);
  xor2 _i1 (i1, addsub, t);
endmodule

module pc_slice0(input wire clk,reset,cin,load,inc,sub,offset,output wire cout,pc);
    wire t;
    wire in;
    or2 o1(offset,inc,t);
    addsub a1(sub,pc,t,cin,in,cout);
    dfrl d1(clk,reset,load,in,pc);
endmodule

module pc_slice1(input wire clk,reset,cin,load,inc,sub,offset,output wire cout,pc);
    wire t,in,inc_;
    invert i0(inc,inc_);
    and2 a2(offset,inc_,t);
    addsub a1(sub,pc,t,cin,in,cout);
    dfrl d1(clk,reset,load,in,pc);
endmodule

module pc(input wire clk, reset, inc, add, sub, input wire [15:0] offset, output wire [15:0] pc);
    wire load;
    wire [15:0] c;
    or3 o1(inc,add,sub,load);
    pc_slice0 i0_(clk,reset,sub,load,inc,sub,offset[0],c[0],pc[0]);
    pc_slice1 i1_(clk,reset,c[0],load,inc,sub,offset[1],c[1],pc[1]);
    pc_slice1 i2_(clk,reset,c[1],load,inc,sub,offset[2],c[2],pc[2]);
    pc_slice1 i3_(clk,reset,c[2],load,inc,sub,offset[3],c[3],pc[3]);
    pc_slice1 i4_(clk,reset,c[3],load,inc,sub,offset[4],c[4],pc[4]);
    pc_slice1 i5_(clk,reset,c[4],load,inc,sub,offset[5],c[5],pc[5]);
    pc_slice1 i6_(clk,reset,c[5],load,inc,sub,offset[6],c[6],pc[6]);
    pc_slice1 i7_(clk,reset,c[6],load,inc,sub,offset[7],c[7],pc[7]);
    pc_slice1 i8_(clk,reset,c[7],load,inc,sub,offset[8],c[8],pc[8]);
    pc_slice1 i9_(clk,reset,c[8],load,inc,sub,offset[9],c[9],pc[9]);
    pc_slice1 i10_(clk,reset,c[9],load,inc,sub,offset[10],c[10],pc[10]);
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```
    pc_slice1 i11_(clk,reset,c[10],load,inc,sub,offset[11],c[11],pc[11]);
    pc_slice1 i12_(clk,reset,c[11],load,inc,sub,offset[12],c[12],pc[12]);
    pc_slice1 i13_(clk,reset,c[12],load,inc,sub,offset[13],c[13],pc[13]);
    pc_slice1 i14_(clk,reset,c[13],load,inc,sub,offset[14],c[14],pc[14]);
    pc_slice1 i15_(clk,reset,c[14],load,inc,sub,offset[15],c[15],pc[15]);
endmodule
```

OUTPUT :

```
C:\Windows\System32\cmd.e
Microsoft Windows [Version 10.0.22621.819]
(c) Microsoft Corporation. All rights reserved.

C:\iverilog\bin>iverilog pc.v tb_pc.v lib_pc.v

C:\iverilog\bin>vvp a.out
VCD info: dumpfile tb_pc.vcd opened for output.

C:\iverilog\bin>gtkwave tb_pc.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[156000] end time.
```