Digital Design and Computer Organization

UE21CS251A

3rd Semester, Academic Year 2021-22

Assignment 3

Name : R NAVEEN KUMAR	SRN : PES1UG21CS367	Section : F

Title of the Program:

Code:

Module file :

```
module updowncounter(clk,cntrl,rst,count);
 input clk,cntrl,rst; // if cntrl = 1 , counts UP else DOWN
 output reg [3:0] count;
 always @ (posedge clk, posedge rst)
 begin
 if(rst)
 count <= 0 ;
 else if (cntrl)
 count <= count + 1;
 else
 count <= count - 1;
```

```
 end
endmodule
```

Testbench file :

```
module updowncountertb();
 reg clk,rst,cntrl;
 wire [3:0] count;
 updowncounter c(clk,cntrl,rst,count);

 initial
 begin
 clk = 0;
 forever #5 clk = ~clk;
 end

 initial
 begin

 $monitor("%7d %1b %1b %1b %4b ",$time,cntrl,clk,rst,count);
 $display("time cntrl clk rst count");
 #10 rst=1; cntrl=1;
 #10 rst=0;
 #60 cntrl =0;
 #100 cntrl =1;
 #30 rst =1;
 #10 rst =0;
 end
```

```
initial
begin
$dumpfile("dump.vcd");
$dumpvars(0,updowncountertb);
#400 $finish;
end

endmodule
```

OUTPUT WAVEFORM :