Digital Design and Computer Organization Assignment 2

UE21CS251A

3rd Semester, Academic Year 2021-22

ASSIGNMENT 2

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FLIPFLOPS

1. SR FlipFlop

Code :

Module file :

```
module srf(input wire clk,s,r,output wire q,q_b);
reg s_o,r_o;
always @(posedge clk) begin
 s_o <= !(s & clk);
 r_o <= !(r & clk);
end
nand2 nand2_3(s_o,q_b,q);
nand2 nand2_4(r_o,q,q_b);
endmodule
```

Testbench :

```
`timescale 1 ns/100 ps
```

```
module tb;
 reg t_s,t_r,clk;
 wire t_q,t_q_b;
 reg [1:0] i_p [0:4];
 integer i;
 initial begin
 $dumpfile("dumpSR.vcd");
 $dumpvars(0,tb);
 end
 initial clk=1'b0; always #5 clk =~clk;
 initial begin
 i_p[0][1:0]=2'b01;
 i_p[1][1:0]=2'b00;
 i_p[2][1:0]=2'b01;
 i_p[3][1:0]=2'b10;
 i_p[4][1:0]=2'b11;
 end
 initial {t_s,t_r, i} =0;
 srf srf_1(clk,t_s,t_r,t_q,t_q_b);
 initial begin
 #5
for(i=0;i<5;i=i+1)
 begin
#10 {t_s,t_r}=i_p[i];
end
 #30
$finish;
```

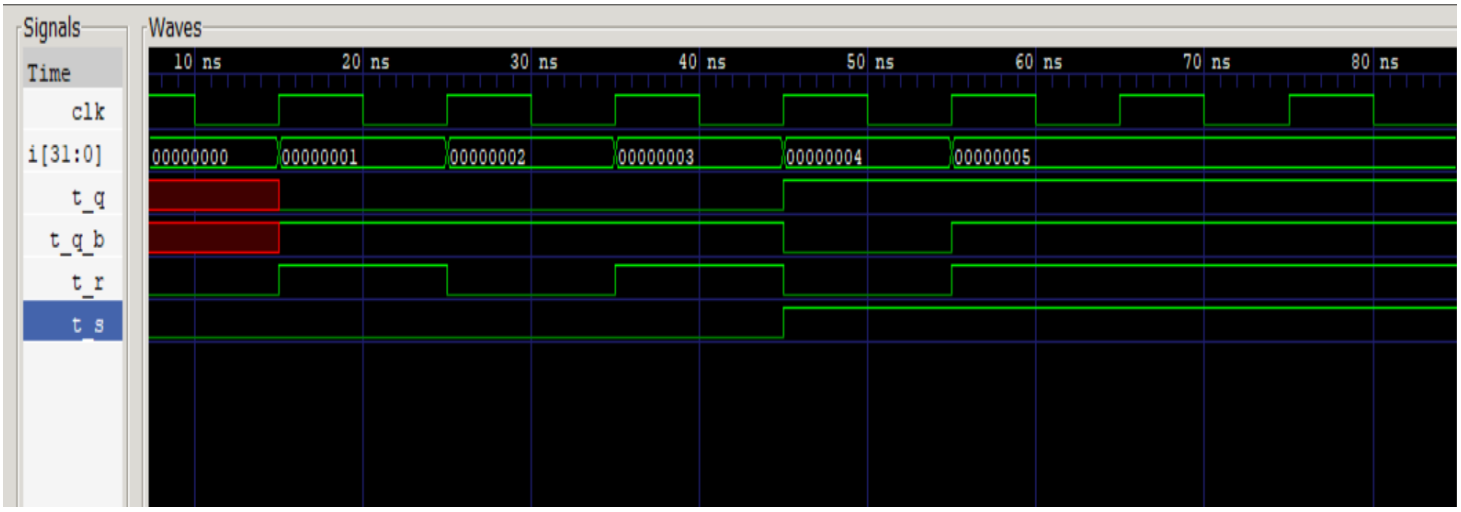
end

endmodule

Compiling files :

```
C:\iverilog\bin>iverilog -o xyz lib.v srtb.v sr.v

C:\iverilog\bin>vvp xyz
VCD info: dumpfile dumpSR.vcd opened for output.

C:\iverilog\bin>gtkwave dumpSR.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[85000] end time.
WM Destroy
```

OUTPUT WAVEFORM:



2. JK FlipFlop

Code :

Module file :

```
module jkf(input wire clk,reset,j,k,output wire q,q_b);
reg s_in,r_in,q_out,q_b_out;
wire s_in_w,r_in_w;
reg a_s_o,a_r_o;
always @(posedge clk,posedge reset) begin
 if(reset == 0) begin
 if(k == 0 & j == 0) begin
 q_out <= q_out;
 q_b_out <= q_b_out;
 end
 else if(k == 1 & j == 1) begin
 q_out <= ~q_out;
 q_b_out <= ~q_b_out;
 end
 else if(j == 1) begin
 q_out <= 1;
 q_b_out <= 0;
 end
 else if(k == 1) begin
 q_out <= 0;
 q_b_out <= 1;
 end
 end
```

```
 else begin
 q_out <= 0;
 q_b_out <= 1;
end
end
assign q = q_out;
assign q_b = q_b_out;
endmodule
```

Testbench :

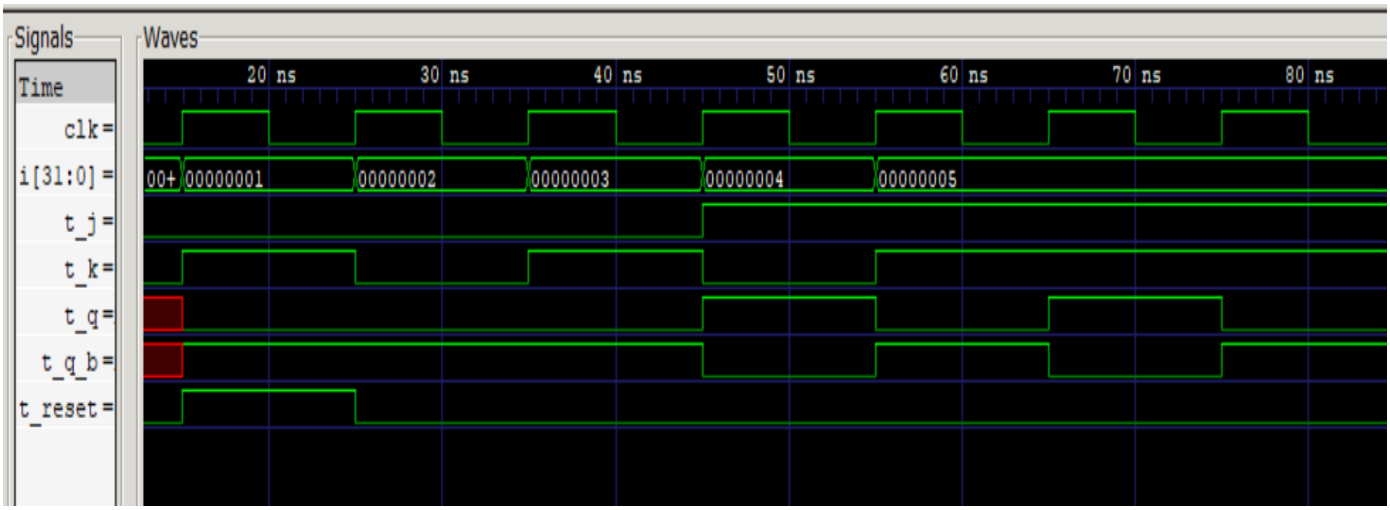
```
`timescale 1 ns/100 ps
module tb;
 reg t_j,t_k,t_reset,clk;
 wire t_q,t_q_b;
 reg [2:0] i_p [0:4];
 integer i;
 initial begin
 $dumpfile("dumpJK_FF.vcd");
 $dumpvars(0,tb);
 end
 initial clk=1'b0; always #5 clk =~clk;
 initial begin
 i_p[0][2:0]=3'b101;
 i_p[1][2:0]=3'b000;
 i_p[2][2:0]=3'b001;
 i_p[3][2:0]=3'b010;
 i_p[4][2:0]=3'b011;
 end
```

```
initial {t_reset,t_j,t_k,i} =0;
jkf jkf_1(clk,t_reset,t_j,t_k,t_q,t_q_b);
initial begin
#5 for(i=0;i<5;i=i+1)
begin #10 {t_reset,t_j,t_k}=i_p[i]; end
#40 $finish;
end
endmodule
```

Compiling files :

```
C:\iverilog\bin>iverilog -o xyz lib.v jktb.v jk.v

C:\iverilog\bin>vvp xyz
VCD info: dumpfile dumpJK_FF.vcd opened for output.

C:\iverilog\bin>gtkwave dumpJK_FF.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[95000] end time.
WM Destroy
```

OUTPUT WAVEFORM:



3.T FlipFlop

Code :

Module file :

```
module tf(input wire clk,reset,t,output wire q,q_b);
reg q_out,q_b_out;
always @(posedge clk,posedge reset) begin
 if(reset == 0) begin
 if(t==0) begin
 q_out <= q_out;
 q_b_out <= q_b_out;
 end
 if(t==1) begin
 q_out <= ~q_out;
 q_b_out <= ~q_b_out;
 end
 end
 else begin
 q_out <= 0;
 q_b_out <= 1;
 end
end
assign q =q_out;
assign q_b =q_b_out;
endmodule
```

Testbench :

```
`timescale 1 ns/100 ps
```

```
module tb;
 reg t_tin,t_reset,clk;
 wire t_q,t_q_b;
 reg [1:0] i_p [0:2] ;
 integer i;
 initial begin
 $dumpfile("dumpT_FF.vcd");
 $dumpvars(0,tb);
 end

 initial clk=1'b0; always #5 clk =~clk;
 initial begin
 i_p[0]=2'b11;
 i_p[1]=2'b00;
 i_p[2]=2'b01;
 end
 initial {t_reset,t_tin,i} =0;
 tf tf_1(clk,t_reset,t_tin,t_q,t_q_b);
 initial begin
 #10 for(i=0;i<3;i=i+1)
 begin #10 {t_reset,t_tin}=i_p[i]; end
 #40 $finish;
 end
endmodule
```

Compiling files :

```
C:\iverilog\bin>iverilog -o xyz lib.v tff.v tfftb.v

C:\iverilog\bin>vvp xyz
VCD info: dumpfile dumpT_FF.vcd opened for output.

C:\iverilog\bin>gtkwave dumpT_FF.vcd

GTKWave Analyzer v3.3.48 (w)1999-2013 BSI

[0] start time.
[80000] end time.
WM Destroy
```

OUTPUT WAVEFORM: