Assignment-2:

Write a Verilog code and test bench for Flip-Flop, Synchronous Register.

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SECTION : F

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1) D Flip Flop

D Flip Flop Behavioural Model

```
module d_ff (
input clk,d,rst,
output reg q);

   //In Synchronous Reset, Reset condition is verified wrt to clk.
//Here It is verified at every posedge of clk.
   always@(.....)
   begin
      if (.....)
         q <=.....;
      else
         q <=.....;
   end
endmodule
```

SOLUTION :

CODE :

dff_tb - Notepad

File Edit View

```
module dff_tb;
    reg RST, CLK,D;
    wire Q;
            initial
begin
$dumpfile ("dff_test.vcd");
$dumpvars (0, dff_tb );
end

    d_ff DFF (.clk(CLK) ,.rst(RST) ,.q(Q),.d(D));

    initial begin
        RST = 1'b0;
        CLK =1'b0;
        D =1'b0;
        #15 RST = 1'b0;
          #30 RST = 1'b1;
          #45 RST = 1'b0;
          #60 RST = 1'b1;
          #75 RST = 1'b0;
        #100 $finish;
    end

    always #10 CLK = ~CLK;
    always #15 D = ~D;

    always @(posedge CLK )
    $strobe("time =%0t \t INPUT VALUES \t D =%b RST_n =%b \t OUTPUT VALUES Q =%d",$time,D,RST,Q);

endmodule
```

TEST–BENCH file :

dff - Notepad

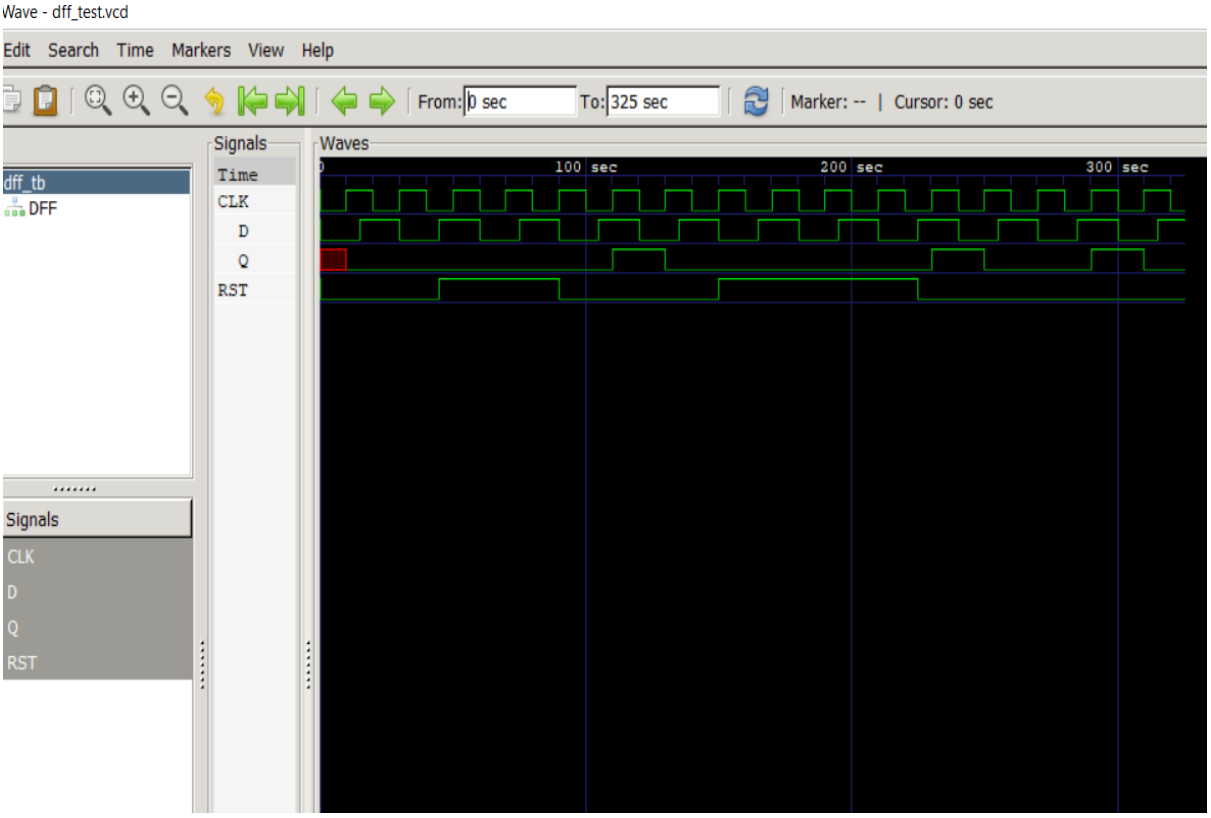
File Edit View

```
module d_ff(input clk , d , rst , output reg q);

//in synchro rest, reser condtn is verified wrt to
     always@(posedge clk)
     begin
          if(rst)
               q <= 1'b0;
          else
               q<= d;
     end


endmodule
```

.vcd :

```
No top level modules, and no -s option.

C:\iverilog\bin>iverilog -o test22 dff.v dff_tb.v

C:\iverilog\bin>vvptest test22
'vvptest' is not recognized as an internal or external command,
operable program or batch file.

C:\iverilog\bin>vvp test22
VCD info: dumpfile dff_test.vcd opened for output.
time =10          INPUT VALUES    D =0 RST_n =0   OUTPUT VALUES Q =0
time =30          INPUT VALUES    D =0 RST_n =0   OUTPUT VALUES Q =0
time =50          INPUT VALUES    D =1 RST_n =1   OUTPUT VALUES Q =0
time =70          INPUT VALUES    D =0 RST_n =1   OUTPUT VALUES Q =0
time =90          INPUT VALUES    D =0 RST_n =0   OUTPUT VALUES Q =0
time =110         INPUT VALUES    D =1 RST_n =0   OUTPUT VALUES Q =1
time =130         INPUT VALUES    D =0 RST_n =0   OUTPUT VALUES Q =0
time =150         INPUT VALUES    D =0 RST_n =1   OUTPUT VALUES Q =0
time =170         INPUT VALUES    D =1 RST_n =1   OUTPUT VALUES Q =0
time =190         INPUT VALUES    D =0 RST_n =1   OUTPUT VALUES Q =0
time =210         INPUT VALUES    D =0 RST_n =1   OUTPUT VALUES Q =0
time =230         INPUT VALUES    D =1 RST_n =0   OUTPUT VALUES Q =1
time =250         INPUT VALUES    D =0 RST_n =0   OUTPUT VALUES Q =0
time =270         INPUT VALUES    D =0 RST_n =0   OUTPUT VALUES Q =0
time =290         INPUT VALUES    D =1 RST_n =0   OUTPUT VALUES Q =1
time =310         INPUT VALUES    D =0 RST_n =0   OUTPUT VALUES Q =0
dff_tb.v:21: $finish called at 325 (1s)

C:\iverilog\bin>
```

GTKWave OUTPUT :



T Flip Flop

T Flip Flop Behavioural Model

```
module t_ff (input clk,rst,t,output reg q);
   always@(.....,.....)
   begin
      if (.....)
         q <= 1'b0;
      else if(.....)
         q <=.....;
      else
         q <=.....;
   end
endmodule
```

CODE :

File Edit View

```
module t_ff (input clk,rst,t,output reg q);
    always@(posedge clk)
    begin
        if (rst)
            q <= 1'b0;
        else if(t)
            q <= ~q;
        else
            q <= q;
    end
endmodule
```

TESTBENCH FILE :

tff_tb - Notepad

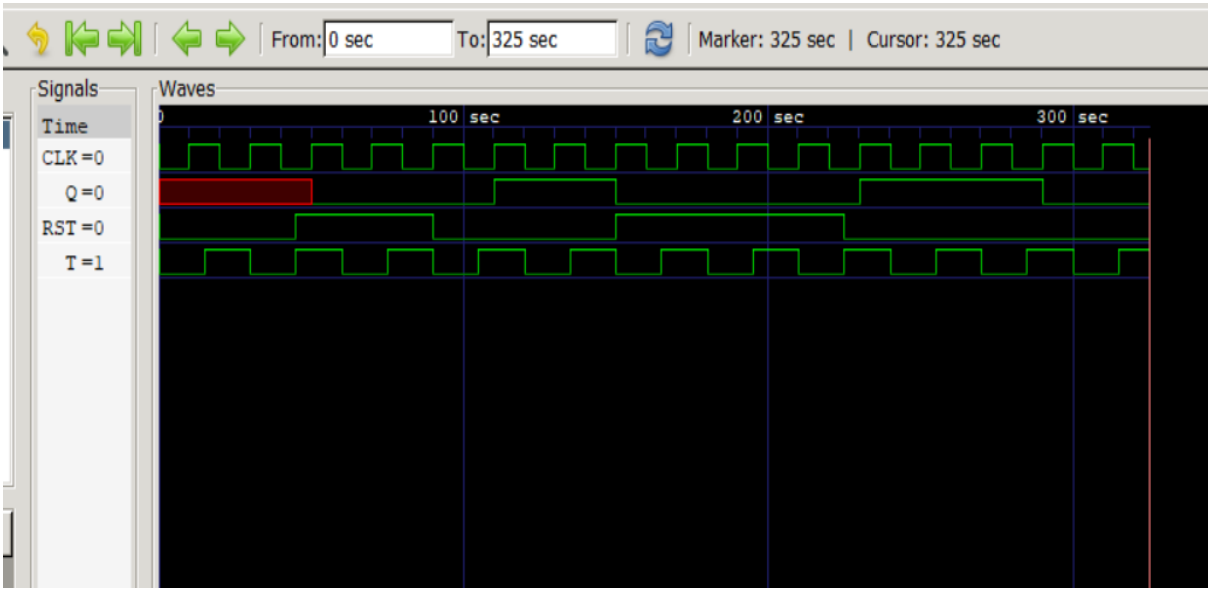
File Edit View

```
module tff_tb;
    reg RST, CLK,T;
    wire Q;
            initial
begin
$dumpfile ("tff_test.vcd");
$dumpvars (0, tff_tb );
end

    t_ff DFF (.clk(CLK) ,.rst(RST) ,.q(Q),.t(T));

    initial begin
        RST = 1'b0;
        CLK =1'b0;
        T=1'b0;
        #15 RST = 1'b0;
         #30 RST = 1'b1;
         #45 RST = 1'b0;
         #60 RST = 1'b1;
         #75 RST = 1'b0;
        #100 $finish;
    end

    always #10 CLK = ~CLK;
    always #15 T= ~T;

    always @(posedge CLK )
    $strobe("time =%0t \t INPUT VALUES \t T =%b RST_n =%b \t OUTPUT VALUES Q =%d",$time,T,RST,Q);

endmodule
```

.vcd :

```
No top level modules, and no -s option.

C:\iverilog\bin>iverilog -o test22 dff.v dff_tb.v

C:\iverilog\bin>vvptest test22
'vvptest' is not recognized as an internal or external command,
operable program or batch file.

C:\iverilog\bin>vvp test22
VCD info: dumpfile dff_test.vcd opened for output.
time =10         INPUT VALUES    D =0 RST_n =0   OUTPUT VALUES Q =0
time =30         INPUT VALUES    D =0 RST_n =0   OUTPUT VALUES Q =0
time =50         INPUT VALUES    D =1 RST_n =1   OUTPUT VALUES Q =0
time =70         INPUT VALUES    D =0 RST_n =1   OUTPUT VALUES Q =0
time =90         INPUT VALUES    D =0 RST_n =0   OUTPUT VALUES Q =0
time =110        INPUT VALUES    D =1 RST_n =0   OUTPUT VALUES Q =1
time =130        INPUT VALUES    D =0 RST_n =0   OUTPUT VALUES Q =0
time =150        INPUT VALUES    D =0 RST_n =1   OUTPUT VALUES Q =0
time =170        INPUT VALUES    D =1 RST_n =1   OUTPUT VALUES Q =0
time =190        INPUT VALUES    D =0 RST_n =1   OUTPUT VALUES Q =0
time =210        INPUT VALUES    D =0 RST_n =1   OUTPUT VALUES Q =0
time =230        INPUT VALUES    D =1 RST_n =0   OUTPUT VALUES Q =1
time =250        INPUT VALUES    D =0 RST_n =0   OUTPUT VALUES Q =0
time =270        INPUT VALUES    D =0 RST_n =0   OUTPUT VALUES Q =0
time =290        INPUT VALUES    D =1 RST_n =0   OUTPUT VALUES Q =1
time =310        INPUT VALUES    D =0 RST_n =0   OUTPUT VALUES Q =0
dff_tb.v:21: $finish called at 325 (1s)

C:\iverilog\bin>
```

GTKWAVE :



JK Flip Flop

JK Flip Flop Behavioural Model

```
module jkff(q,j,k,clk,clr);
input j,k,clk,clr;
output q;
reg q;
always @ (.....)
begin
if(clr==.....)
q<=.....;
else if (j==.....& k==----------)
q<=q;
else if (j==.....& k==----------)
q<=1'b0;
else (j==.....& k==----------)
q<=1'b1;
else if (j==.....& k==----------)
q<=~q;
end
endmodule
```

CODE :

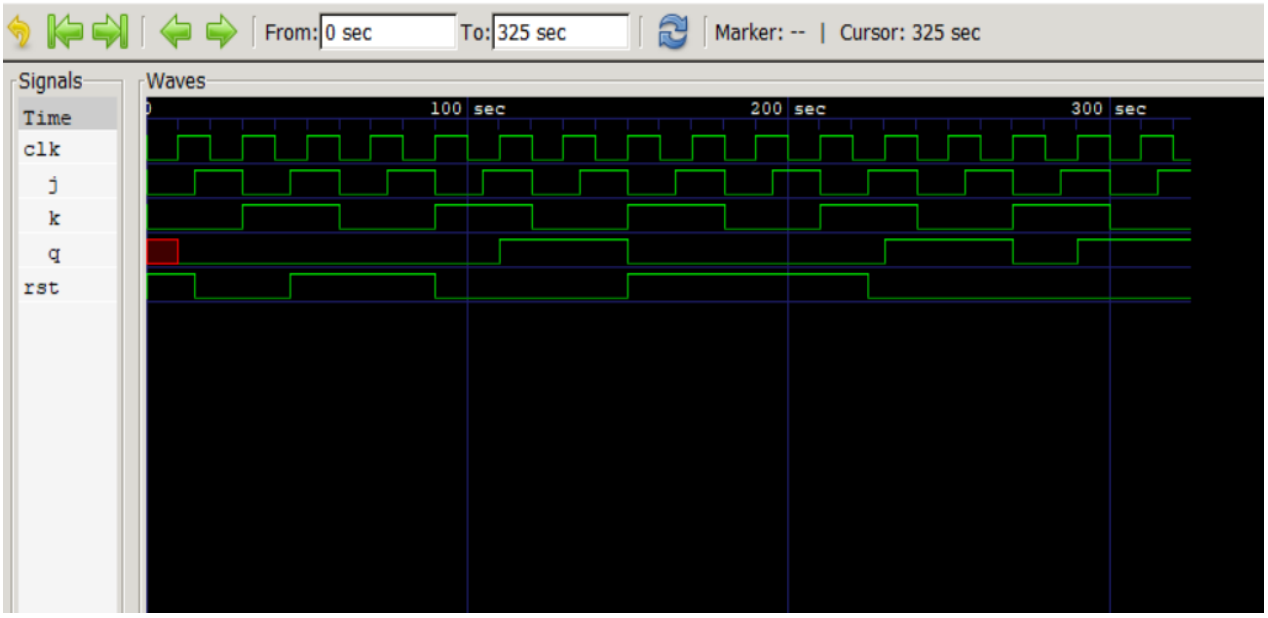
```
module jk_ff(q,j,k,clk,rst);

    input j,k,clk,rst;
    output q;
    reg q;

    always @ (posedge clk)

        begin
        if(rst)
            q<=1'b0;
        else if (j==1'b0 & k==1'b0)
            q<=q;
        else if (j==1'b0 & k==1'b1)
            q<=1'b0;
        else if(j==1'b1 & k==1'b0)
            q<=1'b1;
        else if (j==1'b1 & k==1'b1)
            q<=~q;
    end
endmodule
```

TESTBENCH FILE :

File Edit View

```
module jkff_tb;
    reg RST, CLK,J,K;
    wire Q;
            initial
begin
$dumpfile ("jkff_test.vcd");
$dumpvars (0, jkff_tb );
end

    jk_ff jk_ff (.clk(CLK) ,.rst(RST) ,.q(Q),.j(J),.k(K));

    initial begin
        RST = 1'b1;
        CLK =1'b0;
        J =1'b0;
        K=1'b0;
        #15 RST = 1'b0;
            #30 RST = 1'b1;
            #45 RST = 1'b0;
            #60 RST = 1'b1;
            #75 RST = 1'b0;
                #100 $finish;
    end

    always #10 CLK = ~CLK;
    always #15 J = ~J;
    always #30 K=~K;

    always @(posedge CLK )
    $strobe("time =%0t \t INPUT VALUES \t J =%b K=%b RST_n =%b \t OUTPUT VALUES Q =%d",$time,J,K,RST,Q);

endmodule
```

gtkwave out :



.vcd :

```
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C:\iverilog\bin>iverilog -o te jk_ff.v jk_tb.v

C:\iverilog\bin>vvp te
VCD info: dumpfile jkff_test.vcd opened for output.
time =10         INPUT VALUES    J =0 K=0 RST_n =1       OUTPUT VALUES Q =0
time =30         INPUT VALUES    J =0 K=1 RST_n =0       OUTPUT VALUES Q =0
time =50         INPUT VALUES    J =1 K=1 RST_n =1       OUTPUT VALUES Q =0
time =70         INPUT VALUES    J =0 K=0 RST_n =1       OUTPUT VALUES Q =0
time =90         INPUT VALUES    J =0 K=1 RST_n =0       OUTPUT VALUES Q =0
time =110        INPUT VALUES    J =1 K=1 RST_n =0       OUTPUT VALUES Q =1
time =130        INPUT VALUES    J =0 K=0 RST_n =0       OUTPUT VALUES Q =1
time =150        INPUT VALUES    J =0 K=1 RST_n =1       OUTPUT VALUES Q =0
time =170        INPUT VALUES    J =1 K=1 RST_n =1       OUTPUT VALUES Q =0
time =190        INPUT VALUES    J =0 K=0 RST_n =1       OUTPUT VALUES Q =0
time =210        INPUT VALUES    J =0 K=1 RST_n =1       OUTPUT VALUES Q =0
time =230        INPUT VALUES    J =1 K=1 RST_n =0       OUTPUT VALUES Q =1
time =250        INPUT VALUES    J =0 K=0 RST_n =0       OUTPUT VALUES Q =1
time =270        INPUT VALUES    J =0 K=1 RST_n =0       OUTPUT VALUES Q =0
time =290        INPUT VALUES    J =1 K=1 RST_n =0       OUTPUT VALUES Q =1
time =310        INPUT VALUES    J =0 K=0 RST_n =0       OUTPUT VALUES Q =1
jk_tb.v:22: $finish called at 325 (1s)

C:\iverilog\bin>
```

SR Flip Flop

SR Flip Flop Behavioural Model

```
module srff_behave(s,r,clk, q, qbar);
input s,r,clk;
output reg q, qbar;
always@((.....))
if(.....)
begin
q =.....;
qbar =.....;
end
else if(.....)
begin
q =.....;
qbar =.....;
end
```

else if(.....)
begin
q <=.....;
qbar <=.....;
end
end
endmodule

CODE :

```
module srff(s,r,clk, q, qbar);
     input s,r,clk;
     output reg q, qbar;
always@(posedge clk)
     if(s==1)
          begin
          q = 1;
          qbar = 0;
end
     else if(r==1)
begin
          q = 0;
          qbar =1;
end
     else if(s==0 && r==0)
begin
     q <= q;
     qbar <= qbar;
end
endmodule
```

TESTBENCH FILE :

```
module srff_tb;
    reg  CLK,S,R;
    wire Q,QBAR;
            initial
begin
$dumpfile ("srff_test.vcd");
$dumpvars (0, srff_tb );
end
    srff DFF (.clk(CLK),.q(Q),.qbar(QBAR),.s(S),.r(R));

    initial begin
         CLK =1'b1;
        S =1'b0;
        R=1'b0;
              #100 $finish;
    end
    always #10 CLK = ~CLK;
    always #15 S = ~S;
always #20 R = ~R;


    always @(posedge CLK )
    $strobe("time =%0t \t INPUT VALUES \t S=%b  R=%b \t OUTPUT VALUES Q =%d QBAR=%d",$time,S,R,Q,QBAR);
endmodule
```

GTKWAVE :

.vcd :

```
module srff(s,r,clk, q, qbar);
     input s,r,clk;
     output reg q, qbar;
always@(posedge clk)
     if(s==1)
          begin
          q = 1;
          qbar = 0;
end
     else if(r==1)
begin
          q = 0;
          qbar =1;
end
     else if(s==0 && r==0)
begin
     q <= q;
     qbar <= qbar;
end
endmodule
```

THANKING YOU MAA'M!

SRN : PES2UG21CS361