Write a Verilog program to implement the following using only gate-level or structural modeling:

1. Ripple Carry Adder using full adders(Use hierarchical modeling) //4 bit adder
2. 8-Bit Ripple Carry Adder using full adders.
3. BCD adder with four-bit numbers.
4. BCD to Excess-3 convertor.
5. Half subtractor.
6. Full subtractor.

Essential instructions for submission:

* All the students must submit the Verilog Code for all the problems with the corresponding test bench mentioning their serial numbers in a single .doc/.docx/pdf file with respective roll numbers(<rollnumber.doc/.docx/pdf>)
* All the submissions must be individual efforts. If anybody shares/receives the code with their friends/colleagues, it will be treated as plagiarism and awarded an F grade.
* Late submissions (or resubmitted ones) will be treated as void and not eligible for taking the corresponding assignment exam and will award null marks for the evaluation.