Write a Verilog program to implement the following using only universal gates (Use hierarchical modeling):



1. 4-bit Incrementer



1. 4-bit Decrementer



1. 16-bit Incrementer



1. 16-bit Decrementer



1. 4-bit Negator (Hint: input: x output:!x)



1. 16-bit Negator (Hint: input: x output:!x)



1. S-R Latch
2. Gated S-R Latch



1. Arithmetic-Logic Unit with the following functions on two 16-bit inputs (x, y):
   * + a.       x+y



* + - b.       x-y



* + - c.       y-x



* + - d.       0



* + - e.       1



* + - f.        -1



* + - g.       -x



* + - h.       -y



* + - i.        !x



* + - j.        !y



* + - k.       x+1



* + - l.        y+1



* + - m.      x-1



* + - n.       y-1



* + - o.       x&y



* + - p.       x|y



Essential instructions for submission:

* All the students must submit the Verilog Code for all the problems with the corresponding test bench mentioning their serial numbers and sub-parts, if any, in a single .doc/.docx/pdf file with respective roll numbers(<rollnumber.doc/.docx/pdf>)
* All the submissions must be individual efforts. If anybody shares/receives the code with their friends/colleagues, it will be treated as plagiarism and awarded an F grade.
* Late submissions (or resubmitted ones) will be treated as void and not eligible for taking the corresponding assignment exam and will award null marks for the evaluation.