1. Write a Verilog program to implement the following logic designs using behavioral modeling:

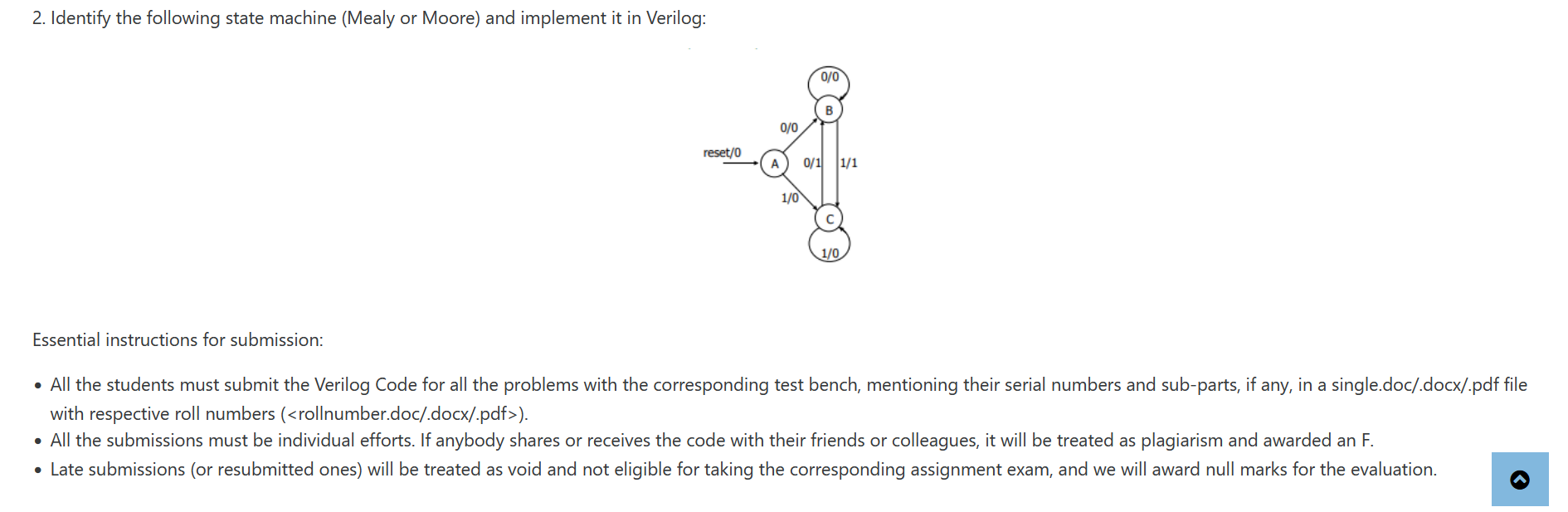
a)      D flip-flop with asynchronous preset and clear

b)      Clocked D latch (Level triggering) with asynchronous preset and clear

c)      8-bit Shift Register



d)      8-bit Register

e)      Multiplier (4×4) using full adders

