

## 8-bit enhanced USB microcontroller CH552, CH551

manual

Version: 1H

<http://wch.cn>

### 1. Overview

The CH552 chip is an enhanced E8051 core microcontroller compatible with the MCS51 instruction set. 79% of its instructions are single-byte single-cycle.

The average instruction speed is 8 to 15 times faster than the standard MCS51.

CH552 supports up to 24MHz system frequency, built-in 16K program memory ROM and 256 bytes internal iRAM and 1K bytes

On-chip xRAM, xRAM supports DMA direct memory access.

CH552 has built-in ADC analog-to-digital conversion, touch button capacitance detection, 3 groups of timers and signal capture and PWM, dual asynchronous serial ports, Functional modules such as SPI, USB device controller and full-speed transceiver.

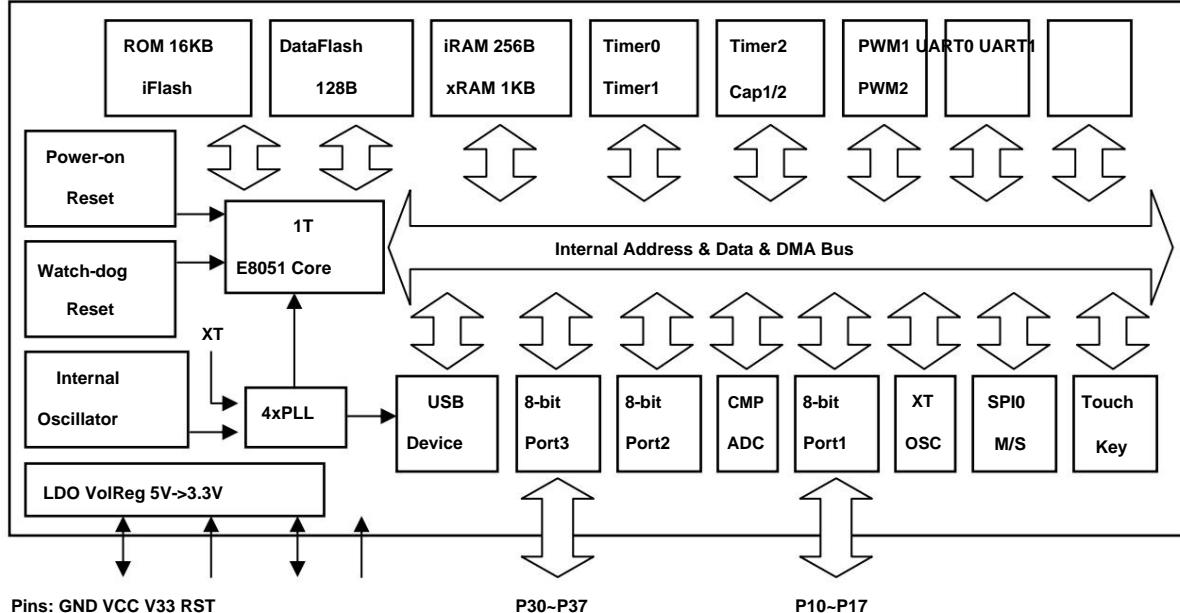
CH551 is a simplified version of CH552, with 10K program memory ROM, 512 bytes on-chip xRAM, and only UART0 asynchronous serial port.

The package is only SOP16, the touch button is only 4 channels, and the ADC analog-to-digital conversion module and USB type-C module are removed.

The CH552 is the same as the CH551, so you can directly refer to the CH552 manual and information.

Model	Program ROM	RAM	DataFlash	USB device	type-C	Timer	PWM	Serial port	SPI	ADC	Touch button		
CH552	16KB	1280				128 Full/Low Speed	Configurable				2 groups	Master/Slave	4-way 6-channel
CH551	10KB	768									1 group		No 4 channels

The following is the internal block diagram of CH552, for reference only.



### 2. Features

I Core: Enhanced E8051 core, compatible with MCS51 instruction set, 79% of its instructions are single-byte single-cycle instructions, average instruction

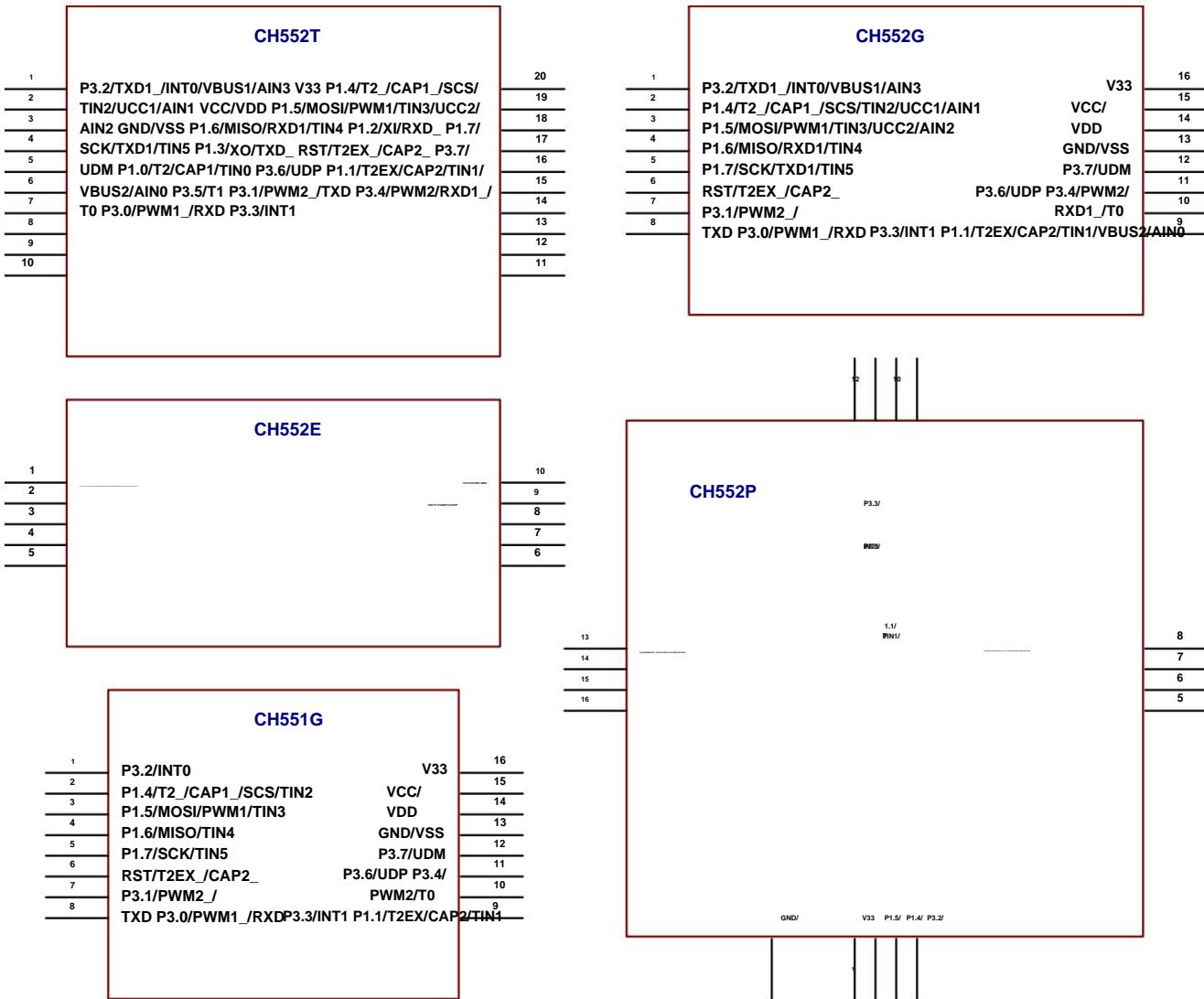
The speed is 8 to 15 times faster than the standard MCS51, with unique XRAM data fast copy instructions and dual DPTR pointers.

- I ROM: 16KB of multi-programmable non-volatile memory ROM, which can be used entirely for program storage; or can be divided into It has 14KB program storage area and 2KB boot code BootLoader/ISP program area.
- I DataFlash: 128 bytes of non-volatile data memory that can be repeatedly erased and written, supporting data rewriting in byte units.
- I RAM: 256 bytes of internal iRAM, which can be used for fast data storage and stack; 1KB of on-chip xRAM, which can be used for large amounts of data Data cache and DMA direct memory access.
- I USB: embedded USB controller and USB transceiver, supports USB-Device device mode, supports USB type-C master-slave detection, Supports USB 2.0 full speed 12Mbps or low speed 1.5Mbps. Supports data packets up to 64 bytes, built-in FIFO, and supports DMA.
- I Timer: 3 groups of timers, T0/T1/T2 are standard MCS51 timers.
- I Capture: Timer T2 is expanded to support 2-way signal capture.
- I PWM: 2 groups of PWM outputs, PWM1/PWM2 are 2-channel 8-bit PWM outputs.
- I UART: 2 sets of asynchronous serial ports, both support higher communication baud rate, UART0 is a standard MCS51 serial port.
- I SPI: SPI controller has built-in FIFO, the clock frequency can reach half of the system main frequency Fsys, and supports serial data input and output Simplex multiplexing, supports Master/Slave mode.
- I ADC: 4-channel 8-bit A/D analog-to-digital converter, supporting voltage comparison.
- I Touch-Key: 6-channel capacitance detection, supports up to 15 touch keys, and supports independent timer interrupts.
- I GPIO: supports up to 17 GPIO pins (including XI/XO and RST and USB signal pins).
- I Interrupt: supports 14 groups of interrupt signal sources, including 6 groups of interrupts compatible with standard MCS51 (INT0, T0, INT1, T1, UART0, T2), and extended 8 groups of interrupts (SPI0, TKEY, USB, ADC, UART1, PWMX, GPIO, WDOG), The GPIO interrupt can be selected from 7 pins.
- I Watch-Dog: 8-bit preset watchdog timer WDOG, supporting timer interrupt.
- I Reset: supports 4 reset signal sources, built-in power-on reset, support software reset and watchdog overflow reset, optional pin external reset Internal input reset.
- I Clock: Built-in 24MHz clock source, can support external crystal by multiplexing GPIO pins.
- I Power: Built-in 5V to 3.3V low voltage dropout voltage regulator, supports 5V or 3.3V power supply voltage. Supports low power sleep, Supports external wakeup of USB, UART0, UART1, SPI0 and some GPIOs.
- I The chip has a built-in unique ID number.

### 3. Encapsulation

Package	Body width		Pin pitch		Package Description	Order Model
TSSOP-20	4.40mm	173mil	0.65mm	25mil thin and small 20-pin SMD CH552T 50mil	standard 16-pin	
SOP-16	3.9mm	150mil	1.27mm	SMD CH552G 19.7mil four-side leadless 16-pin	CH552P 19.7mil	
QFN-16	3*3mm		0.50mm	micro-miniature 10-pin SMD CH552E 50mil standard	16-pin SMD	
MSOP-10	3.0mm	118mil	0.50mm	CH551G		
SOP-16	3.9mm	150mil	1.27mm			

Note: CH543 and CH548 chips are recommended for new designs; CH552E is not recommended for new designs.



## 4. Pins

Pin Number			Pins name	Other function names (Left function takes priority)	Other function description
TSSOP20	SOP16	QFN16			
19	15	16	VCC/VDD		The power input terminal requires an external 0.1uF power decoupling capacitor.
20	16	1	V33		Internal USB power regulator output and internal USB power input, When the power supply voltage is less than 3.6V, connect VCC to input external power supply. When the power supply voltage is greater than 3.6V, connect an external 0.1uF power decoupling capacitor
18	14	0 baseplate	GND VSS		Common ground terminal.
6	6	7	RST RST/T2EX_ /CAP2_	Pins with an underscore suffix are a reflection of the pins with the same name without an underscore.	
7	-	8 P1.0	T2/CAP1/TIN0	RST pin has a built-in pull-down resistor; other GPIOs have pull-up resistors by default.	
8	9	11 P1.1	T2EX/CAP2/TIN1 /VBUS2/AIN0	RST: External reset input. T2: External count input/clock output of timer/counter 2.	
17	-	- P1.2 XI/RXD_ - P1.3 XO/TXD_		T2EX: Timer/Event Counter 2 reload/capture input.	
16	-			CAP1, CAP2: Capture input 1, 2 of timer/counter 2.	
2	2	3 P1.4	T2_/_CAP1_/_SCS /TIN2/UCC1/AIN1	TIN0-TIN5: 0#-5# channel touch button capacitance detection input. AIN0-AIN3: 0#-3# channel ADC analog signal input.	

3	3	2 P1.5		MOSI/PWM1/TIN3 /UCC2/AIN2	UCC1, UCC2: USB type-C bidirectional configuration channels. VBUS1, VBUS2: USB type-C bus voltage detection input.
4	4	5 P1.6	MISO/RXD1/TIN4		XI, XO: External crystal oscillator input and inverting output.
5	5	6 P1.7	SCK/TXD1/TIN5		RXD, TXD: UART0 serial data input, serial data output.
10	8	10 P3.0	PWM1_/_RXD P3.1 PWM2_/_		SCS, MOSI, MISO, SCK: SPI0 interface, SCS is the chip select input
9	7	9	TXD		MOSI is the master output/slave input, MISO is the master input
1	1	4 P3.2		TXD1_/_INT0 /VBUS1/AIN3	/Slave output, SCK is the serial clock. PWM1, PWM2: PWM1 output, PWM2 output.
11	10	12 P3.3	INT1		RXD1, TXD1: UART1 serial data input, serial data output.
12	11	13 P3.4	PWM2/RKD1_/_T0		INT0, INT1: external interrupt 0, external interrupt 1 input.
13		- P3.5	T1		T0, T1: Timer 0, Timer 1 external input.
14	12	14 P3.6	UDP		UDM, UDP: D-, D+ signal terminals of USB devices.
15	13	15 P3.7	UDM		Note: P3.6 and P3.7 use V33 as I/O power supply internally. The high level of its input and output can only reach V33 voltage, and does not support 5V

Note: The USB transceiver is designed to be fully integrated with USB2.0. Resistors cannot be connected in series when the P3.6 and P3.7 pins are used for USB.

## 5. Special Function Register SFR

The following abbreviations may be used in this manual when describing registers:

Abbreviations	describe
RO	Indicates access type: read-only
WHERE	Indicates access type: write-only, read values are invalid
RW	Indicates access type: readable and writable
H	It ends with a hexadecimal number.
B	End with this to represent a binary number

### 5.1 SFR Introduction and Address Distribution

CH552 uses special function registers (SFRs) to control and manage devices and set working modes.

SFR occupies the address range of 80h-FFh in the internal data memory space and can only be accessed through direct address instructions.

Registers with addresses x0h or x8h are bit-addressable, which avoids modifying the values of other bits when accessing a specific bit;

Other registers whose addresses are not multiples of 8 can only be accessed by byte.

Some SFRs can only be written in safe mode and are read-only in non-safe mode, for example: GLOBAL\_CFG,

CLOCK\_CFG\_/\_WAKE\_CTRL\_/\_

Some SFRs have one or more aliases, for example: SPI0\_CK\_SE/SPI0\_S\_PRE.

Some addresses correspond to multiple independent SFRs, such as SAFE\_MOD/CHIP\_ID, ROM\_CTRL/ROM\_STATUS.

CH552 contains the 8051 standard SFR registers, and also adds other device control registers. Specific SFRs are shown in the table below.

Table 5.1 Special Function Register Table

SFR 0y8		1y9	2yA	3yB	4yC	5yD	6yAnd	7yF
0xF8	<b>SPI0_STAT</b>	<b>SPI0_DATA</b>	<b>SPI0_CTRL</b>	<b>SPI0_CK_SE</b> <b>SPI0_S_PRE</b>	<b>SPI0_SETUP</b>		<b>RESET_KEEP</b>	<b>WDOG_COUNT</b>
0xF0	<b>B</b>							
0xE8	<b>IE_EX</b>	<b>IP_EX</b>	<b>UEP4_1_MOD</b>	<b>UEP2_3_MOD</b>	<b>UEP0_DMA_L</b>	<b>UEP0_DMA_H</b>	<b>UEP1_DMA_L</b>	<b>UEP1_DMA_H</b>
0xE0	<b>ACC</b>	<b>USB_INT_EN</b>	<b>USB_CTRL</b>	<b>USB_DEV_AD</b>	<b>UEP2_DMA_L</b>	<b>UEP2_DMA_H</b>	<b>UEP3_DMA_L</b>	<b>UEP3_DMA_H</b>
0xD8	<b>USB_INT_FG</b>	<b>USB_INT_ST</b>	<b>USB_MIS</b>	<b>ST_USB_RX_LEN</b>	<b>UEP0_CTRL</b>	<b>UEP0_T_LEN</b>	<b>UEP4_CTRL</b>	<b>UEP4_T_LEN</b>

0xD0	<b>PSW</b>	UDEV_CTRL UEP1	CTRL UEP1_T_LEN	UEP2_CTRL UEP2_T_LEN	UEP3_CTRL UEP3_T_LEN			
0xC8	<b>T2CON</b>	T2MOD	RCAP2L	RCAP2L	TL2	TH2	T2CAP1L	T2CAP1H
0xC0	<b>SCON1</b>	SBUF1	SBAUD1	TKEY_CTRL TKEY	DATL TKEY_DATH		PIN_FUNC	GPIO_IE
0xB8	<b>IP</b>	CLOCK_CFG						
0xB0	<b>P3</b>	GLOBAL_CFG						
0xA8	<b>IE</b>	WAKE_CTRL						
0xA0	<b>P2</b>	SAFE_MOD CHIP_ID	XBUS_AUX					
0x98	<b>SCON</b>	SBUF	ADC_CFG	PWM_DATA2_PWM	DATA1	PWM_CTRL	PWM_CK_SE	ADC_DATA
0x90	<b>P1</b>	USB_C_CTRL P1_M	MOD_OC P1_DIR_PU				P3_MOD_OC P3_DR_PU	
0x88	<b>TCON</b>	TMOD	TL0	TL1	TH0	TH1	ROM_DATA_L ROM_DATA_H	
0x80	<b>ADC_CTRL</b>	SP	DPL	VAT	ROM_ADDR_L ROM_ADDR_H		ROM_CTRL ROM_STATUS	PCON

Note: (1) Red text indicates bit-wise addressing; (2) The following are the corresponding descriptions of the color boxes

	Register address
	SPI0 related registers
	ADC related registers
	Touch-Key related registers
	USB related registers
	Timer/Event Counter 2 Related Registers
	Port setting related registers
	PWM1 and PWM2 related registers
	UART1 related registers
	Flash-ROM related registers

## 5.2 SFR Classification and Reset Values

Table 5.2 SFR description and reset value

Functional classification	name address		describe	Reset value
System Settings Related registers	B	F0h	B register	0000 0000b
	ACC	E0h	accumulator	0000 0000b
	PSW	D0h	Program Status Register	0000 0000b
	GLOBAL_CFG	B1h	Global configuration register (CH552 bootloader state) 1010 0000b	
			Global configuration register (CH552 application state) 1000 0000b	
			Global configuration register (CH551 bootloader state) 1110 0000b	
			Global configuration register (in CH551 application state) 1100 0000b	
	CHIP_ID	A1h	CH552 chip ID identification code (read only)	0101 0010b
			CH551 chip ID identification code (read only)	0101 0001b
	SAFE_MOD	A1h	Security Mode Control Register (Write Only)	0000 0000b
	VAT	83h	Data Address Pointer High 8 bits 82h	0000 0000b
	DPL	82h	Data Address Pointer Low 8 bits 82h DPL	0000 0000b
	DPTR	81h	and DPH form a 16-bit SFR 81h Stack Pointer	0000h
	SP			0000 0111b
Clock, Sleep WDOG	COUNT	FFh	Watchdog count register	0000 0000b

and power control Related registers	RESET_KEEP	FEh Reset holding register (power-on reset state)	0000 0000b
	CLOCK_CFG	B9h System Clock Configuration Register	1000 0011b
	WAKE_CTRL	A9h Sleep wake-up control register	0000 0000b
	PCON	87h Power control register (power-on reset state)	0001 0000b
Interrupt Control Related registers	IP_EX	E9h Extended Interrupt Priority Control Register	0000 0000b
	IE_EX	E8h Extended Interrupt Enable Register	0000 0000b
	GPIO_IE	C7h GPIO Interrupt Enable Register	0000 0000b
	IP	B8h Interrupt Priority Control Register	0000 0000b
	IE	A8h Interrupt Enable Register	0000 0000b
Flash-ROM Related registers	ROM_DATA_H	8Fh flash-ROM data register high byte	xxxx xxxx b
	ROM_DATA_L	8Eh flash-ROM data register low byte	xxxx xxxx b
	ROM_DATA	8Eh ROM_DATA_L and ROM_DATA_H form a 16-bit SFR 86h flash-	xxxx
	ROM_STATUS	ROM status register (read only) 86h flash-ROM	0000 0000b
	ROM_CTRL	control register (write only) 85h flash-ROM address	0000 0000b
	ROM_ADDR_H	register high byte 84h flash-ROM address register	xxxx xxxx b
	ROM_ADDR_L	low byte 84h ROM_ADDR_L and ROM_ADDR_H	xxxx xxxx b
	ROM_ADDR	form a 16-bit SFR	xxxx h
Port Settings Related registers	PIN_FUNC	C6h Pin Function Select Register	1000 0000b
	XBUS_AUX	A2h External Bus Auxiliary Setting Register	0000 0000b
	P3_DIR_PU	97h P3 Port Direction Control and Pull-up Enable Register	1111 1111b
	P3_MOD_OC	96h P3 Port Output Mode Register 93h P1	1111 1111b
	P1_DIR_PU	Port Direction Control and Pull-up Enable Register 92h P1	1111 1111b
	P1_MOD_OC	Port Output Mode Register	1111 1111b
	P3	B0h P3 port input and output register	1111 1111b
	P2	A0h P2 port output register 90h P1	1111 1111b
	P1	port input and output register	1111 1111b
Timer/Counter 0 and 1 related registers	TH1	8Dh Timer1 count high byte	xxxx xxxx b
	TH0	8Ch Timer0 count high byte	xxxx xxxx b
	TL1	8Bh Timer1 count low byte	xxxx xxxx b
	TL0	8Ah Timer0 count low byte 89h	xxxx xxxx b
	TMOD	Timer0/1 mode register 88h Timer0/1	0000 0000b
	TCON	control register 99h UART0 data register	0000 0000b
UART0 Related registers	SBUF	98h UART0 control register	xxxx xxxx b
	SCON		0000 0000b
Timer/Counter 2 Related registers	T2CAP1H	CFh Timer2 capture 1 data high byte (read only)	xxxx xxxx b
	T2CAP1L	CEh Timer2 capture 1 data low byte (read only)	xxxx xxxx b
	T2CAP1	CEh T2CAP1L and T2CAP1H form a 16-bit SFR	xxxx
	TH2	CDh Timer2 counter high byte	0000 0000b
	TL2	CCh Timer2 counter low byte	0000 0000b
	T2COUNT	CCh TL2 and TH2 form a 16-bit SFR	0000h
	RCAP2H	CBh Count Reload/Capture 2 Data Register High Byte	0000 0000b
	RCAP2L	CAh Count Reload/Capture 2 Data Register Low Byte	0000 0000b
	RCAP2	CAh RCAP2L and RCAP2H form a 16-bit SFR	0000h

	T2MOD	C9h Timer2 Mode Register	0000 0000b
	T2CON	C8h Timer2 Control Register	0000 0000b
PWM1 and PWM2 Related registers	PWM_CK_SE	9Eh PWM clock frequency division setting register	0000 0000b
	PWM_CTRL	9Dh PWM Control Register	0000 0010b
	PWM_DATA1	9Ch PWM1 data register	xxxx xxxx b
	PWM_DATA2	9Bh PWM2 Data Register	xxxx xxxx b
SPI0 Related registers	SPI0_SETUP	FCh SPI0 Setup Register	0000 0000b
	SPI0_S_PRE	FBh SPI0 slave mode preset data register	0010 0000b
	SPI0_CK_SE	FBh SPI0 clock division setting register	0010 0000b
	SPI0_CTRL	FAh SPI0 Control Register	0000 0010b
	SPI0_DATA	F9h SPI0 data transmit and receive register	xxxx xxxx b
	SPI0_STAT	F8h SPI0 Status Register	0000 1000b
UART1 Related registers	SBAUD1	C2h UART1 baud rate setting register	xxxx xxxx b
	SBUF1	C1h UART1 data register	xxxx xxxx b
	SCON1	C0h UART1 Control Register	0100 0000b
ADC Related registers	ADC_DATA	9Fh ADC Data Register	xxxx xxxx b
	ADC_CFG	9Ah ADC Configuration	0000 0000b
	ADC_CTRL	Register 80h ADC Control Register	x000 0000b
Touch-Key related registers	TKEY_DATH	C5h Touch-Key data high byte (read only)	0000 0000b
	TKEY_DATL	C4h Touch-Key data low byte (read only)	xxxx xxxx b
	TKEY_DAT	C4h TKEY_DATL and TKEY_DATH form a 16-bit SFR	00xxh
	TKEY_CTRL	C3h Touch-Key Control Register	x000 0000b
USB Related registers	UEP1_DMA_H	EFh Endpoint 1 buffer start address high byte	0000 00xxb
	UEP1_DMA_L	EEh Endpoint 1 buffer start address low byte	xxxx xxxx b
	UEP1_DMA	EEh UEP1_DMA_L and UEP1_DMA_H form a 16-bit SFR	0xxxh
	UEP0_DMA_H	EDh Endpoint 0 and 4 buffer start address high byte	0000 00xxb
	UEP0_DMA_L	ECh endpoint 0 and 4 buffer start address low byte	xxxx xxxx b
	UEP0_DMA	ECh UEP0_DMA_L and UEP0_DMA_H form a 16-bit SFR	0xxxh
	UEP2_3_MOD	EBh Endpoint 2, 3 mode control register	0000 0000b
	UEP4_1_MOD	EAh Endpoint 1, 4 mode control register	0000 0000b
	UEP3_DMA_H	E7h Endpoint 3 buffer start address high byte	0000 00xxb
	UEP3_DMA_L	E6h Endpoint 3 buffer start address low byte	xxxx xxxx b
	UEP3_DMA	E6h UEP3_DMA_L and UEP3_DMA_H form a 16-bit SFR	0xxxh
	UEP2_DMA_H	E5h Endpoint 2 buffer start address high byte	0000 00xxb
	UEP2_DMA_L	E4h Endpoint 2 buffer start address low byte	xxxx xxxx b
	UEP2_DMA	E4h UEP2_DMA_L and UEP2_DMA_H form a 16-bit SFR	0xxxh
	USB_DEV_AD	E3h USB device address register	0000 0000b
	USB_CTRL	E2h USB Control Register	0000 0110b
	USB_INT_EN	E1h USB interrupt enable register	0000 0000b
	UEP4_T_LEN	DFh Endpoint 4 Send Length Register	0xxx xxxx b
	UEP4_CTRL	DEh Endpoint 4 Control Register	0000 0000b
	UEP0_T_LEN	DDh Endpoint 0 Send Length Register	0xxx xxxx b
	UEP0_CTRL	DCh Endpoint 0 Control Register	0000 0000b

	USB_RX_LEN	DBh USB receive length register (read only)	0xxx xxxx b
	USB_MIS_ST	DAh USB Miscellaneous Status Register (read only)	xx10 1000 b
	USB_INT_ST	D9h USB interrupt status register (read only)	00xx xxxx b
	USB_INT_FG	D8h USB Interrupt Flag Register	0010 0000 b
	UEP3_T_LEN	D7h Endpoint 3 Send Length Register	0xxx xxxx b
	UEP3_CTRL	D6h Endpoint 3 Control Register	0000 0000 b
	UEP2_T_LEN	D5h Endpoint 2 Send Length Register	0000 0000 b
	UEP2_CTRL	D4h Endpoint 2 Control Register	0000 0000 b
	UEP1_T_LEN	D3h Endpoint 1 Send Length Register	0xxx xxxx b
	UEP1_CTRL	D2h Endpoint 1 Control Register	0000 0000 b
	UDEV_CTRL	D1h USB device port control register 91h USB	10xx 0000 b
	USB_C_CTRL	type-C configuration channel control register	0000 0000 b

### 5.3 General 8051 Registers

Table 5.3.1 General 8051 register list

name	address	describe	Reset value
B	F0h	B register	00h
A/ACC	E0h	accumulator	00h
PSW	D0h	Program Status Register	00h
GLOBAL_CFG	B1h	Global Configuration Register (CH552 in Boot Program)	A0h
		(State) Global Configuration Register (CH552 in Application)	80 hours
		(State) Global Configuration Register (CH551 in Boot)	Yes
		Program State) Global Configuration Register (CH551 in Application State)	C0h
CHIP_ID	A1h	CH552 chip ID identification code (read only)	52h
		CH551 chip ID identification code (read only)	51h
SAFE_MOD	A1h	Security Mode Control Register (Write Only)	00h
PCON	87h	Power Control Register (Power-On Reset) 83h Data	10h
VAT	Address	Pointer High 8 bits 82h Data	00h
DPL	Address	Pointer Low 8 bits 82h DPL and	00h
DPTR	DPH	form a 16-bit SFR 81h Stack Pointer	0000h
SP			07h

B register (B):

Bit Name Access [7:0]		describe	Reset value
	B	RW Arithmetic operation register, mainly used for multiplication and division operations, can be addressed by bit 00h	

A accumulator (A, ACC):

Bit Name Access [7:0]		describe	Reset value
	A/ACC	RW Arithmetic operation accumulator, bit addressable	00h

Program Status Register (PSW):

Bit name access		describe	Reset value
7	EN	RW Carry flag: used to record the highest bit 0 when executing arithmetic and logical operation instructions	

			Carry or borrow; when performing 8-bit addition, if the highest bit carries, the bit is set. Otherwise it is cleared to zero; when performing 8-bit subtraction, if there is a borrow, the bit is set, otherwise it is cleared to zero; Logical instructions can set or clear this bit.	
6	AC	RW	Auxiliary carry flag: records whether there is a carry or borrow from the lower 4 bits to the upper 4 bits during addition and subtraction operations. AC is set, otherwise it is cleared	0
5	F0	RW Bit	addressable general flag bit 0: User-defined, software cleared or set to 0	
4	RS1	RW Register bank select bit high		0
3	RS0	RW register bank selection bit low		0
2	OV	RW	overflow flag: during addition and subtraction operations, if the result exceeds 8 bits of binary number, OV is set. 1, flag overflow, otherwise clear to 0	0
1	F1	RW Bit	addressable general flag 1: User-defined, can be cleared or set to 0 by software	Parity flag: records the parity of
0	P	RO	1 in accumulator A after the instruction is executed. If there are an odd number of 1s, P Set, an even number of 1s will clear P	0

The processor status is stored in the status register PSW, which supports bit addressing. The status word includes a carry flag, which is used to Auxiliary carry flag, parity flag, overflow flag for BCD code processing, and RS0 and RS1 for working register bank selection.

The area where the working register group is located can be accessed directly or indirectly.

Table 5.3.2 RS1 and RS0 working register bank selection table

RS1		RS0	Working register set
0		0	Group 0 (00h-07h)
0		1	Group 1 (08h-0Fh)
1		0	2 groups (10am-5pm)
1		1	3 groups (18h-1Fh)

Table 5.3.3 Operations affecting flags (X indicates the flag is related to the result of the operation)

operate	EN	OV	AC	operate	EN	OV	AC
ADD	X	X	X	SETB C	1		
ADDC	X	X	X	CLR C	0		
SUBB	X	X	X	CPL C	X		
I	0	X		MOV C, bit	X		
DIV	0	X		ANL C, bit	X		
AND A	X			ANL C,/bit	X		
RRC A	X			ORL C, bit	X		
RLC A	X			ORL C,/bit	X		
CJNE	X						

#### Data address pointer (DPTR):

Bit name	access		describe	Reset value
[7:0]	DPL	RW Data pointer low byte		00h
[7:0]	VAT	RW Data pointer high byte		00h

DPL and DPH form a 16-bit data pointer DPTR, which is used to access the xRAM data memory or program memory.

Corresponding to the two physical 16-bit data pointers DPTR0 and DPTR1, they are dynamically selected by DPS in XBUS\_AUX.

#### Stack Pointer (SP):

Bit name	access		describe	Reset value

[7:0]	SP	RW stack pointer, mainly used for program calls and interrupt calls as well as data in and out of the stack 07h	
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The specific functions of the stack are to protect breakpoints and scenes, and to manage them according to the principle of first in, last out. When the stack is pushed, the SP pointer is automatically increased by 1.

Save data or breakpoint information; when popping the stack, the SP pointer points to the data unit and the SP pointer automatically decreases by 1. The initial value of SP after reset is 07h.

The corresponding default stack memory starts at 08h.

## 5.4 Special registers

Global configuration register (GLOBAL\_CFG), writable only in safe mode:

Bit	Name Access [7:6]		describe	Reset value
Reserved	RO For CH552, the fixed value is 10	[7:6] Reserved RO For CH551, the fixed value		10b
is 11				11b
5	bBOOT_LOAD	RO	Boot loader status bit, used to distinguish ISP boot program status or application  Program status: set to 1 when power is turned on and cleared to 0 when the software is reset.  For chips with ISP bootloader, this bit is 1, indicating that it has never been reset by software.  The ISP boot program is usually running after power on; this bit is 0  Indicates that the software has been reset, usually the application status	1
4	bSW_RESET	RW Software	reset control bit: Setting it to 1 causes software reset, and the hardware	0
3	bCODE_WE	RW	automatically clears the Flash-ROM and DataFlash write enable bits:  If this bit is 0, it is write protected; if it is 1, Flash-ROM and Data can rewrite the	0
2	bDATA_WE	RW	DataFlash area of Flash-ROM. Write enable bit:  If this bit is 0, it is write protected; if it is 1, the DataFlash area can rewrite the USB	0
1	bLDO3V3_OFF	RW	power regulator LDO disable control bit:  If this bit is 0, LDO is enabled and 3.3V voltage can be generated from 5V power supply for USB and internal clock oscillator;  If it is 1, LDO is disabled and the V33 pin must be connected to an external 3.3V power supply.	0
0	bWDOG_EN	RW	Watchdog reset enable bit: When this bit is 0, the watchdog is only used as a timer;  Set to 1 to enable watchdog reset when timer overflows	0

Chip ID identification code (CHIP\_ID):

Bit name	access		describe	Reset value
[7:0]	CHIP_ID	RO For CH552, it is a fixed value of 52h, used to identify the chip		52h
[7:0]	CHIP_ID	RO For CH551, it is a fixed value 51h, used to identify the chip		51h

Safe Mode Control Register (SAFE\_MOD):

Bit name	access		describe	Reset value
[7:0] SAFE_MOD	WO	Description	WO is used to enter or terminate the safe	00h

mode. Some SFRs can only be written in the safe mode and are always read-only in the non-safe mode. Steps to enter the safe mode:

- (1) Write 55h to this register;
- (2) Then write AAh to the register;
- (3) After that, the system will be in safe mode for about 13 to 23 main frequency cycles. During this period, one or more security classes can be rewritten.

SFR or ordinary SFR;

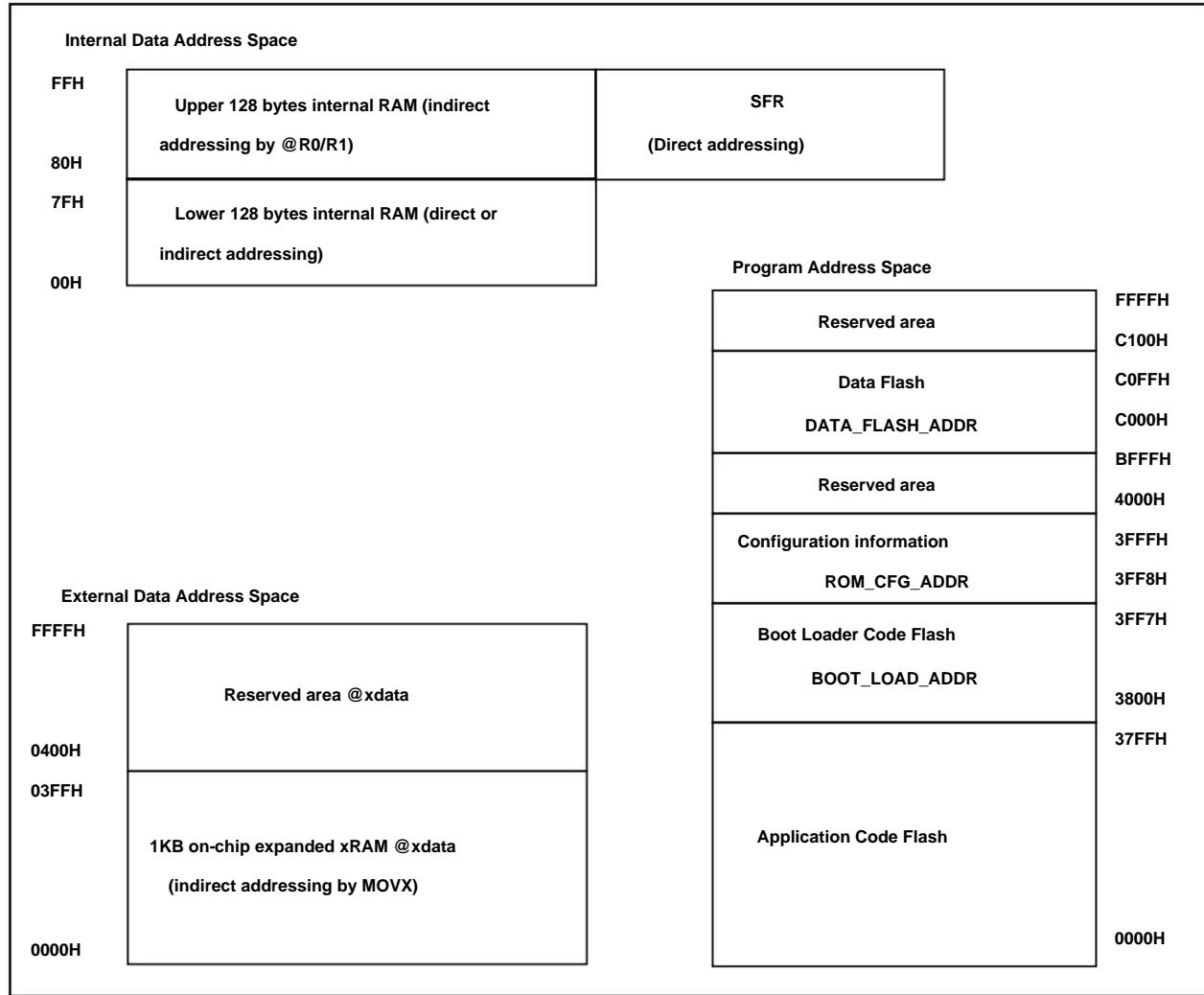
- (4) Automatically terminate the safety mode after the above validity period;
- (5) Alternatively, writing any value to this register can terminate the safe mode early.

## 6. Memory structure

### 6.1 Memory Space

The CH552 addressing space is divided into program storage space, internal data storage space, and external data storage space.

Figure 6.1 Memory structure diagram



### 6.2 Program Storage Space

The program storage space is 64KB in total, as shown in Figure 6.1, of which 16KB is used for ROM, including Code Flash to store instruction codes.

#### Area and Configuration Information area.

Code Flash includes application code in the low address area and boot code in the high address area.

Merging is used to preserve a single application code.

For CH551, the application code area of Code Flash is only 10KB.

The ROM is made of iFlash™ technology. After the blank ROM is formally packaged, it can be programmed approximately 200 times under a 5V power supply.

If you need to support program space programming under 3.3V power supply or more programming times, it is recommended to use CH548, CH547 or CH543 chips.

The Data Flash address range is C000h to C0FFH (only even addresses are valid, there is actually a storage unit every other byte).

Only supports single byte (8-bit) read and write operations, the data remains unchanged after the chip is powered off. Data Flash supports about 10,000 erase and write times, it is recommended

Balanced use, prohibit the same storage unit from being erased and written more than 10K times. If more erase and write times are required, it is recommended to use CH548, CH547, CH558

Or CH543 and other chips.

Configuration Information Configuration Information includes 4 groups of 16-bit data located at addresses 3FF8H to 3FFFH.

This is a read-only unit that provides the chip ID. The configuration data at address 3FF8H is set by the programmer as needed. See Table 6.2.

Table 6.2 Flash-ROM configuration information description

Bit Address	Bit Name		Recommended value
15	Code_Protect	Describes the code and data protection modes in flash-ROM: 0-Prohibit programmer from reading, program confidential; 1-Allow reading	0/1
14	No_Boot_Load	Enable BootLoader boot code startup mode: 0-Start the application from address 0000h; 1-Start from the bootloader at address 3800h	1
13	En_Long_Reset	Enable additional delayed reset during power-on reset: 0-standard short reset; 1-wide reset, additional 44mS reset time	0
12	En_RST_RESET Enable	RST pin as manual reset input pin: 0-disable; 1-enable RST	0
[11:10]	Reserved (automatically set to 00 by the programmer as needed)		00
9	Must_1 (automatically set to 1 by the programmer as needed)		1
8	Must_0 (automatically set to 0 by the programmer as needed)		0
[7:0]	All_1 (automatically set to FFh by the programmer as needed)		FFh

### 6.3 Data Storage Space

The internal data storage space is 256 bytes in total, as shown in Figure 6.1. All of it is used for SFR and iRAM, of which iRAM is used for stack And fast data temporary storage, which can be subdivided into working registers R0-R7, bit variables bdata, byte variables data, idata, etc.

The external data storage space is 64KB in total, as shown in Figure 6.1. Part of it is used for 1KB on-chip expansion xRAM, and the rest is reserved area.

For CH551, the on-chip extended xRAM is only 512 bytes.

### 6.4 Flash-ROM Registers

Table 6.4 Flash-ROM operation register list

name	address	describe	Reset value
ROM_DATA_H	8Fh	Flash-ROM data register high byte Flash-	xxh
ROM_DATA_L	8Eh	ROM data register low byte	xxh
ROM_DATA	8Eh	ROM_DATA_L and ROM_DATA_H form a 16-bit SFR flash-ROM	xxxxh
ROM_STATUS	86h	status register (read only) flash-ROM control	00h
ROM_CTRL	86h	register (write only) flash-ROM address	00h
ROM_ADDR_H	85h	register high byte flash-ROM address	xxh
ROM_ADDR_L	84h	register low byte	xxh
ROM_ADDR	84h	ROM_ADDR_L and ROM_ADDR_H form a 16-bit SFR	xxxxh

Flash-ROM address register (ROM\_ADDR):

Bit	Name access		describe	Reset value
[7:0]	ROM_ADDR_H	RW	flash-ROM address high byte	xxh
[7:0]	ROM_ADDR_L	RW	The flash-ROM address low byte only supports even addresses. For Data Flash, the actual offset address 00H-7FH must be shifted left 1 bit becomes an even address 00H/02H/04H...yFEH and then puts	xxh

Flash-ROM data register (ROM\_DATA):

Bits [7:0]	Name access		describe	Reset value
Bits [7:0]	ROM_DATA_H	RW	flash-ROM high byte of data to be written	xxh
[7:0]	ROM_DATA_L	RW	Flash-ROM low byte of data to be written, For DataFlash, it is the data byte to be written or the data byte to be read.	xxh

Flash-ROM control register (ROM\_CTRL):

Bit	Name access		describe	Reset value
[7:0]	ROM_CTRL	WO	flash-ROM control register	00h

Flash-ROM status register (ROM\_STATUS):

Bit	Name access reservation		describe	Reset value
7		RO Reserved		0
6	bROM_ADDR_OK	RO	Flash-ROM write operation address valid status bit: If this bit is 0, it means the parameter is invalid; if it is 1, it means the address is valid.	0
[5:2]	reserve	RO Reserved		0000b
1	bROM_CMD_ERR	RO	Flash-ROM operation command error status bit: If this bit is 0, it means the command is valid; if it is 1, it means it is an unknown command.	0
0	reserve	RO Reserved		0

## 6.5 Flash-ROM Operation Steps

### 1. Write the flash-ROM code area and write double-byte data to the target address:

- (1) If you need to write flash-ROM code, you must select a 5V power supply voltage;
- (2) Enable safe mode, SAFE\_MOD = 55h; SAFE\_MOD = 0AAh;
- (3) Set the global configuration register GLOBAL\_CFG to enable write (bCODE\_WE or bDATA\_WE corresponds to code or data);
- (4) Set the address register ROM\_ADDR and write the 16-bit target address (the lowest bit is always 0);
- (5) Set the data register ROM\_DATA and write the 16-bit data to be written. The order of steps (4) and (5) can be reversed.
- (6) Set the operation control register ROM\_CTRL to 09Ah and perform a write operation. The program will automatically pause during the operation.
- (7) After the operation is completed, the program resumes running. At this time, query the status register ROM\_STATUS to view the status of this operation; if To write multiple data, loop through steps (4), (5), (6), and (7);
- (8) Enter safe mode again, SAFE\_MOD = 55h; SAFE\_MOD = 0AAh;
- (9) Set the global configuration register GLOBAL\_CFG to enable write protection (bCODE\_WE=0, bDATA\_WE=0).

### 2. Write the Data Flash data area and write single-byte data to the target address:

- (1) Enable safe mode, SAFE\_MOD = 55h; SAFE\_MOD = 0AAh;
- (2) Set the global configuration register GLOBAL\_CFG to enable write (bDATA\_WE corresponds to data);
- (3) Set the address register ROM\_ADDR and write the 16-bit target address. The actual offset address 00H-7FH must be shifted left by 1 bit to become Even addresses 00H/02H/04H..yFEH are then placed, and the final addresses are C000H/C002H/C004...;
- (4) Set the data register ROM\_DATA\_L and write 8 bits of data to be written. The order of steps (3) and (4) can be reversed.
- (5) Set the operation control register ROM\_CTRL to 09Ah and perform a write operation. The program will automatically pause during the operation.
- (6) After the operation is completed, the program resumes running. At this time, query the status register ROM\_STATUS to view the status of this operation; if To write multiple data, loop through steps (3), (4), (5), and (6);
- (7) Enter safe mode again, SAFE\_MOD = 55h; SAFE\_MOD = 0AAh;
- (8) Set the global configuration register GLOBAL\_CFG to enable write protection (bCODE\_WE=0, bDATA\_WE=0).

### 3. Read the Data Flash data area and read single-byte data from the target address:

- (1) Set the address register ROM\_ADDR and write the 16-bit target address. The actual offset address 00H-7FH must be shifted left by 1 bit to become Even address, the final address is C000H/C002H/C004...;
- (2) Set the operation control register ROM\_CTRL to 08Eh and perform a read operation. The program will automatically pause during the operation.
- (3) After the operation is completed, the program resumes running. At this time, query the bROM\_CMD\_ERR in the status register ROM\_STATUS to view this

Second operation status; if the command is valid, the read 8-bit data will be saved in the data register ROM\_DATA\_L;  
 (4) If you want to read multiple data, loop through steps (1), (2), and (3).

#### 4. Read flash-ROM:

Use the MOVC instruction directly or through a pointer to the program memory space to read the code or data at the target address.

### 6.6 On-board Programming and ISP Download

When the configuration information Code\_Protect=1, the code in the CH552 chip flash-ROM and the data in the Data Flash can be

Read and write by an external programmer through the synchronous serial interface; when the configuration information Code\_Protect=0, the code in the flash-ROM and the data in the Data Flash are protected and cannot be read, but can be erased. After erasing, powering on again will release the code protection.

When the CH552 chip is pre-installed with the BootLoader, it can support multiple ISPs such as USB or asynchronous serial port.

Download the application; however, in the absence of a bootloader, CH552 can only be written to the bootloader by an external dedicated programmer.

Or application. In order to support on-board programming, a 5V power supply voltage must be used temporarily, and the CH552 and programming voltage must be reserved in the circuit.

There are 4 connecting pins between the devices, and the minimum necessary connecting pins are 3: P1.4, P1.6, and P1.7.

Table 6.6.1 Connection pins with the programmer

Pin GPIO RST	Reset	Pin Description
RST	control pin in programming state, high level allows entering programming state	
SCS	P1.4 Chip select input pin in programming state (necessary), high level by default, low level is valid	
SCK	P1.7 Clock input pin in programming state (required)	
MISO	P1.6 Data output pin in programming state (required)	

Note: Whether programming on the board or downloading the program through the serial port or USB, you must temporarily use a 5V power supply voltage.

For programming or downloading under 3.3V power supply voltage, it is recommended to use CH548, CH547 or CH543 chips.

### 6.7 Chip Unique ID Number

Each microcontroller has a unique ID number when it leaves the factory, which is the chip identification number. The ID data is 5 bytes in total and is stored in the configuration

The address 3FFAH to 3FFFH in the Configuration Information area. 3FFBH is a reserved location, and 3FFCH

The 16-bit data of the two addresses 3FFEHE and 3FFAH and the 8-bit data of the address are combined into 40-bit chip ID data.

Table 6.7.1 Chip ID Address Table

Program space address	ID Data Description
3FFAh, 3FFBh	last word data, which is the highest byte of the 40-bit ID number, the reserved byte
3FFCh, 3FFDh	ID first word data, followed by the lowest byte, second lowest byte of the ID number
3FFEh, 3FFFh	ID sub-word data, which are the second high byte, high byte of the ID number respectively.

The ID data can be obtained by reading the Code Flash. The ID number can be used with the download tool to download the target program.

For general applications, only the first 32 bits of the ID number need to be used, and the 8 bits of data at address 3FFAH can be ignored.

## 7. Power management, sleep and reset

### 7.1 External power input

The CH552 chip has a built-in 5V to 3.3V low-dropout voltage regulator and supports external 5V or 3.3V power supply input.

Refer to the table below for power supply input modes.

External power supply voltage	VCC pin voltage: external voltage 3V~5V	V33 pin voltage: internal voltage 3.3V
3.3V or 3V including less than 3.6V	Input external 3.3V voltage to the voltage regulator, A decoupling capacitor of no less than 0.1uF must be connected to the ground	Input external 3.3V as internal working power supply, A decoupling capacitor of no less than 0.1uF must be connected to the ground
5V	Input external 5V voltage to the voltage regulator,	Internal voltage regulator 3.3V output

Including more than 3.6V must be connected to the ground with a decoupling capacitor of no less than 0.1uF and 3.3V internal working power input,	A decoupling capacitor of no less than 0.1uF must be connected to the ground
---	--

After power on or system reset, CH552 is in running state by default.

The system main frequency can reduce the power consumption during operation. When CH552 does not need to run at all, you can set the PD in PCON to enter the sleep state.

In sleep state, you can choose to wake up externally through USB, UART0, UART1, SPI0 and some GPIOs.

## 7.2 Power and Sleep Control Registers

Table 7.2.1 Power and sleep control register list

name	address	describe	Reset value
WDOG_COUNT	FFh Watchdog count register		00h
RESET_KEEP	FEh Reset Holding Register		00h
WAKE_CTRL	A9h Sleep Wake-up Control Register 87h Power		00h
PCON	Control Register		10h

Watchdog count register (WDOG\_COUNT):

Bit	Name access			Reset value
[7:0] WDOG_COUNT	RW	Describes the current count of the watchdog. When the count reaches OFFh, it will turn to 00h. Automatically set the interrupt flag bWDOG_IF_TO to 1		00h

Reset hold register (RESET\_KEEP):

Bit	Name access			Reset value
[7:0] RESET_KEEP	RW	Describes the reset holding register, the value can be modified manually, except for the power-on reset Except clearing it to zero, any other reset will not affect the value		00h

Sleep wake-up control register (WAKE\_CTRL), writable only in safe mode:

Bit	name	Access	Description	Reset value
7	bWAK_BY_USB	0 to disable	wake-up, UART1 receive input low level wake-up enable. This bit is	0
6	bWAK_RXD1_LO	RW	bit is 0 to disable wake-up. Select RXD1 or RXD1_ pin according to bUART1_PIN_X=0/1	0
5	bWAK_P1_5_LO	RW	P1.5 Low level wake-up enable, 0 disable wake-up RW P1.4 Low level	0
4	bWAK_P1_4_LO	RW	wake-up enable, 0 disable wake-up RW P1.3 Low level wake-up enable,	0
3	bWAK_P1_3_LO	RW	0 disable wake-up RW RST High level wake-up enable, 0 disable wake-	0
2	bWAK_RST_HI	RW	P3.2 Edge change and P3.3 Low level wake-up enable, 0 disable	0
1	bWAK_P3_2E_3L	RW	wake-up 0	0
0	bWAK_RXD0_LO	RW	UART0 receive input low level wake-up enable, 0 disables wake-up. Select RXD0 or RXD0_ pin according to bUART0_PIN_X=0/1	0

Power Control Register (PCON):

Bit	name	access	describe	Reset value
7	SMOD	RW	When using Timer 1 to generate the UART0 baud rate, select UART0 Mode 1, 2, 3 communication baud rate: 0-slow mode; 1-fast mode	0
6	reserve	RO	Reserved	0
5	bRST_FLAG1	RO	The last reset flag of the chip is high	0

4	bRST_FLAG0	R0 The last reset flag of the chip is low	1
3	GF1	RW General flag bit 1: User-defined, software cleared or set to 0	
2	GF0	RW General flag bit 0: User-defined, software cleared or set to 0	
1	PD	RW Sleep mode enable, set to 1 and then sleep, hardware automatically cleared after waking up	0
0	reserve	RO Reserved	0

Table 7.2.2 Description of the chip's most recent reset flag

bRST_FLAG1	bRST_FLAG0	Reset Flag Description
0	0	Software reset, source: bSW_RESET=1 and (bBOOT_LOAD=0 or bWDOG_EN=1) Power-on reset, source: VCC pin
0	1	voltage is lower than the detection level
1	0	Watchdog reset, source: bWDOG_EN=1 and watchdog timeout
1	1	External pin manual reset, source: En_RST_RESET=1 and RST input high level

## 7.3 Reset Control

CH552 has 4 reset sources: power-on reset, external reset, software reset, and watchdog reset. The last three are thermal resets.

### 7.3.1 Power-On Reset

The power-on reset (POR) is generated by the on-chip voltage detection circuit. The POR circuit continuously monitors the power supply voltage of the VCC pin. If the voltage is lower than the detection voltage, the

When Vpot is equal, a power-on reset is generated, and the hardware automatically delays Tpor to maintain the reset state. After the delay, CH552 runs.

Only power-on reset can make CH552 reload configuration information and clear RESET\_KEEP, and other warm resets have no effect.

### 7.3.2 External reset

External reset is generated by applying a high level to the RST pin.

When the high level duration is greater than Trst, the reset process is triggered. When the external high level signal is removed, the hardware automatically delays Trdl to maintain Reset state, after the delay ends, CH552 starts to execute from address 0.

### 7.3.3 Software Reset

CH552 supports internal software reset so that it can actively reset the CPU state and restart without external intervention.

When bSW\_RESET in the configuration register GLOBAL\_CFG is 1, the software can be reset and Trdl will be automatically delayed to maintain the reset state.

After the delay, CH552 starts executing from address 0, and the bSW\_RESET bit is automatically cleared by hardware.

When bSW\_RESET is set to 1, if bBOOT\_LOAD=0 or bWDOG\_EN=1, then bRST\_FLAG1/0 will indicate

Software reset; when bSW\_RESET is set to 1, if bBOOT\_LOAD = 1 and bWDOG\_EN = 0, then bRST\_FLAG1/0 will not be

Generate a new reset flag, but keep the previous reset flag unchanged.

For chips with ISP boot program, after power on reset, the boot program will be run first. This program will reset the chip as needed.

The chip switches to the application state. This software reset only causes bBOOT\_LOAD to be cleared and does not affect the state of bRST\_FLAG1/0 (by

Before reset, bBOOT\_LOAD=1), so when switching to application state, bRST\_FLAG1/0 still indicates the power-on reset state.

### 7.3.4 Watchdog reset

The watchdog reset is generated when the watchdog timer overflows. The watchdog timer is an 8-bit counter with a clock frequency of

The system frequency is Fsys/65536. When the counter reaches 0FFh and rolls over to 00h, an overflow signal is generated.

The watchdog timer overflow signal will trigger the interrupt flag bWDOG\_IF\_TO to 1. The interrupt flag will reload WDOG\_COUNT

It is automatically cleared when the corresponding interrupt service routine is entered.

By writing different count initial values to WDOG\_COUNT, different timing cycles Twdc can be achieved. At 6MHz main frequency,

The watchdog timer period Twdc is approximately 2.8 seconds when 00h is written, and approximately 1.4 seconds when 80h is written. It is halved at a 12MHz main frequency.

If bWDOG\_EN=1 when the watchdog timer overflows, a watchdog reset is generated and Trdl is automatically delayed to maintain the reset.

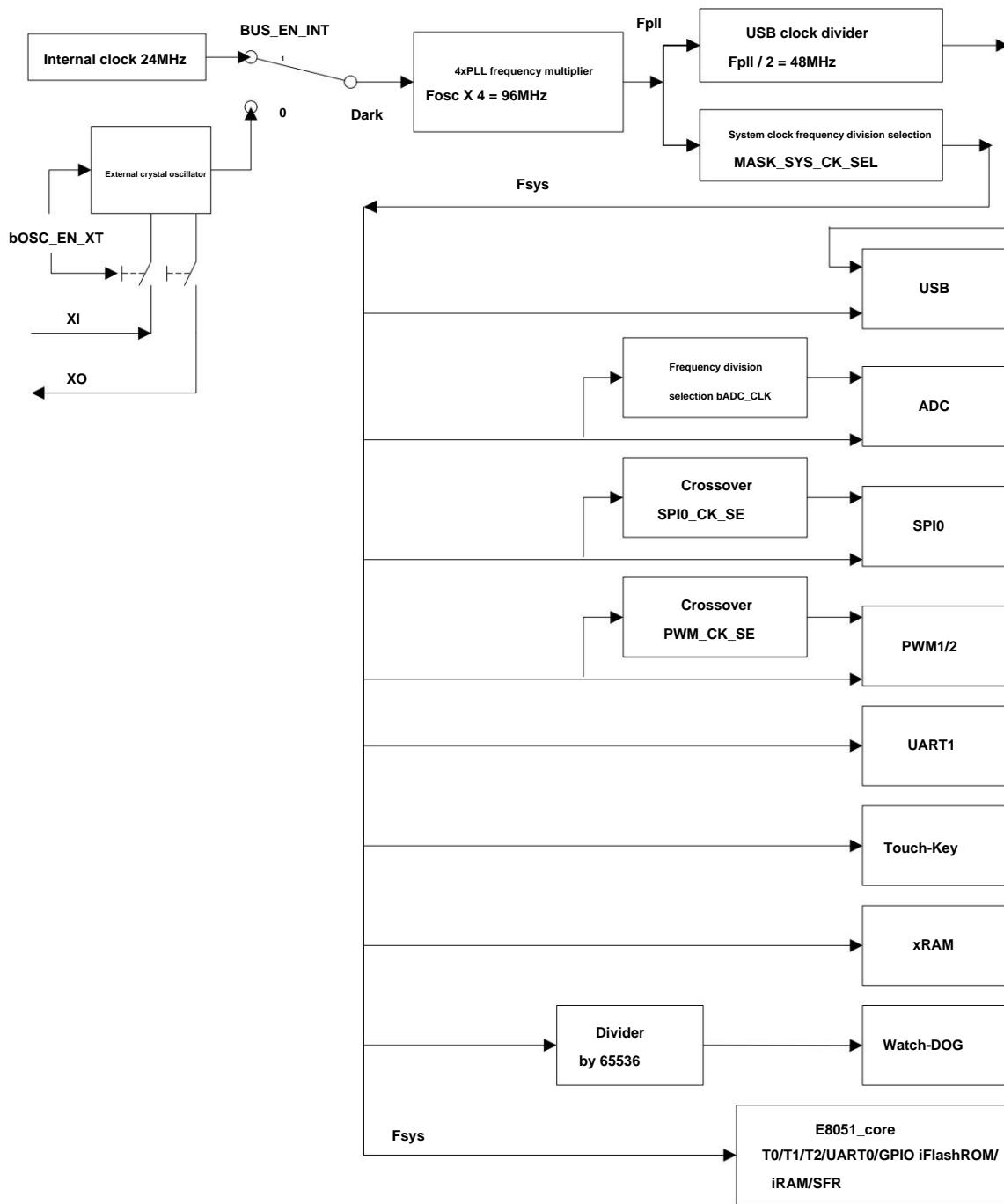
After the delay, CH552 starts to execute from address 0.

To avoid being reset by the watchdog timer when bWDOG\_EN=1, WDOG\_COUNT must be reset in time to prevent it from overflowing.

## 8. System clock

### 8.1 Clock Block Diagram

Figure 8.1.1 Clock system and structure diagram



The internal clock or external clock is selected as the original clock Fosc, which is then multiplied by 4xPLL to generate the Fpll high-frequency clock.

Finally, two sets of frequency dividers are used to generate the system clock Fsys and the USB module clock Fusb4x. The system clock Fsys is directly provided to each module of CH552.

## 8.2 Register Description

Table 8.2.1 Clock Control Register List

name	address	describe	Reset value
CLOCK_CFG	B9h	System Clock Configuration Register	83h

System clock configuration register (CLOCK\_CFG), writable only in safe mode:

Bit	name	access		Reset value
7	FOSC_EN_INT	RW	Describes the internal clock oscillator enable. This bit is 1 to enable the internal clock oscillator. And select the internal clock; this bit is 0 to turn off the internal clock oscillator and And select external crystal oscillator to provide clock	
6	bOSC_EN_XT	RW	External crystal oscillator is enabled. If this bit is 1, the P1.2/P1.3 pins will be used as To enable XI/XO and oscillator, connect an external quartz crystal between XI and XO. 0 Crystal or ceramic oscillator; this bit is 0 to turn off the external oscillator	0
5	bWDOG_IF_TO	RO	Watchdog timer interrupt flag, this bit is 1, indicating an interrupt. Timer overflow signal triggers; this bit is 0 means no interrupt. Reload the watchdog count register WDOG_COUNT or enter Automatically clear the flash-ROM after the	0
4	bROM_CLK_FAST	RW	corresponding interrupt service routine Reference clock frequency selection: 0- Normal (If Fosc>=16MHz); 1-speed up (if Fosc<16MHz)	0
3	bRST	RO RST	pin status input bit [2:0]	0
MASK_SYS_CK_SEL RW System clock frequency selection, refer to Table 8.2.2 below				011b

Table 8.2.2 System main frequency selection table

MASK_SYS_CK_SEL	Relationship between system main frequency Fsys and crystal frequency Fxt	Fxt When Fosc=24MHz Fsys
000	Fpll / 512	Fxt / 128
001	Fpll / 128	Fxt / 32
010	Fpll / 32	Fxt / 8
011	Fpll / 16	Fxt / 4
100	Fpll / 8	Fxt / 2
101	Fpll / 6	Fxt / 1.5 Only when VCC is higher than 3.8V
110	Fpll / 4	16MHz 24MHz Only when VCC is above 4.5V
111	Fpll / 3	Reserved, disabled

## 8.3 Clock Configuration

After the CH552 chip is powered on, it uses the internal clock by default, and the internal clock frequency is 24MHz. You can select the internal clock by CLOCK\_CFG.

If the external crystal oscillator is turned off, the XI and XO pins can be used as P1.2 and P1.3.

Ordinary I/O port use. If an external crystal oscillator is used to provide the clock, the crystal should be connected between the XI and XO pins.

And connect the oscillation capacitor to GND for XI and XO pins respectively; if the clock signal is directly input from the outside, it should be connected from XI pin Input, XO pin is left floating.

Original clock frequency Fosc = bOSC\_EN\_INT ? 24MHz: Fxt PLL frequency

Fpll = Fosc \* 4 = 96MHz USB clock frequency Fusb4x

= Fpll / 2 = 48MHz

System main frequency Fsys is obtained by dividing Fpll according to Table 8.2.2

In the default state after reset, Fosc=24MHz, Fpll=96MHz, Fusb4x=48MHz, and Fsys=6MHz.

The steps to switch to an external crystal oscillator to provide the clock are as follows:

- (1) Enter safe mode, step 1 SAFE\_MOD = 55h; step 2 SAFE\_MOD = AAh;
- (2) Use the "bitwise OR" operation to set bOSC\_EN\_XT in CLOCK\_CFG to 1, and keep other bits unchanged to enable the crystal oscillator;
- (3) Delay for several milliseconds, usually 5mS to 10mS, to wait for the crystal oscillator to stabilize;
- (4) Enter safe mode again, step 1 SAFE\_MOD = 55h; step 2 SAFE\_MOD = AAh;
- (5) Use the "bit AND" operation to clear bOSC\_EN\_INT in CLOCK\_CFG to 0, leaving other bits unchanged, and switch to the external clock;
- (6) Turn off the safe mode and write any value to SAFE\_MOD to terminate the safe mode early.

The steps to modify the system main frequency are as follows:

- (1) Enter safe mode, step 1 SAFE\_MOD = 55h; step 2 SAFE\_MOD = AAh;
- (2) Write a new value to CLOCK\_CFG;
- (3) Turn off the safe mode and write any value to SAFE\_MOD to terminate the safe mode early.

Remark:

- (1) If using a USB module, the Fusb4x must be 48MHz; and when using full-speed USB, the system frequency Fsys must not be lower than 6MHz; when using low-speed USB, the system main frequency Fsys shall not be lower than 1.5MHz.
- (2) Give priority to using a lower system clock frequency Fsys, thereby reducing the system dynamic power consumption and widening the operating temperature range.
- (3) The internal clock oscillator is powered by the V33 power supply, so changes in the V33 voltage, especially low voltage, will affect the internal clock frequency.

## 9. Interruption

The CH552 chip supports 14 groups of interrupt signal sources, including 6 groups of interrupts compatible with the standard MCS51: INT0, T0, INT1, T1, UART0, T2, and extended 8 groups of interrupts: SPI0, TKEY, USB, ADC, UART1, PWMX, GPIO, WDOG, among which GPIO Interrupts can be selected from 7 I/O pins.

### 9.1 Register Description

Table 9.1.1 Interrupt vector table

Interrupt Source Entry Address	Interrupt Number	Description	External Interrupt 0	External Interrupt 1	Timer 0	Default priority order
INT_NO_INT0	0x0003	Interrupt				High priority
INT_NO_TMR0	0x000B					
INT_NO_INT1	0x0013	2 External interrupt	1	3	Timer	
INT_NO_TMR1	0x001B	1 interrupt				
INT_NO_UART0	0x0023	4	UART0	interrupt		
INT_NO_TMR2	0x002B	5 Timer	2	interrupt		
INT_NO_SPI0	0x0033	6	SPI0	interrupt		
INT_NO_TKEY	0x003B	7 Touch	key	timer	interrupt	
INT_NO_USB	0x0043	8	USB	interrupt		
INT_NO_ADC	0x004B	9	ADC	interrupt		
INT_NO_UART1	0x0053	10	UART1	interrupt		
INT_NO_PWMX	0x005B	11	PWM1/PWM2	interrupt		
INT_NO_GPIO	0x0063	12	GPIO	interrupts		

INT_NO_WDOG	0x006B	13 Watchdog timer interrupt	Low priority
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Table 9.1.2 Interrupt related register list

name	address	describe	Reset value
IP_EX	E9h Extended	Interrupt Priority Control Register	00h
IE_EX	E8h Extended	Interrupt Enable Register	00h
GPIO_IE	C7h	GPIO interrupt enable register	00h
IP	B8h Interrupt	Priority Control Register	00h
IE	A8h Interrupt	Enable Register	00h

Interrupt enable register (IE):

Bit name access				Reset value
7 YES	RW	Describes the global interrupt enable control bit. If this bit is 1 and E_DIS is 0, interrupts are enabled. The global interrupt disable control bit	0	
6 E_DIS	RW	is 0 to mask all interrupt requests, and the bit is 1 to mask all interrupt requests; the bit is 0 and EA is 1, the interrupt is enabled. This bit is usually used to temporarily Disable interrupts	0	
5 ET2	RW Timer 2 interrupt enable bit, this bit is 1 to allow T2 interrupt; 0 to mask	0		
4 IS	RW Asynchronous serial port 0 interrupt enable bit, this bit is 1 to allow UART0 interrupt; 0 to mask 0	0		
3 ET1	RW Timer 1 interrupt enable bit, this bit is 1 to allow T1 interrupt; 0 to mask	0		
2 EX1	RW External interrupt 1 enable bit, this bit is 1 to allow INT1 interrupt; 0 to mask	0		
1 ET0	RW Timer 0 interrupt enable bit, this bit is 1 to allow T0 interrupt; 0 to mask	0		
0 EX0	RW External interrupt 0 enable bit, this bit is 1 to allow INT0 interrupt; 0 to mask	0		

Extended interrupt enable register (IE\_EX):

Bit name access			describe	Reset value
7 IE_WDOG	RW Watchdog timer interrupt enable bit, this bit is 1 to enable WDOG interrupt; 0 to mask 0			
6 IE_GPIO	RW GPIO interrupt enable bit, this bit is 1 to allow the interrupt enabled in GPIO_IE; 0 to screen Mask all interrupts in GPIO_IE		0	
5 IE_PWMX	RW PWM1/PWM2 interrupt enable bit, this bit is 1 to enable PWM1/2 interrupt; 0 to mask 0			
4 IE_UART1	RW Asynchronous serial port 1 interrupt enable bit, this bit is 1 to allow UART1 interrupt; 0 to mask 0			
3 IE_ADC	RW ADC analog-to-digital conversion interrupt enable bit, this bit is 1 to allow ADC interrupt; 0 to mask 0			
2 IE_USB	RW USB interrupt enable bit, this bit is 1 to enable USB interrupt; 0 to mask		0	
1 IE_TKEY	RW Touch key timer interrupt enable bit, this bit is 1 to allow timer interrupt; 0 to mask 0			
0 IE_SPI0	RW SPI0 interrupt enable bit, this bit is 1 to enable SPI0 interrupt; 0 to mask		0	

GPIO interrupt enable register (GPIO\_IE):

Bit name access			describe	Reset value
7 bIE_IO_EDGE	RW	GPIO edge interrupt mode enable: This bit is 0 to select the level interrupt mode, the GPIO pin input valid level bIO_INT_ACT is 1 and has been requesting an interrupt, GPIO input invalid level bIO_INT_ACT is 0 and the interrupt request is canceled; This bit is 1 to select edge interrupt mode, and a valid edge is generated when the GPIO pin inputs	0	

			The interrupt flag bIO_INT_ACT is set to request an interrupt. This interrupt flag cannot be cleared by software.  Zero, can only be reset or in level interrupt mode or enter the corresponding interrupt service  It is automatically cleared when programming	
6	bIE_RXD1_LO	RW	This bit is 1 to enable UART1 receive pin interrupt (level mode low level is valid, Edge mode (falling edge is valid); this bit is 0 to disable.  bUART1_PIN_X=0/1 select RXD1 or RXD1_ pin	0
5	bIE_P1_5_LO	RW	This bit is 1 to enable P1.5 interrupt (low level is valid in level mode and low level is valid in edge mode).  This bit is 0 to disable this bit and 1 to	0
4	bIE_P1_4_LO	RW	enable P1.4 interrupt (low level is valid in level mode and falling edge is valid in edge mode).  This bit is 0 to disable this bit and 1 to	0
3	bIE_P1_3_LO	RW	enable P1.3 interrupt (low level is valid in level mode and falling edge is valid in edge mode).  This bit is 0 to disable and 1 to enable RST	0
2	bIE_RST_HI	RW	interrupt (high level is valid in level mode and falling edge is valid in edge mode).  This bit is 0 to disable this bit and 1 to	0
1	bIE_P3_1_LO	RW	enable P3.1 interrupt (low level is valid in level mode and rising edge is valid in edge mode).  This bit is 0 to disable and 1 to enable	0
0	bIE_RXD0_LO	RW	UART0 receive pin interrupt (level mode low level is valid, Edge mode (falling edge is valid); this bit is 0 to disable.  bUART0_PIN_X=0/1 select RXD0 or RXD0_ pin	0

Interrupt priority control register (IP):

Bit name access			describe	Reset value
7	PH_FLAG	RO High	priority interrupt is executing flag	0
6	PL_FLAG	RO Low	priority interrupt is executing flag	0
5	PT2	RW	Timer 2 interrupt priority control bit	0
4	PS	RW	UART0 interrupt priority control bit	0
3	PT1	RW	Timer 1 interrupt priority control bit	0
2	PX1	RW	External interrupt 1 interrupt priority control bit	0
1	PT0	RW	Timer 0 interrupt priority control bit	0
0	PX0	RW	External interrupt 0 interrupt priority control bit	0

Extended interrupt priority control register (IP\_EX):

Bit name access				Reset value
7	bIP_LEVEL	RO	Describes the current interrupt nesting level flag. If the bit is 0, it means no interrupt or nesting Level 2 interrupt; if this bit is 1, it means the current level 1 interrupt is nested.	0
6	bIP_GPIO	RW	GPIO interrupt priority control bit	0
5	bIP_PWMX	RW	PWM1/PWM2 interrupt priority control bit	0
4	bIP_UART1	RW	UART1 interrupt priority control bit	0
3	bIP_ADC	RW	ADC interrupt priority control bit	0
2	bIP_USB	RW	USB interrupt priority control bit	0
1	bIP_TKEY	RW	Touch key timer interrupt priority control bit	0
0	bIP_SPI0	RW	SPI0 interrupt priority control bit	0

The IP and IP\_EX registers are used to set the interrupt priority. If a bit is set to 1, the corresponding interrupt source is set to high priority.

If a bit is cleared to 0, the corresponding interrupt source is set to low priority. For interrupt sources of the same level, the system has a default priority order.

The default priority order is shown in Table 9.1.1, where the combination of PH\_FLAG and PL\_FLAG indicates the priority of the current interrupt.

Table 9.1.3 Current interrupt priority status indication

PH_FLAG	PL_FLAG	Current interrupt priority status
0	0	No interruption currently
0	1	A low priority interrupt is currently being executed
1	0	A high priority interrupt is currently being executed.
1	1	Unexpected state, unknown error

## 10. I/O ports

### 10.1 Introduction to GPIO

CH552 provides up to 17 I/O pins, some of which have multiplexing functions. Among them, the input and output of ports P1 and P3 are

Port P2 is an internal port and is only used to select the xRAM page when performing MOVX access with R0 or R1.

If the pin is not configured as an alternate function, it defaults to the general I/O pin state.

All I/O ports have true "read-modify-write" functionality, supporting bit manipulation instructions such as SETB or CLR to independently change certain

The direction of the pin or the port level, etc.

### 10.2 GPIO Registers

All registers and bits in this section are represented in a common format: lowercase "n" represents the port number (n=1 or 3), and lowercase "x" represents the

Represents the ordinal number of the bit (x=0, 1, 2, 3, 4, 5, 6, 7).

Table 10.2.1 GPIO register list

name	address	describe	Reset value
P1	90h	P1 port input and output registers	FFh
P1_MOD_OC	92h	P1 port output mode register	FFh
P1_DIR_PU	93h	P1 port direction control and pull-up enable register	FFh
P2	A0h	P2 port output register	FFh
P3	B0h	P3 port input and output registers	FFh
P3_MOD_OC	96h	P3 port output mode register	FFh
P3_DIR_PU	97h	P3 port direction control and pull-up enable register	FFh
PIN_FUNC	C6h	Pin Function Select Register	80 hours
XBUS_AUX	A2h	Bus Auxiliary Setup Register	00h

Pn port input and output register (Pn):

	Name access		describe	Reset value
Bits [7:0]	Pn.0~Pn.7	RW	Pn.x pin status input and data output bit, can be addressed bit by bit FFh	

Pn port output mode register (Pn\_MOD\_OC):

	Name access		describe	Reset value
Bits [7:0]	Pn_MOD_OC	RW	Pn.x pin output mode setting: 0-push-pull output; 1-open drain output FFh	

Pn port direction control and pull-up enable register (Pn\_DIR\_PU):

Bit	Name access		describe	Reset value

[7:0]	Pn_DIR_PU	RW is the direction control of Pn.x pin in push-pull output mode: 0-input; 1-output;  In open-drain output mode, the pull-up resistor on the Pn.x pin is enabled: 0-disable pull-up resistor; 1-enable pull-up resistor	FFh
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The relevant configuration of the Pn port is implemented by combining Pn\_MOD\_OC[x] and Pn\_DIR\_PU[x], as shown below.

Table 10.2.2 Port Configuration Register Combination

Pn_MOD_OC	Pn_DIR_PU	Working mode description
0	0	High-impedance input mode, the pin has no pull-up resistor
0	1	Push-pull output mode, with symmetrical driving capability, can output or absorb large current
1	0	Open drain output, supports high impedance input, pin has no pull-up resistor
1	1	Quasi-bidirectional mode (standard 8051), open drain output, support input, pin has pull-up resistor, when When the output switches from low to high, it automatically drives the high level for 2 clock cycles to speed up the conversion.

P1 and P3 ports support pure input or push-pull output and quasi-bidirectional modes. Each pin has an internal pull-up that can be freely controlled.

resistors, and protection diodes connected to VCC and GND.

Figure 10.2.1 is the equivalent schematic diagram of the P1.x pins of the P1 port. After removing AIN, it can be applied to the P3 port.

After changing to V33, it applies to P3.6 and P3.7, that is, the pull-up or input or output high level of P3.6 and P3.7 can only reach V33 voltage.

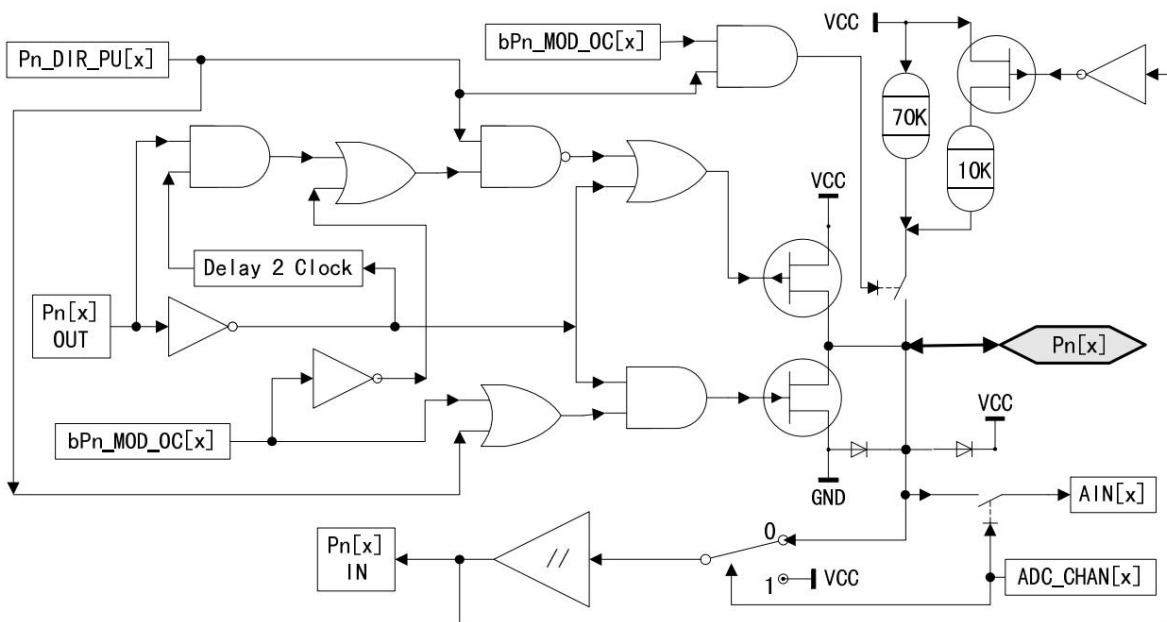
P3.6 and P3.7 can select standard pull-up resistor (to V33), 15K $\Omega$  pull-down resistor, or provide 1.5K $\Omega$  strong pull-up resistor for one of the pins.

Pull-up resistor (to V33). Standard pull-up resistor is only valid when bUSB\_IO\_EN=0, that is, in GPIO mode, and is controlled by bits 7 and 6 of P3\_DIR\_PU.

Control; Pull-down resistor is controlled by bUD\_PD\_DIS when bUC\_RESET\_SIE=0, and has nothing to do with bUSB\_IO\_EN; 1.5K $\Omega$  strong pull-up resistor

The pull-down resistor takes precedence over the pull-up resistor and is controlled by bUC\_DEV\_PU\_EN when bUC\_RESET\_SIE=0, and has nothing to do with bUSB\_IO\_EN.

Figure 10.2.1 I/O pin equivalent schematic diagram



#### 10.4 GPIO Multiplexing and Mapping

Some I/O pins of CH552 have multiplexing functions. After power on, they are all general I/O pins by default. After different functional modules are enabled, the corresponding

The pins are configured as the functional pins corresponding to their respective functional modules.

Pin function selection register (PIN\_FUNC):

Bit name access				Reset value
7 bUSB_IO_EN	RW	Describes the USB UDP/UDM pin enable bit. If this bit is 0, P3.6/P3.7 is used for GPIO. Support P3_DIR_PU to control the pull-up resistor and support P3_MOD_OC; this bit is 1 Then P3.6/P3.7 is used for UDP/UDM and controlled by USB module, P3_DIR_PU and P3_MOD_OC have no effect on it		1
6 bIO_INT_ACT	R0	GPIO interrupt request activation status: When bIE_IO_EDGE=0, this bit is 1, indicating that the GPIO input is valid. The request will be interrupted, and 0 means the input is invalid level; When bIE_IO_EDGE=1, this bit is used as edge interrupt flag. 1 indicates detection. When a valid edge is detected, this bit cannot be cleared by software and can only be cleared when reset or the level is mid-level. It is automatically cleared in interrupt mode or when entering the corresponding interrupt service routine		0
5 bUART1_PIN_X	RW	UART1 pin mapping enable bit, if this bit is 0, RXD1/TXD1 will be used P1.6/P1.7; if this bit is 1, RXD1/TXD1 uses P3.4/P3.2 UART0 pin mapping		0
4 bUART0_PIN_X	RW	enable bit, if this bit is 0, RXD0/TXD0 uses P3.0/P3.1; if this bit is 1, RXD0/TXD0 uses P1.2/P1.3 PWM2 pin mapping		0
3 bPWM2_PIN_X	RW	enable bit, if this bit is 0, PWM2 uses P3.4; this bit is 1, PWM2 uses P3.1 PWM1		0
2 bPWM1_PIN_X	RW	pin mapping enable bit, this bit is 0, PWM1 uses P1.5; this bit is 1, PWM1 uses P3.0 T2EX/		0
1 bT2EX_PIN_X	RW	CAP2 pin mapping enable bit, if this bit is 0, T2EX/CAP2 uses P1.1; if this bit is 1, T2EX/CAP2 uses the RST T2/CAP1		0
0 bT2_PIN_X	RW	pin mapping enable bit, and if this bit is 0, T2/CAP1 uses P1.0; If this bit is 1, T2/CAP1 uses P1.4		0

Table 10.4.1 GPIO pin multiplexing function list

GPIO	Other functions: in order of priority from left to right
RST	RST/bT2EX_/_bCAP2_/_bRST
P1[0]	T2/bT2_/_bCAP1/bCAP1_/_TIN0_/_P1.0
P1[1]	T2EX/bT2EX_/_bCAP2/bCAP2_/_TIN1_/_VBUS2_/_AIN0_/_P1.1
P1[2]	XI_/_RXD_/_bRXD_/_P1.2 XO_/_TXD_/_
P1[3]	bTXD_/_P1.3 T2_/_bT2_/_bCAP1_/_
P1[4]	bCAP1_/_SCS/bSCS_/_TIN2_/_UCC1_/_AIN1_/_P1.4 MOSI/bMOSI_/_PWM1/bPWM1_/_TIN3_/_UCC2_/_AIN2_/_
P1[5]	P1.5
P1[6]	MISO/bMISO_/_RXD1/bRXD1_/_TIN4_/_P1.6
P1[7]	SCK/bSCK_/_TXD1/bTXD1_/_TIN5_/_P1.7
P3[0]	PWM1_/_bPWM1_/_RXD/bRXD_/_P3.0 PWM2_/_
P3[1]	bPWM2_/_TXD/bTXD_/_P3.1 TXD1_/_bTXD1_/_
P3[2]	INT0/bINT0_/_VBUS1_/_AIN3_/_P3.2
P3[3]	INT1/bINT1_/_P3.3
P3[4]	PWM2/bPWM2_/_RXD1_/_bRXD1_/_T0/bT0_/_P3.4
P3[5]	T1/bT1_/_P3.5
P3[6]	UDP/bUDP_/_P3.6
P3[7]	UDM/bUDM_/_P3.7

The priority order from left to right in the table above refers to the priority order when multiple functional modules compete for the use of the GPIO. For example,

When P3.1 is used for TXD serial port transmission, P3.0 can still be used for higher priority PWM1 output.

## 11. External bus

CH552 does not provide bus signals to the outside of the chip and does not support external buses, but can access the on-chip xRAM normally.

External bus auxiliary setting register (XBUS\_AUX):

Bit	name	access	describe	Reset value
7	bUART0_TX	RO	Indicates the sending status of UART0, 1 means it is in the process of sending	0
6	bUART0_RX	RO	Indicates the receiving status of UART0, 1 means it is in the receiving process	0
5	bSAFE_MOD_ACT	RO	Indicates the safe mode status, 1 means it is currently in safe mode	0
4	Reserved	RO Reserved		0
3	GF2	RW	General flag bit 2: User-defined, software cleared or set to 0	
2	bDPTR_AUTO_INC	RW	Enables DPTR to automatically increase by 1 after the MOVX_@DPTR instruction is completed	0
1	reserve	RO Reserved		0
0	DPS	RW	Dual DPTR data pointer selection bit: This bit is 0 to select DPTR0; this bit is 1 to select DPTR1	0

## 12. Timer

12.1 Timer0/1 Timer0/1 is

two 16-bit timers/counters. Timer0 and Timer1 are configured through TCON and TMOD. TCON is used to set the timer.

Timer/counter T0 and T1 start control and overflow interrupt and external interrupt control. Each timer is composed of two 8-bit registers

The high byte counter of timer 0 is TH0, and the low byte is TL0; the high byte counter of timer 1 is

TH1, the low byte is TL1. Timer 1 can also be used as the baud rate generator for UART0.

Table 12.1.1 Timer0/1 related register list

name	address	describe	Reset value
TH1	8Dh	Timer1 count high byte	xxh
TH0	8Ch	Timer0 count high byte	xxh
TL1	8Bh	Timer1 count low byte	xxh
TL0	8Ah	Timer0 count low byte	xxh
TMOD	89h	Timer0/1 Mode Register	00h
TCON	88h	Timer0/1 Control Register	00h

Timer/Event Counter 0/1 Control Register (TCON):

Bit name	access		describe	Reset value
7	TF1	RW	Timer1 overflow interrupt flag, automatically cleared after entering Timer 1 interrupt	0
6	TR1	RW	Timer1 start/stop bit, set to 1 to start, set or cleared by software	0
5	TF0	RW	Timer0 overflow interrupt flag, automatically cleared after entering Timer 0 interrupt	0
4	TR0	RW	Timer0 start/stop bit, set to 1 to start, set or cleared by software	0
3	IE1	RW	INT1 External interrupt 1 interrupt request flag, automatically cleared after entering the interrupt	0
2	IT1	RW	INT1 External interrupt 1 trigger mode control bit, this bit is 0 to select the external interrupt as low Level trigger; this bit is 1 to select the external interrupt as falling edge trigger	0
1	IE0	RW	INT0 External interrupt 0 interrupt request flag, automatically cleared after entering the interrupt	0

0	IT0	RW	INT0 External interrupt 0 trigger mode control bit, this bit is 0 to select the external interrupt as low Level trigger; this bit is 1 to select the external interrupt as falling edge trigger	0
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Timer/Event Counter 0/1 Mode Register (TMOD):

Bit name access				Reset value
7 bT1_GATE		RW	Describes the gate enable bit, which controls whether Timer1 start is affected by the external interrupt signal INT1. If this bit is 0, whether the timer/counter 1 is started has nothing to do with INT1; if this bit is 1 The INT1 pin is high and TR1 is 1 to start	0
6	bT1_CT	RW	Timing or counting mode selection bit, this bit is 0 working in timing mode; this bit is 1 Works in counting mode, using the falling edge of T1 pin as the clock	0
5	bT1_M1	RW	Timer/Event Counter 1 Mode Select High	0
4	bT1_M0	RW	Timer/Event Counter 1 Mode Select Low	0
3 bT0_GATE		RW	Gate enable bit, which controls whether Timer0 start is affected by external interrupt signal INT0. If this bit is 0, whether the timer/counter 0 is started has nothing to do with INT0; if this bit is 1 The INT0 pin is high and TR0 is 1 to start.	0
2	bT0_CT	RW	Timing or counting mode selection bit, this bit is 0 working in timing mode; this bit is 1 Works in counting mode, using the falling edge of T0 pin as the clock	0
1	bT0_M1	RW	Timer/Event Counter 0 Mode Select High	0
0	bT0_M0	RW	Timer/Event Counter 0 Mode Select Low Bit	0

Table 12.1.2 bTn\_M1 and bTn\_M0 select Timern working mode (n=0, 1)

bTn_M1 bTn_M0		Timer n working mode (n=0, 1) Mode 0:
0	0	13-bit timer/counter n, the counting unit consists of the lower 5 bits of TLn and THn, the upper 3 bits of TLn When the count changes from all 1 to all 0, the overflow flag TFn is set and the initial value needs to be reset.
0	1	Mode 1: 16-bit timer/counter n, counting unit consists of TLn and THn. Counting starts when all 16 bits are 1 When all are 0, the overflow flag TFn is set and the initial value needs to be reset.
1	0	Mode 2: 8-bit reload timer/counter n, the counting unit uses TLn and THn as the reload counting unit. When the count changes from 8 bits all 1 to all 0, the overflow flag TFn is set and the initial value is automatically loaded from THn
1	1	Mode 3: If it is Timer/Event Counter 0, then Timer/Event Counter 0 is divided into 2 parts TL0 and TH0. TL0 is used as an 8-bit timer/counter, occupying all the control bits of Timer0; while TH0 also serves as another 8-bit timer is used, occupying TR1, TF1 and interrupt resources of Timer1, and Timer1 is still Yes, except that the start control bit TR1 and overflow flag TF1 cannot be used. If it is Timer/Event Counter 1, then entering Mode 3 will stop Timer/Event Counter 1.

Timern count low byte (TLn) (n=0, 1):

Bit Name	Access [7:0]		describe	Reset value
	TLn	RW	Timern count low byte	xxh

Timern count high byte (THn) (n=0, 1):

Bit Name	Access [7:0]		describe	Reset value
	THn	RW	Timern count high byte	xxh

## 12.2 Timer2

Timer2 is a 16-bit auto-reload timer/counter configured via the T2CON and T2MOD registers.

The high byte counter is TH2 and the low byte is TL2. Timer2 can be used as the baud rate generator of UART0 and also has two signal level capture

The capture count is stored in the RCAP2 and T2CAP1 registers.

Table 12.2.1 Timer2 related register list

name	address	describe	Reset value
TH2	CDh	Timer2 counter high byte	00h
TL2	CCh	Timer2 counter low byte	00h
T2COUNT	CCh	TL2 and TH2 form a 16-bit SFR	0000h
T2CAP1H	CFh	Timer2 capture 1 data high byte (read only)	xxh
T2CAP1L	CEh	Timer2 capture 1 data low byte (read only)	xxh
T2CAP1	CEh	T2CAP1L and T2CAP1H form a 16-bit SFR	xxxxh
RCAP2H	CBh	Reload/Capture 2 Data Register High Byte	00h
RCAP2L	CAh	Count Reload/Capture 2 Data Register Low Byte	00h
RCAP2	CAh	RCAP2L and RCAP2H form a 16-bit SFR	0000h
T2MOD	C9h	Timer2 Mode Register	00h
T2CON	C8h	Timer2 Control Register	00h

Timer/Event Counter 2 Control Register (T2CON):

Bit name access				Reset value
7	TF2	RW	Description When bT2_CAP1_EN=0, it is the overflow interrupt flag of Timer2. When the count changes from 16 bits all 1 to all 0, the overflow flag is set to 1. To be cleared by software; when RCLK=1 or TCLK=1, this bit will not be set to 1. When	0
7	CAP1F	RW	bT2_CAP1_EN=1, it is the Timer2 capture 1 interrupt flag, which is valid by T2. Edge triggered, requires software clearing	0
6	EXF2	RW	The external trigger flag of Timer2 is triggered by the valid edge of T2EX when EXEN2=1. Set to 1, need to be cleared by software	0
5	RCLK	RW	UART0 receive clock selection, this bit is 0 to select Timer1 overflow pulse to generate wave Baud rate; this bit is 1 to select the baud rate of Timer2 overflow pulse generation	0
4	TCLK	RW	UART0 transmit clock selection, this bit is 0 to select Timer1 overflow pulse to generate wave Baud rate; this bit is 1 to select the baud rate of Timer2 overflow pulse generation	0
3	EXEN2	RW	T2EX trigger enable bit, this bit is 0 to ignore T2EX; this bit is 1 to enable T2EX Trigger reload or capture on valid edge	0
2	TR2	RW	Timer2 start/stop bit, set to 1 to start, set or cleared by software	0
1	C_T2	RW	Timer2 clock source selection bit, this bit is 0 to use the internal clock; this bit is 1 to use Using edge counting based on the falling edge of the T2 pin	0
0	CP_RL2	RW	Timer2 function selection bit. If RCLK or TCLK is 1, this bit should be set to If this bit is 0, Timer2 will be used as a timer/counter, and when the counter The initial value of the count can be automatically reloaded when overflow or T2EX level changes; this bit is 1 Enable the capture 2 function of Timer2 and capture the valid edge of T2EX	0

Timer/Event Counter 2 Mode Register (T2MOD):

Bit name access				Reset value
7	bTMR_CLK	RW	Describes the fastest clock mode enabled for T0/T1/T2 timers with fast clock selected. If the bit is 1, the system main frequency Fsys without frequency division is used as the counting clock; If it is 0, the divided clock is used. This bit has no effect on the timer that selects the standard clock.	0

6	bT2_CLK	RW	Timer2 internal clock frequency selection bit, this bit is 0 to select the standard clock, timer/counter The clock mode is Fsys/12, and the UART0 clock mode is Fsys/4; this bit is 1 to select fast The timer/counter mode is Fsys/4 (bTMR_CLK=0) or Fsys(bTMR_CLK=1), UART0 clock mode is Fsys/2(bTMR_CLK=0) or Fsys(bTMR_CLK=1)	0
5	bT1_CLK	RW	Timer1 internal clock frequency selection bit, this bit is 0 to select the standard clock Fsys/12; 1 selects fast clock Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1)	0
4	bT0_CLK	RW	Timer0 internal clock frequency selection bit, this bit is 0 to select the standard clock Fsys/12; 1 selects fast clock Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1)	0
3 bT2_CAP_M1		RW	Timer2 capture mode high bit  Capture mode selection: X0: from falling edge to falling edge	0
2 bT2_CAP_M0		RW	Timer2 capture mode low bit  01: From any edge to any edge, that is, the level changes 11: From rising edge to rising edge	0
1	T2OE	RW	Timer2 clock output enable bit, this bit is 0 to disable output; this bit is 1 to enable The T2 pin outputs a clock with a frequency half the Timer2 overflow rate.	0
0 bT2_CAP1_EN		RW	Capture 1 when RCLK=0, TCLK=0, CP_RL2=1, C_T2=0, T2OE=0 Mode enable, this bit is 1 to enable the capture 1 function to capture the T2 valid edge; 0 disables capture 1	0

Count reload/capture 2 data register (RCAP2):

Bit name	access			Reset value
[7:0]	RCAP2H	RW	Description In the timer/counter mode, it is the high byte of the reload value; in the capture mode, it is The high byte of the timer captured by CAP2	00h
[7:0]	RCAP2L	RW	is the low byte of the reload value in the timer/counter mode and the low byte in the capture mode. CAP2 captures the low byte of the timer	00h

Timer2 Counter (T2COUNT):

Bit name	access		describe	Reset value
[7:0]	TH2	RW	Current counter high byte	00h
[7:0]	TL2	RW	Current counter low byte	00h

Timer2 capture 1 data (T2CAP1):

Bit name	access		describe	Reset value
[7:0] T2CAP1H	RO		CAP1 captures the high byte of the timer	xxh
[7:0] T2CAP1L	RO		CAP1 captures the low byte of the timer	xxh

## 12.3 PWM Function

CH552 provides 2 8-bit PWM channels. The PWM output polarity can be set to low or high by default and can be modified dynamically.

The output duty cycle of PWM can be integrated and low-pass filtered by simple RC resistors and capacitors to obtain various output voltages, which is equivalent to low

High-speed digital-to-analog converter DAC.

PWM1 output duty cycle = PWM\_DATA1 / 256, supporting a range of 0% to 99.6%.

PWM2 output duty cycle = PWM\_DATA2 / 256, supporting a range of 0% to 99.6%.

In actual applications, it is recommended to enable PWM pin output and set the PWM output pin to push-pull output mode.

## 12.3.1 PWM1 and PWM2

Table 12.3.1 PWM1 and PWM2 related register list

name	address	describe	Reset value
PWM_CK_SE	9Eh	PWM clock frequency division setting register	00h
PWM_CTRL	9Dh	PWM Control Register	02h
PWM_DATA1	9Ch	PWM1 data register	xxh
PWM_DATA2	9Bh	PWM2 Data Register	xxh

## PWM2 data register (PWM\_DATA2):

Bit	Name access		describe	Reset value
[7:0]	PWM_DATA2	RW	Store PWM2 current data, PWM2 output active level duty cycle = PWM_DATA2/256	xxh

## PWM1 data register (PWM\_DATA1):

Bit	Name access		describe	Reset value
[7:0]	PWM_DATA1	RW	Store PWM1 current data, PWM1 output active level duty cycle = PWM_DATA1/256	xxh

## PWM Control Register (PWM\_CTRL):

Bit	Name access		describe	Reset value
7	bPWM_IE_END	RW	This bit is 1 to enable the PWM cycle end or MFM buffer empty interrupt	0
6	bPWM2_POLAR	RW	Control PWM2 output polarity. If this bit is 0, it is low level by default. If it is high, it is If this bit is 1, the default is high level, and low level is valid	0
5	bPWM1_POLAR	RW	Control PWM1 output polarity. If this bit is 0, it is low level by default. If it is high level, it is If this bit is 1, the default is high level, and low level is valid	0
4	bPWM_IF_END	RW	PWM cycle end interrupt flag, this bit is 1 means there is an interrupt, write 1 Cleared or reloaded when PWM_DATA1 data is cleared	0
3	bPWM2_OUT_EN	RW	PWM2 output enable, this bit is 1 to enable PWM2 output	0
2	bPWM1_OUT_EN	RW	PWM1 output enable, this bit is 1 to enable PWM1 output	0
1	bPWM_CLR_ALL	RW	This bit is 1 to clear the PWM1 and PWM2 counts and FIFO, and needs to be cleared by software 1	
0	Reserved	RO	Reserved	0

## PWM clock frequency division setting register (PWM\_CK\_SE):

	Name access		describe	Reset value
Bits [7:0]	PWM_CK_SE	RW Set	PWM clock frequency divisor	00h

## 12.4 Timer Function

## 12.4.1 Timer0/1

(1) Set T2MOD to select the Timer internal clock frequency. If bTn\_CLK (n=0/1) is 0, then the clock frequency corresponding to Timer0/1 is

If bTn\_CLK is 1, then bTMR\_CLK=0 or 1 selects Fsys/4 or Fsys as the clock.

(2) Set TMOD to configure the working mode of the Timer.

Mode 0: 13-bit timer/counter

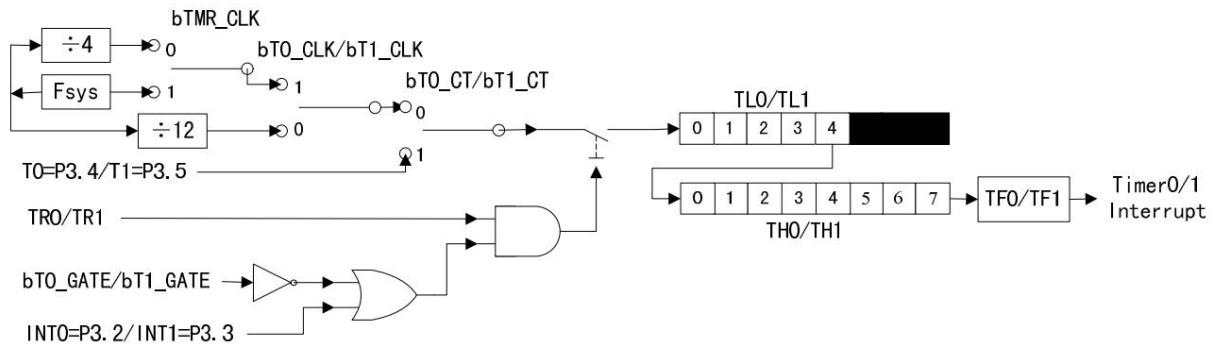


Figure 12.4.1.1 Timer0/1 Mode 0

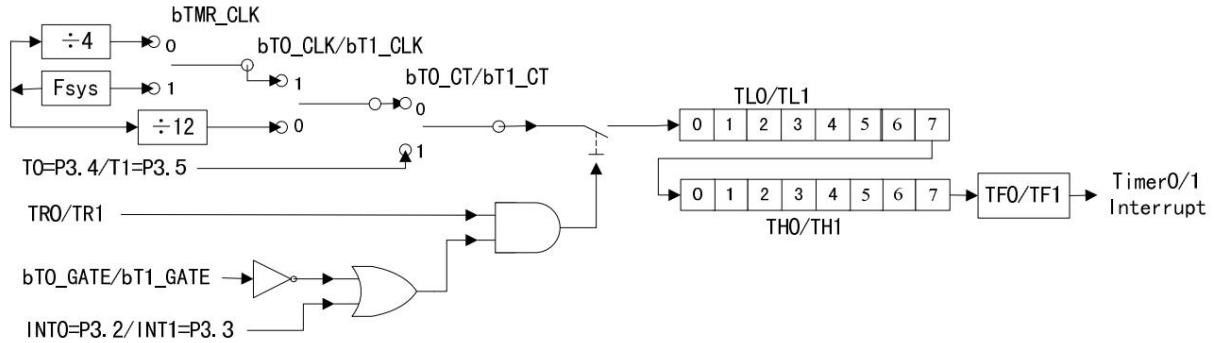
**Mode 1: 16-bit timer/counter**

Figure 12.4.1.2 Timer0/1 Mode 1

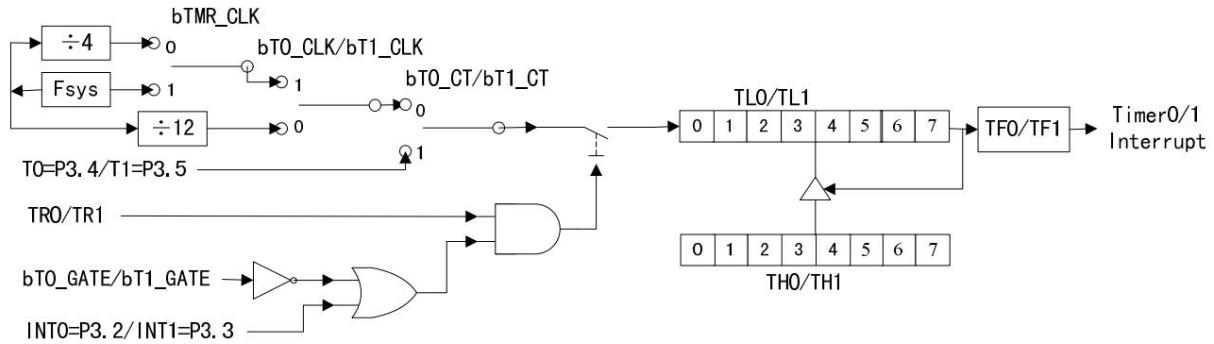
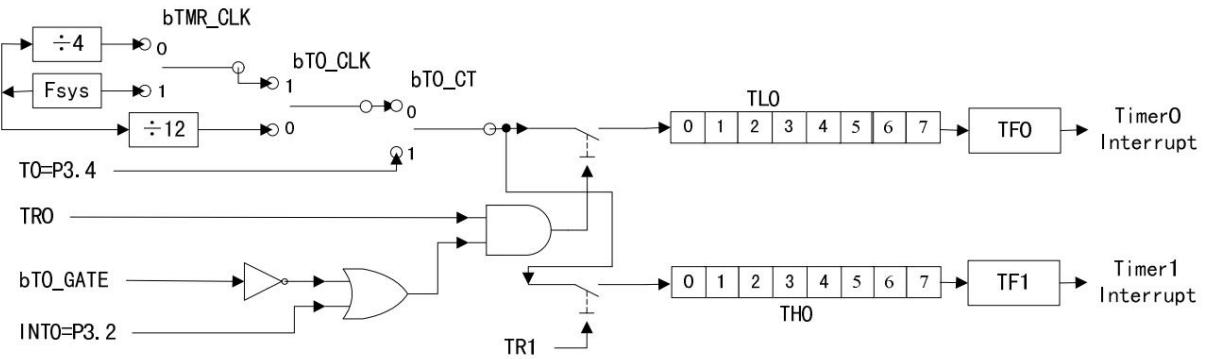
**Mode 2: Auto-reload 8-bit timer/counter**

Figure 12.4.1.3 Timer0/1 Mode 2

**Mode 3: Timer0 is decomposed into two independent 8-bit timer/counters and uses the TR1 control bit of Timer1; Timer1 is passed**

**By starting Mode 3 instead of borrowing TR1 control bit, Timer 1 enters Mode 3 and Timer 1 stops running.**



**Figure 12.4.1.4 Timer0 Mode 3**

- (3) Set the initial value of the timer/counter TL<sub>n</sub> and TH<sub>n</sub> (n=0/1).

Set the bit TRn (n=0/1) in TCON to start

## 12.4.2 Timer2

#### Timer2 16-bit reload timer/counter mode: (1) Set

**the bits RCLK and TCLK in T2CON to 0 to select the non-serial port baud rate generator mode. (2) Set**

the bit C T2 in T2CON to 0 to select the internal clock and go to step (3); you can also set it to 1 to select the falling edge of the T2 pin.

**As a counting clock, skip step (3).**

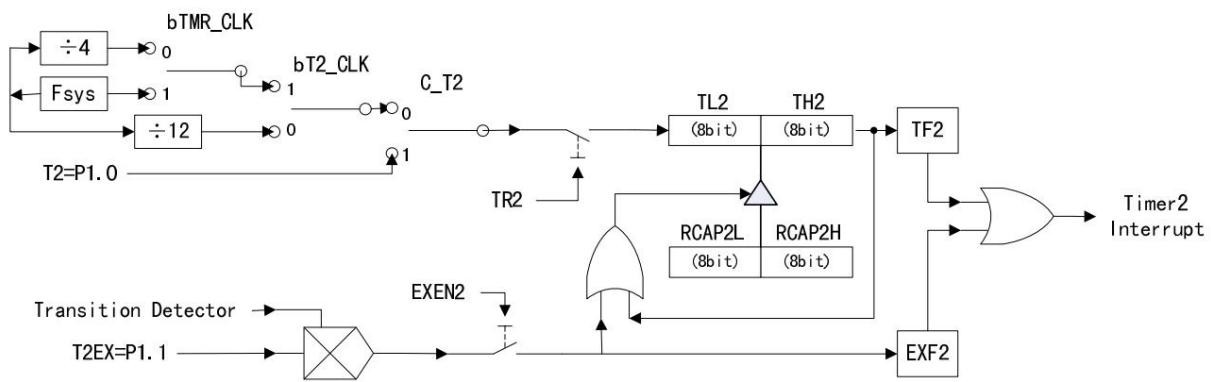
- (3) Set T2MOD to select the Timer internal clock frequency. If bT2\_CLK is 0, the Timer2 clock is Fsys/12; if bT2\_CLK is 1,

**bTMR\_CLK=0 or 1 selects Fsys/4 or Fsys as the clock.**

- (4) Set the bit CP\_RL2 of T2CON to 0, and select the 16-bit reload timer/counter function of Timer2. (5) Set

RCAP2L and RCAP2H as the reload value after the timer overflows, and set TL2 and TH2 as the initial value of the timer (usually the same as RCAP2L and RCAP2H are the same), set TR2 to 1, and start Timer2.

- (6) The current timer/counter status can be obtained by querying TF2 or Timer 2 interrupt.



**Figure 12.4.2.1 Timer2 16-bit reloadable timer/counter**

#### **Timer2 clock output mode:**

Refer to the 16-bit reload timer/counter mode and set the bit T2OE in T2MOD to 1 to enable the output from the T2 pin.

**TF2 frequency divided by 2 clock.**

## Timer2 serial port 0 baud rate generator

mode: (1) Set the bit C<sub>2</sub> in T2CON to 0 to select the internal clock, or set it to 1 to select the falling edge of the T2 pin as the clock.

Set the bits RCLK and TCLK in T2CON to 1 or one of them to 1 as needed to select the serial port baud rate generator mode.

(2) Set T2MOD to select the Timer internal clock frequency. If bT2\_CLK is 0, the Timer2 clock is Fsys/4. If bT2\_CLK is 1, Fsys/2 or Fsys is selected as the clock by bTMR\_CLK = 0 or 1. (3) Set RCAP2L and RCAP2H to the reload value after the timer overflows, set TR2 to 1, and start Timer2.

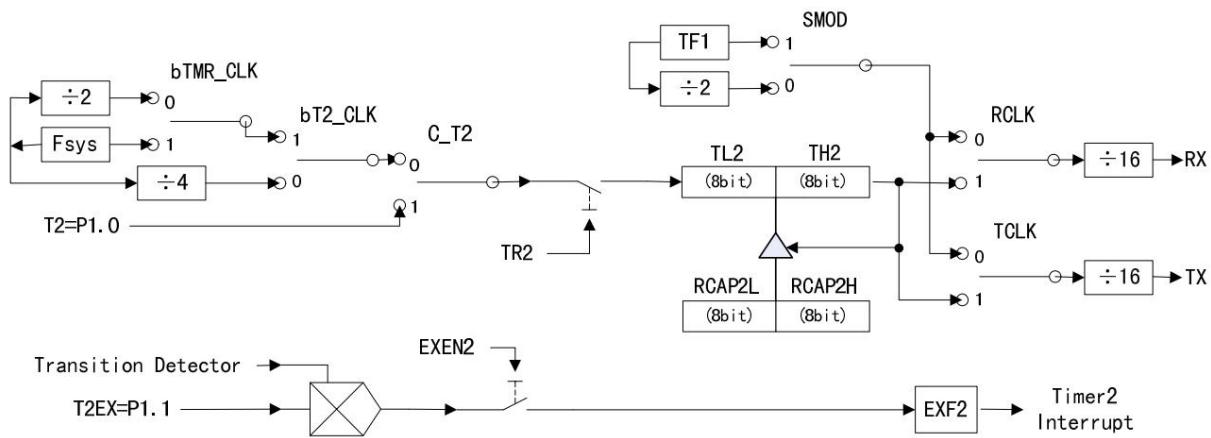


Figure 12.4.2.2 Timer2 UART0 Baud Rate Generator

#### Timer2 dual channel capture

mode: (1) Set the bits RCLK and TCLK in T2CON to 0 to select the non-serial port baud rate generator

mode. (2) Set the bit C\_T2 in T2CON to 0 to select the internal clock and go to step (3); you can also set it to 1 to select the falling edge of the T2 pin.

The edge is used as the counting clock and step (3) is skipped.

(3) Set T2MOD to select the Timer internal clock frequency. If bT2\_CLK is 0, the Timer2 clock is Fsys/12; if bT2\_CLK is 1, bTMR\_CLK=0 or 1 selects Fsys/4 or Fsys as the clock.

(4) Set bits bT2\_CAP\_M1 and bT2\_CAP\_M0 of T2MOD to select the corresponding edge capture mode.

(5) Set bit CP\_RL2 of T2CON to 1 to select Timer2's capture function on the T2EX pin. (6) Set TL2

and TH2 to the initial values of the timer, set TR2 to 1, and start Timer2. (7) When CAP2

capture is completed, RCAP2L and RCAP2H will save the count values of TL2 and TH2 at that time, and set EXF2 to generate an interrupt. The difference between the next captured RCAP2L and RCAP2H and the previous captured RCAP2L and RCAP2H is the signal width between the two valid edges.

(8) If the bit C\_T2 in T2CON is 0 and the bit bT2\_CAP1\_EN in T2MOD is 1, then the capture function of Timer2 on the T2 pin will be enabled at the same time. When CAP1 capture is completed, T2CAP1L and T2CAP1H will save the count values of TL2 and TH2 at that time, and set CAP1F to generate an interrupt.

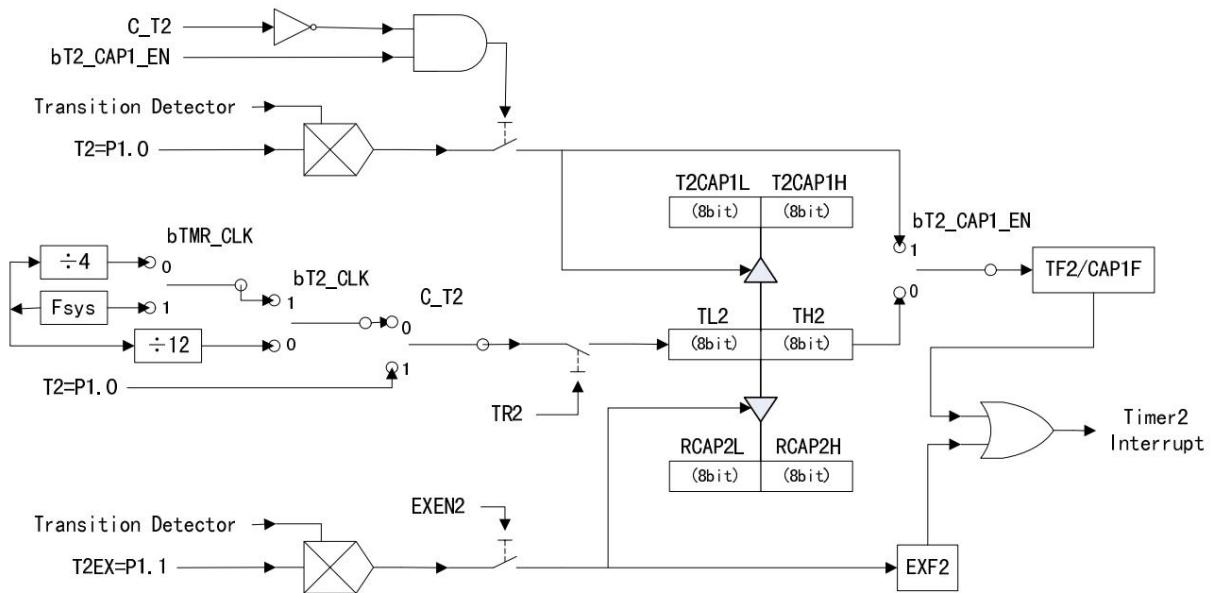


Figure 12.4.2.3 Timer2 Capture Mode

### 13. Universal Asynchronous Receiver/Transmitter (UART)

#### 13.1 UART Introduction

The CH552 chip provides two full-duplex asynchronous serial ports: UART0 and UART1. The CH551 only provides UART0.

UART0 is a standard MCS51 serial port. Data reception and transmission are achieved by accessing physically separate receive/transmit registers via SBUF.

The data written into SBUF is loaded into the transmit register, and the read operation of SBUF corresponds to the receive buffer register.

UART1 is a simplified MCS51 serial port. Data reception and transmission are achieved by accessing physically separate receive/transmit registers via SBUF1.

The data written into SBUF1 is loaded into the transmit register, and the read operation of SBUF1 corresponds to the receive buffer register.

UART0 has removed the multi-machine communication mode and fixed baud rate, and UART1 has an independent baud rate generator.

#### 13.2 UART Registers

Table 13.2.1 UART related register list

name	address	describe	Reset value
SCON	98h	UART0 Control Register	00h
SBUF	99h	UART0 Data Register	xxh
SCON1	C0h	UART1 Control Register	40h
SBUF1	C1h	UART1 data register	xxh
SBAUD1	C2h	UART1 baud rate setting register	xxh

##### 13.2.1 UART0 Register Description

UART0 Control Register (SCON):

Bit name access		describe	Reset value
7	SM0	RW UART0 working mode selection bit 0, this bit is 0 to select 8-bit data asynchronous communication; this bit is 1 Select 9-bit data asynchronous communication	0
6	SM1	RW UART0 working mode selection bit 1, this bit is 0 to set the fixed baud rate; this bit is 1 to set Variable baud rate, generated by timer T1 or T2	0
5	SM2	RW UART0 multi-machine communication control bit:  When receiving data in Mode 2 and 3, when SM2=1, if RB8 is 0, then RI is not If RB8 is set to 1, reception is invalid; if RB8 is 1, then RI is set to 1, reception is valid; when SM2=0 When , no matter RB8 is 0 or 1, RI is set when receiving data, and reception is valid; In mode 1, if SM2=1, the receiver will only receive the valid stop bit. efficient; In Mode 0, the SM2 bit must be set to 0	0
4	REN	RW UART0 allows receiving control bit, this bit is 0 to prohibit receiving; this bit is 1 to allow receiving	0
3	TB8	RW The 9th bit of the transmitted data. In modes 2 and 3, TB8 is used to write the 9th bit of the transmitted data. bit, which can be a parity bit; in multi-machine communication, it is used to indicate whether the host sends an address. Address byte or data byte, TB8=0 is data, TB8=1 is address	0
2	RB8	RW The 9th bit of the received data. In modes 2 and 3, RB8 is used to store the 9th bit of the received data. bit; in mode 1, if SM2=0, then RB8 is used to store the received stop bit; In mode 0, the RB8 transmit interrupt flag	0
1	OF	RW is not used. It is set by hardware after a data byte is sent and needs to be cleared by software. zero	0

0	RI	RW	Receive interrupt flag, set by hardware after a data byte is received, requires software Clear	0
---	----	----	---	---

Table 13.2.1.1 UART0 operating mode selection

SMD0 SM1		describe
0	0 Mode	0, shift register mode, baud rate is fixed at Fsys/12 1 Mode 1, 8-bit asynchronous
0	communication mode, baud rate is variable, generated by timer T1 or T2	
1	0 Mode	2, 9-bit asynchronous communication mode, baud rate is Fsys/128 (SMOD=0) or Fsys/32 (SMOD=1) 1 Mode 3, 9-bit asynchronous
1	communication mode, baud rate is variable, generated by timer T1 or T2	

In modes 1 and 3, when RCLK=0 and TCLK=0, the UART0 baud rate is generated by timer T1. T1 should be set to

Mode 2: Auto-reload 8-bit timer mode. bT1\_CT and bT1\_GATE must both be 0. It is divided into the following clock conditions.

Table 13.2.1.2 Calculation formula for UART0 baud rate generated by T1

bTMR_CLK	bT1_CLK	SMOD	describe
1	1	0	TH1 = 256 - Fsys / 32 / baud rate
1	1	1	TH1 = 256 - Fsys / 16 / baud rate
0	1	0	TH1 = 256 - Fsys / 4 / 32 / baud rate
0	1	1	TH1 = 256 - Fsys / 4 / 16 / baud rate
X	0	0	TH1 = 256 - Fsys / 12 / 32 / baud rate
X	0	1	TH1 = 256 - Fsys / 12 / 16 / baud rate

In modes 1 and 3, when RCLK=1 or TCLK=1, the UART0 baud rate is generated by timer T2. T2 should be set to

In 16-bit automatic re-carrying baud rate generator mode, C\_T2 and CP\_RL2 must both be 0, which is divided into the following clock conditions.

Table 13.2.1.3 Calculation formula for UART0 baud rate generated by T2

bTMR_CLK	bT2_CLK	describe
1	1	RCAP2 = 65536 - Fsys / 16 / baud rate
0	1	RCAP2 = 65536 - Fsys / 2 / 16 / baud rate
X	0	RCAP2 = 65536 - Fsys / 4 / 16 / baud rate

#### UART0 data register (SBUF):

Bit name	access		Reset value
[7:0]	SBUF	RW	Describes the UART0 data register, including two physically separate registers for sending and receiving. Writing data to SBUF corresponds to sending data register; reading data from SBUF corresponds to sending data register xxh Corresponding receive data register

#### 13.2.2 UART1 Register Description

##### UART1 Control Register (SCON1):

Bit name	access		describe	Reset value
7 U1SM0	RW		UART1 working mode selection bit, this bit is 0 to select 8-bit data asynchronous communication; this bit is 1 Select 9-bit data asynchronous communication	0
6 Reserved RO Reserved				1
5 U1SMOD RW			Select the communication baud rate of UART1: 0-slow mode; 1-fast mode	0
4 U1REN	RW		UART1 allows receiving control bit, this bit is 0 to prohibit receiving; this bit is 1 to allow receiving	0
3 U1TB8	RW		The 9th bit of the transmitted data. In 9-bit data mode, TB8 is used to write the 9th bit of the transmitted data. 9 bits, can be parity bit; in 8-bit data mode, TB8 is ignored	0

2 U1RB8	RW	The 9th bit of the received data. In 9-bit data mode, RB8 is used to store the 9th bit of the received data. 9 bits; in 8-bit data mode, RB8 is used to store the received stop bit	0
1	U1TI	RW	Send interrupt flag, set by hardware after a data byte is sent, needs to be cleared by software zero
0	U1RI	RW	Receive interrupt flag, set by hardware after a data byte is received, requires software Clear

The baud rate of UART1 is generated by SBAUD1 setting, and is divided into two cases according to the selection of U1SMOD:

When U1SMOD=0, SBAUD1 = 256 - Fsys / 32 / baud rate;

When U1SMOD=1, SBAUD1 = 256 - Fsys / 16 / baud rate.

#### UART1 data register (SBUF1):

Bit name	access		Reset value
[7:0]	SBUF1	RW	Describes the UART1 data register, including the send and receive registers, which are physically separated. Writing data to SBUF1 corresponds to sending data register; reading data from SBUF1 corresponds to sending data register xxh According to the corresponding receive data register

### 13.3 UART Application

#### UART0 Application:

- (1) Select the baud rate generator of UART0, which can be from timer T1 or T2, and configure the corresponding counter.
- (2) Start timer T1 or T2.
- (3) Set SM0, SM1, and SM2 of SCON to select the working mode of serial port 0. Set REN to 1 to enable UART0 reception.
- (4) You can set serial port interrupt or query RI and TI interrupt status.
- (5) Read and write SBUF to realize serial port data transmission and reception. The allowable baud rate error of the serial port receiving signal is no more than 2%.

#### UART1 Application:

- (1) Select U1SMOD and set SBAUD1 according to the baud rate.
- (2) Set U1SM0 of SCON1 to select the working mode of serial port 1. Set U1REN to 1 to enable UART1 reception.
- (3) You can set the serial port 1 interrupt or query the interrupt status of U1RI and U1TI.
- (4) Read and write SBUF1 to realize serial port 1 data transmission and reception. The allowable baud rate error of the serial port receiving signal is no more than 2%.

## 14. Synchronous Serial Interface SPI

### 14.1 Introduction to SPI

The CH552 chip provides an SPI interface for high-speed synchronous data transmission with peripherals.

- (1) Support master mode and slave mode;
- (2) Support mode 0 and mode 3 clock modes;
- (3) Optional 3-wire full-duplex or 2-wire half-duplex mode;
- (4) Optional MSB high bit is sent first or LSB low bit is sent first;
- (5) The clock frequency is adjustable, up to nearly half of the system main frequency;
- (6) Built-in 1-byte receive FIFO and 1-byte transmit FIFO;
- (7) In slave mode, it supports preloading data in the first byte, so that the host can immediately obtain the return data in the first byte.

### 14.2 SPI Registers

Table 14.2.1 SPI related register list

name	address	describe	Reset value
SPI0_SETUP	FCh SPI0	Setup Register	00h
SPI0_S_PRE	FBh SPI0	slave mode preset data register	20h
SPI0_CK_SE	FBh SPI0	clock division setting register	20h
SPI0_CTRL	FAh SPI0	Control Register	02h
SPI0_DATA	F9h SPI0	data transmit and receive register	xxh
SPI0_STAT	F8h SPI0	Status Register	08h

SPI0 Setup Register (SPI0\_SETUP):

Bit	name	access	describe	Reset value
7	bS0_MODE_SLV	RW	SPI0 master-slave mode selection bit, if this bit is 0, SPI0 is in master mode; If the bit is 1, SPI0 is in slave mode/device mode	0
6 bS0_IE_FIFO_OV		RW	FIFO overflow interrupt enable bit in slave mode, this bit is 1 to enable FIFO Overflow interrupt; if this bit is 0, FIFO overflow does not generate an	0
5 bS0_IE_FIRST		RW	interrupt. In slave mode, the first byte received is completed interrupt enable bit. If this bit is 1, the slave In this mode, an interrupt is triggered when the first data byte is received; if this bit is 0, an interrupt is triggered when the first data byte is received. 0 No interrupt is generated when the first byte is received	0
4 bS0_IE_BYTE		RW	Data byte transfer completion interrupt enable bit, this bit is 1 to allow byte transfer completion If this bit is 0, the byte transfer is completed without interruption. The order	0
3 bS0_BIT_ORDER		RW	control bit of the data byte. If this bit is 0, the MSB high bit is in front. If it is 1, the LSB is in the first place.	0
2 reserve		RO Reserved		0
1 bS0_SLV_SEL		RO	Chip select activation status bit in slave mode. A value of 0 indicates that the chip is not currently selected. In the selected state, the bit is 1, indicating that the preloaded data status	0
0 bS0_SLV_PRELOAD		RO	bit in slave mode is in the selected state. The bit is 1, indicating that the preloaded data status bit in slave mode is in the selected state. Preload status after selecting valid and before data is transmitted	0

SPI0 clock division setting register (SPI0\_CK\_SE):

Bit	Name access		describe	Reset value
[7:0] SPI0_CK_SE		RW Set	SPI0 clock division coefficient in master mode	20h

SPI0 slave mode preset data register (SPI0\_S\_PRE):

Bit	Name access		describe	Reset value
[7:0] SPI0_S_PRE		RW Pre	load the first transmission data in slave mode	20h

SPI0 Control Register (SPI0\_CTRL):

Bit	name	access	describe	Reset value
7 bS0_MISO_OE		RW	SPI0 MISO output enable control bit, this bit is 1 to allow output; 0 disables output	0
6 bS0_MOSI_OE		RW	MOSI output enable control bit of SPI0, this bit is 1 to allow output; 0 disables output	0
5 bS0_SCK_OE		RW	SPI0 SCK output enable control bit, this bit is 1 to allow output; 0 disables output	0

4	bS0_DATA_DIR	RW	SPI0 data direction control bit, if this bit is 0, the data will be output and only the FIFO will be written. As a valid operation, start an SPI transfer; if this bit is 1, input data, Writing or reading FIFO is considered a valid operation and starts an SPI transfer	0
3	bS0_MST_CLK	RW	SPI0 master clock mode control bit, if this bit is 0, mode 0, SCK idle The default is low level; if this bit is 1, mode 3, SCK defaults to high level	0
2	bS0_2_WIRE	RW	SPI0 2-wire half-duplex mode enable bit, if this bit is 0, 3-wire full-duplex Mode, including SCK, MOSI, MISO; if this bit is 1, it is 2-wire half-duplex mode. Mode, including SCK, MISO	0
1	bS0_CLR_ALL	RW	This bit is 1 to clear the SPI0 interrupt flag and FIFO, which needs to be cleared by software	1
0	bS0_AUTO_IF	RW	Allows automatic clearing of the byte receive complete interrupt flag by valid FIFO operation The enable bit of the FIFO is automatically cleared when the FIFO is effectively read or written. Byte reception completion interrupt flag S0_IF_BYTE	0

SPI0 data transmit and receive register (SPI0\_DATA):

Bit	Name access		The	Reset value
[7:0]	SPI0_DATA	RW	description includes two physically separate FIFOs for sending and receiving. The read operation corresponds to the receive data FIFO; write operation corresponds to send data FIFO, effective read and write operation Can start an SPI transfer	xxh

SPI0 status register (SPI0\_STAT):

Bit	Name access		describe	Reset value
7	S0_FST_ACT	R0	This bit is 1, indicating that the current state is the completion of receiving the first byte in slave mode.	0
6	S0_IF_OV	RW	FIFO overflow flag in slave mode, this bit is 1, indicating FIFO overflow. If the bit is 0, there is no interrupt. Directly write 0 to clear the corresponding bit of the register. Write 1 to clear. When bS0_DATA_DIR=0, the transmit FIFO empty triggers an interrupt; When bS0_DATA_DIR=1, the receive FIFO is full and triggers an interrupt.	0
5	S0_IF_FIRST	RW	In slave mode, the first byte received is completed. If this bit is 1, it indicates The first byte is received. Directly write 0 to clear the bit or write 1 to the corresponding bit of the	0
4	S0_IF_BYTE	RW	register to clear the data byte transmission completion interrupt flag. If the bit is 1, it means one byte The transfer is complete. Directly write 0 to clear the bit or write 1 to clear the corresponding bit of the register, or or cleared by FIFO valid operation when bS0_AUTO_IF=1	0
3	S0_FREE	R0	SPI0 idle flag, this bit is 1, indicating that there is no SPI shift at present. Often the gap between data bytes	1
2	S0_T_FIFO	R0	SPI0 transmit FIFO count, valid value is 0 or 1 R0 Reserved R0 SPI0 receive	0
1	reserve	FIFO count, valid		0
0	S0_R_FIFO	value is 0 or 1		0

#### 14.3 SPI Transmission Format

SPI master mode supports two transmission formats: Mode 0 and Mode 3. You can set the SPI control register SPIn\_CTRL to

The bit bSn\_MST\_CLK is selected, CH552 always samples MISO data on the rising edge of CLK. The data transmission format is shown in the figure below.

Mode 0: bSn\_MST\_CLK = 0

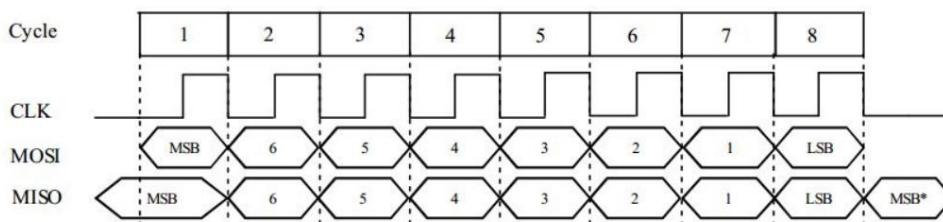


Figure 14.3.1 SPI Mode 0 Timing Diagram

Mode 3: bSn\_MST\_CLK = 1

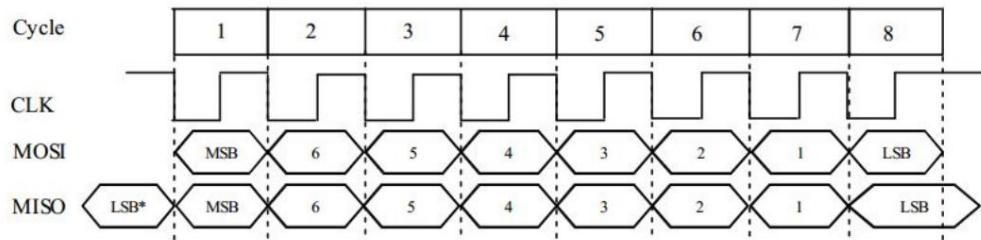


Figure 14.3.2 SPI Mode 3 Timing Diagram

## 14.4 SPI Configuration

### 14.4.1 SPI Master Mode Configuration

In SPI master mode, the SCK pin outputs the serial clock, and the chip select output pin can be designated as any I/O pin.

SPI0 configuration steps:

(1) Set the SPI clock divider setting register SPI0\_CK\_SE to configure the SPI clock frequency. (2) Set the bit bS0\_MODE\_SLV in the SPI setting register SPI0\_SETUP to 0 to configure it to host mode. (3) Set the bit bS0\_MST\_CLK in the SPI control register SPI0\_CTRL to mode 0 or 3 as required. (4) Set the bits bS0\_SCK\_OE and bS0\_MOSI\_OE in the SPI control register SPI0\_CTRL to 1 and the bit bS0\_MISO\_OE to 0 to set the P1 port direction bSCK and bMOSI to output, bMISO to input, and the chip select pin to output.

Data sending process:

(1) Write the SPI0\_DATA register to write the data to be sent to the FIFO, and automatically start an SPI transmission. (2) Wait for S0\_FREE to be 1, indicating that the transmission is completed and the next byte can be sent.

Data receiving process:

(1) Write the SPI0\_DATA register and write arbitrary data, such as 0FFh, to the FIFO to start an SPI transfer. (2) Wait for S0\_FREE to be 1, indicating that the reception is complete. You can then read SPI0\_DATA to obtain the received data. (3) If bS0\_DATA\_DIR was previously set to 1, the above read operation will also start the next SPI transfer; otherwise, it will not start.

### 14.4.2 SPI Slave Mode Configuration

Only SPI0 supports slave mode. In slave mode, the SCK pin is used to receive the serial clock from the connected SPI master.

(1) Set the bit bS0\_MODE\_SLV of the SPI0 setup register SPI0\_SETUP to 1 and configure it to slave mode. (2) Set the bits bS0\_SCK\_OE and bS0\_MOSI\_OE of the SPI0 control register SPI0\_CTRL to 0, set bS0\_MISO\_OE to 1, and set the P1 port direction bSCK, bMOSI and bMISO and the chip select pins to input. When the SCS chip select is valid (low level), MISO will automatically enable the output. It is also recommended to set the MISO pin to high-impedance input mode (P1\_MOD\_OC[6]=0, P1\_DIR\_PU[6]=0), so that MISO does not output during the chip select invalid period, which facilitates sharing of the SPI bus. (3) Optionally, set the SPI slave mode preset data register SPI0\_S\_PRE, which is used to automatically load the data into the buffer for external output after the chip is selected. After 8 serial clocks, that is, the first data byte transmission exchange is completed, CH552 receives the first byte of data sent by the external SPI host (possibly a command code), and the external SPI host exchanges the preset data in SPI0\_S\_PRE (possibly a status value). Bit 7 of register SPI0\_S\_PRE will be automatically loaded to the MISO pin during the SCK low level period after the SPI chip select is valid. For SPI mode 0, if CH552 presets bit 7 of SPI0\_S\_PRE, then the external SPI host will be able to obtain the preset value of bit 7 of SPI0\_S\_PRE by querying the MISO pin when the SPI chip select is valid but no data has been transmitted. Therefore, the value of bit 7 of SPI0\_S\_PRE can be obtained by simply validating the SPI chip select.

**Data sending process:**

Query S0\_IF\_BYTE or wait for interrupt, write SPI0\_DATA register after each SPI data byte transmission is completed.

Write the data to be sent into FIFO, or wait for S0\_FREE to change from 0 to 1 before sending the next byte.

**Data receiving process:**

Query S0\_IF\_BYTE or wait for interrupt, read SPI0\_DATA register after each SPI data byte transmission is completed,

FIFO gets the received data. Querying S0\_R\_FIFO can determine whether there are any remaining bytes in the FIFO.

**15. Analog-to-digital converter ADC and voltage comparator (not applicable to CH551)****15.1 Introduction to ADC**

The CH552 chip provides an 8-bit analog-to-digital converter, including a voltage comparator and an ADC module.

The signal input channel can be collected in time-sharing mode and supports analog input voltage range from 0 to VCC.

**15.2 ADC Registers**

Table 15.2.1 ADC related register list

name	address	describe	Reset value
ADC_CTRL	80 hours	ADC Control Register	x0h
ADC_CFG	9AH	ADC Configuration Register	00h
ADC_DATA	9Fh	ADC data register	xxh

**ADC Control Register (ADC\_CTRL):**

Bit	name	access		Reset value
7	CMP0	RO	Describes the voltage comparator result output bit. This bit is 0 and indicates the positive input terminal. The voltage of the positive input terminal is lower than the voltage of the negative input terminal; if this bit is 1, it means the positive input terminal X The voltage at the input is higher than the voltage at the inverting input	x
6	CMP_IF	RW	Voltage comparator result change flag, this bit is 1, indicating that the voltage comparison If the result of the device has changed, write 0 to clear it.	0
5	ADC_IF	RW	ADC conversion complete interrupt flag, this bit is 1, indicating an ADC conversion is complete. After the change is completed, write 0 directly to clear the bit	0
4	ADC_START	RW	ADC start control bit, set to 1 to start an ADC conversion. ADC automatically clears after conversion is completed	0
3	CMP_CHAN	RW	Voltage comparator inverting input selection: 0-AIN1; 1-AIN3	0
2	Reserved	R0 reserved		0
1	ADC_CHAN1	RW	Voltage comparator non-inverting input and ADC input channel selection high 0	
0	ADC_CHAN0	RW	Voltage comparator non-inverting input and ADC input channel selection low 0	

Table 15.2.1 Voltage Comparator CMP Non-inverting Input and ADC Input Channels

ADC_CHAN1	ADC_CHAN0	the voltage comparator non-inverting input and ADC input channel
0	0	AIN0̄P1.1̄
0	1	AIN1 (P1.4)
1	0	AIN2̄P1.5̄
1	1	AIN3̄P3.2̄

ADC Configuration Register (ADC\_CFG):

Bits	Name	access	describe	Reset value
[7:4]	reserved	R0 reserved		0000b
3	ADC_EN	RW	The power control bit of the ADC module. When the bit is 0, it means the ADC module is turned off. The power of the block enters the sleep state; this bit is 1 to turn on the	0
2	CMP_EN	RW	power control bit of the voltage comparator, and this bit is 0 to turn off the voltage The power supply of the comparator enters the sleep state; this bit is 1 to turn on	0
1	reserve	R0 reserved		0
0	ADC_CLK	RW	ADC reference clock frequency selection bit, this bit is 0 to select slow clock, Each ADC needs 384 Fosc cycles; when this bit is 1, fast Clock, each ADC needs 96 Fosc cycles	0

ADC data register (ADC\_DATA):

Bit	Name access		describe	Reset value
[7:0]	ADC_DATA	RO ADC	sampling result data	xxh

### 15.3 ADC Function

ADC sampling mode configuration steps:

- (1) Set the ADC\_EN bit in the ADC\_CFG register to 1 to turn on the ADC module and set bADC\_CLK to select the frequency.
- (2) Set ADC\_CHAN1/0 in the ADC\_CTRL register to select the input channel.
- (3) Optionally, clear the interrupt flag ADC\_IF. Optionally, if interrupt mode is used, you also need to enable interrupts here.
- (4) Set ADC\_START in the ADC\_CTRL register to start an ADC conversion.
- (5) Wait for ADC\_START to become 0, or ADC\_IF to be set to 1 (if it has been cleared before), indicating that the ADC conversion is completed.

ADC\_DATA reads the result data. The data is the value of the input voltage divided by 255 with respect to the VCC power supply voltage.

If the data is 47, it means the input voltage is close to 47/255 of the VCC voltage. If the VCC power supply voltage is also uncertain, you can

Measure another certain reference voltage value, and then calculate the measured input voltage value and VCC power supply voltage value in proportion.

- (6) If ADC\_START is set again, the next ADC conversion can be started.

Voltage comparator mode configuration steps:

- (1) Set the CMP\_EN bit in the ADC\_CFG register to 1 to enable the voltage comparator module.
- (2) Set ADC\_CHAN1/0 and CMP\_CHAN in the ADC\_CTRL register to select the positive and negative input terminals.
- (3) Optionally, clear the flag CMP\_IF.
- (4) The status of the CMPO bit can be queried at any time to obtain the current comparator result.
- (5) If CMP\_IF becomes 1, it means that the result of the comparator has changed.

The GPIO pins of the selected analog signal input channels must be set to high-impedance input mode or open-drain output mode.

And it is in the output 1 state (equivalent to high-impedance input), Pn\_DIR\_PU[x]=0, and it is recommended to turn off the pull-up resistor and pull-down resistor.

## 16. USB controller

### 16.1 Introduction to USB Controllers

CH552 has built-in USB controller and USB transceiver, with the following features:

- (1) Support USB Device function, support USB 2.0 full speed 12Mbps or low speed 1.5Mbps;
- (2) Support USB control transmission, batch transmission, interrupt transmission, synchronous/real-time transmission;
- (3) Supports data packets up to 64 bytes, built-in FIFO, and supports interrupts and DMA.

The USB related registers of CH552 are divided into two parts: USB global registers and USB endpoint registers.

## 16.2 Global Registers

Table 16.2.1 USB Global Register List (grayed out registers are controlled by bUC\_RESET\_SIE reset)

name	address		Reset value
USB_C_CTRL	Description 91h USB type-C configuration channel control register		0000 0000b
USB_INT_FG	D8h USB interrupt Flag Register		0010 0000b
USB_INT_ST	D9h USB interrupt status register (read only)		00xx xxxx b
USB_MIS_ST	DAh USB Miscellaneous Status Register (read only)		xx10 1000b
USB_RX_LEN	DBh USB receive length register (read only)		0xxx xxxx b
USB_INT_EN	E1h USB interrupt enable register		0000 0000b
USB_CTRL	E2h USB Control Register		0000 0110b
USB_DEV_AD	E3h USB device address register		0000 0000b

USB type-C configuration channel control register (USB\_C\_CTRL): (not applicable to CH551)

Bit	Name Access Description RW	This bit is 1 to enable the internal 10K pull-down resistor of the VBUS2 pin; 0 to disable	0	Reset value
7	bVBUS2_PD_EN	of the VBUS2 pin; 0 to disable 0 RW This bit is 1 to enable the internal 5.1K pull-down resistor of the UCC2 pin; 0 to		
6	bUCC2_PD_EN	disable 0 RW This bit is the internal pull-up resistor control selection high bit of the UCC2 pin RW This bit is the		
5	bUCC2_PU1_EN	internal pull-up resistor control selection low bit of the UCC2 pin RW This bit is 1 to enable	0	
4	bUCC2_PU0_EN	the internal 10K pull-down resistor of the VBUS1 pin; 0 to disable 0 RW This bit is 1 to	0	
3	bVBUS1_PD_EN	enable the internal 5.1K pull-down resistor of the UCC1 pin; 0 to disable 0 RW This bit is the internal pull-up resistor		
2	bUCC1_PD_EN	control selection high bit of the UCC1 pin RW This bit is the internal pull-up resistor control selection low bit of the		
1	bUCC1_PU1_EN	UCC1 pin	0	
0	bUCC1_PU0_EN	The internal pull-up resistor of the UCCn pin is selected by bUCCn_PU1_EN and bUCCn_PU0_EN.	0	

The above USB type-C pull-up resistors and pull-down resistors are independent of the Pn\_DIR\_PU port direction control and pull-up enable registers.

bUCCn_PU1_EN bUCCn_PU0_EN		Select the internal pull-up resistor of the UCCn pin
0	0	Disable the internal pull-up resistor
0	1	Enable the internal 56K $\Omega$ pull-up resistor, indicating that the default USB current is provided.
1	0	Enabling the internal 22K $\Omega$ pull-up resistor means it can provide 1.5A current
1	1	Enable the internal 10K $\Omega$ pull-up resistor, which means it can provide 3A current.

When a pin is used for USB type-C, the pull-up resistor of the port corresponding to the pin should be disabled.

The pin enables high-impedance input mode (to prevent the pin from outputting a low level or a high level).

For detailed control and input detection of the USB type-C configuration channel, please refer to the USB type-C application description and examples.

USB interrupt flag register (USB\_INT\_FG):

Bit name access			Reset value
7	U_IS_NAK	RO	Description: When this bit is 1, it indicates that a NAK busy response is received during the current USB transmission process. A bit of 0 indicates a non-NAK response was received.
6	U_TOG_OK	RO	The current USB transmission DATA0/1 synchronization flag matching status, this bit is 1 to indicate Synchronous, the data is valid; if this bit is 0, it means it is not synchronized and the data may be invalid
5	U_SIE_FREE	RO	The idle status bit of the USB protocol processor. If the bit is 0, it means it is busy and in progress. USB transfer; this bit is 1 when USB is idle

4	UIF_FIFO_OV	RW	USB FIFO overflow interrupt flag, this bit is 1, indicating FIFO overflow interrupt; This bit is 0, no interrupt. Write 0 to clear the bit directly or write 1 to clear the corresponding bit in the register. 0 zero	0
3	reserve	RO Reserved		0
2	UIF_SUSPEND	RW	USB bus suspend or wake-up event interrupt flag. When this bit is 1, it indicates that there is a The interrupt is triggered by the USB suspend event or wake-up event; this bit is 0 Directly write 0 to clear the bit or write 1 to clear the corresponding bit in the register.	0
1	UIF_TRANSFER	RW	USB transfer completion interrupt flag, this bit is 1, indicating an interrupt. A USB transfer is completed trigger; this bit is 0 means no interrupt. Direct bit write 0 Clear or write 1 to the corresponding bit in the register to clear	0
0	UIF_BUS_RST	RW	USB bus reset event interrupt flag, this bit is 1, indicating an interrupt. The interrupt is triggered by a USB bus reset event; a 0 in this bit indicates no interrupt. Write 0 to clear the bit or write 1 to clear the corresponding bit in the register.	0

USB Interrupt Status Register (USB\_INT\_ST):

Bit	Name access			Reset value
7	tube_IS_NAK	RO	Description: When this bit is 1, it indicates that a NAK busy response is received during the current USB transmission process. Same as U_IS_NAK	0
6	bUIS_TOG_OK	RO	Current USB transmission DATA0/1 synchronization flag matching status, this bit is 1 Indicates synchronization; 0 indicates out of synchronization. Same as U_TOG_OK	0
5	buis_token1	RO	The token PID of the current USB transfer transaction identifies the high bit	x
4	bUIS_TOKEN0	RO	PID identifier low bit of the current USB transfer transaction	x
[3:0] MASK	UIS_ENDP	RO	The endpoint number of the current USB transfer transaction, 0000 represents endpoint 0; ...; 1111 indicates endpoint 15	xxxxb

bUIS\_TOKEN1 and bUIS\_TOKEN0 form MASK\_UIS\_TOKEN, which is used to identify the token PID of the current USB transfer transaction:

00 indicates OUT packet; 01 indicates SOF packet; 10 indicates IN packet; 11 indicates SETUP packet.

USB Miscellaneous Status Register (USB\_MIS\_ST):

Bits	Name access reservation		describe	Reset value
[7:6]		RO Reserved		xxb
5	bUMS_SIE_FREE	RO	The idle status bit of the USB protocol processor. If the bit is 0, it means it is busy. U_SIE_FREE USB	1
4	bUMS_R_FIFO_RDY	RO	receive FIFO data ready status bit, this bit is 0 means receiving FIFO is empty; this bit is 1, indicating that the receive FIFO is not empty.	0
3	bUMS_BUS_RESET	RO	USB bus reset status bit. If this bit is 0, it means there is no USB bus. Line reset; this bit is 1, indicating that the USB bus is currently being reset.	1
2	bUMS_SUSPEND	RO	USB suspend status bit, this bit is 0, which means there is USB activity. A bit of 1 indicates that there has been no USB activity for a while and a suspend request is requested.	0
[1:0]	reserve	RO Reserved		00b

USB receive length register (USB\_RX\_LEN):

Bits	Name access		describe	Reset value
[7:0]	bUSB_RX_LEN	RO	The number of bytes of data received by the current USB endpoint	xxh

USB Interrupt Enable Register (USB\_INT\_EN):

Bit	name	Access	Description	Reset value
7	bUIE_DEV_SOF	RW	This bit is 1 to enable the SOF packet interrupt; 0 to disable	0
6	bUIE_DEV_NAK	RW	This bit is 1 to enable the NAK interrupt; 0 to disable	0
5		RO	Reserved	0
4	bUIE_FIFO_OV	RW	This bit is 1 to enable FIFO overflow interrupt; this bit is 0 to disable	0
3		RO	Reserved	0
2	BUIE_SUSPEND	RW	This bit is 1 to enable USB bus suspend or wake-up event interrupt; 0 to disable	0
1	bUIE_TRANSFER	RW	This bit is 1 to enable the USB transfer completion interrupt; this bit is 0 to disable	0
0	bUIE_BUS_RST	RW	This bit is 1 to enable the USB bus reset event interrupt; this bit is 0 to disable	0

USB Control Register (USB\_CTRL):

Bit	Name	access	reservation	describe	Reset value
7		RO	Reserved		0
6	bUC_LOW_SPEED	RW		USB bus signal transmission rate selection bit, this bit is 0 to select full speed 12Mbps; This bit is 1 to select the low-speed 1.5Mbps USB	0
5	bUC_DEV_PU_EN	RW		device enable and internal pull-up resistor control bit. This bit is 1 to enable USB The device transmits and enables the internal pull-up resistor	0
5	bUC_SYS_CTRL1	RW	USB	system control high RW USB	0
4	bUC_SYS_CTRL0		system	control low USB transfer completion	0
3	bUC_INT_BUSY	RW		interrupt flag is not cleared before the automatic pause enable bit, this bit is 1, it will automatically pause before the interrupt flag UIF_TRANSFER is cleared. Active response busy NAK; if this bit is 0, no pause	0
2	bUC_RESET_SIE	RW		USB protocol processor software reset control bit, this bit is 1 to force reset USB The protocol processor and most USB control registers need to be cleared by software	1
1	bUC_CLR_ALL	RW	This	bit is 1 to clear the USB interrupt flag and FIFO, which needs to be cleared by software	1
0	bUC_DMA_EN	RW	This	bit is 1 to enable USB DMA and DMA interrupt; 0 to disable	0

The USB system control group is composed of bUC\_SYS\_CTRL1 and bUC\_SYS\_CTRL0:

bUC_SYS_CTRL1	bUC_SYS_CTRL0	USB System Control Description
0	0	Disable USB device function and turn off internal pull-up resistor
0	1	Enable USB device function, turn off internal pull-up, and add external pull-up
1	X	Enable the USB device function and enable the internal 1.5K $\Omega$ pull-up resistor. This pull-up resistor takes precedence over the pull-down resistor and can also be used in GPIO mode.

USB device address register (USB\_DEV\_AD):

Bit	Name	access	bUDA	GP_BIT	describe	Reset value
7		RW	USB	general flag: user-defined, can be cleared or set to 0 by software		
[6:0]	MASK_USB_ADDR	RW		The	address of the USB device	00h

### 16.3 Endpoint Registers

CH552 provides 5 groups of bidirectional endpoints, namely endpoints 0, 1, 2, 3 and 4. The maximum data packet length of all endpoints is 64 bytes.

Endpoint 0 is the default endpoint, which supports control transfers. Sending and receiving share a 64-byte data buffer.

Endpoint 1, Endpoint 2, and Endpoint 3 each include a sending endpoint IN and a receiving endpoint OUT, each with a separate

Independent 64-byte or dual 64-byte data buffers support control transfers, bulk transfers, interrupt transfers, and real-time/isochronous transfers.

Endpoint 4 includes a transmit endpoint IN and a receive endpoint OUT. Each of the transmit and receive endpoints has an independent 64-byte data buffer.

Buffer area, supporting control transmission, bulk transmission, interrupt transmission and real-time/synchronous transmission.

Each endpoint has a control register UEPn\_CTRL and a transmit length register UEPn\_T\_LEN (n=0/1/2/3/4).

It is used to set the synchronization trigger bit of the endpoint, the response to OUT transactions and IN transactions, and the length of the sent data.

As the USB bus pull-up resistor necessary for USB devices, the software can set whether to enable it at any time.

When bUC\_DEV\_PU\_EN in USB\_CTRL is set to 1, CH552 internally switches the DP pin of the USB bus or

The DM pin is connected to a pull-up resistor and the USB device function is enabled.

When a USB bus reset, USB bus suspend or wake-up event is detected, or when the USB successfully processes the data transmission or data

After receiving, the USB protocol processor will set the corresponding interrupt flag and generate an interrupt request. The application can directly query or

In the interrupt service routine, query and analyze the interrupt flag register USB\_INT\_FG, and perform corresponding operations according to UIF\_BUS\_RST and UIF\_SUSPEND.

And, if UIF\_TRANSFER is valid, then it is necessary to continue to analyze the USB interrupt status register USB\_INT\_ST.

Process accordingly based on the current endpoint number MASK UIS\_ENDP and the current transaction token PID MASK UIS\_TOKEN.

First set the synchronous trigger bit bUEP\_R\_TOG of the OUT transaction of each endpoint, then you can use U\_TOG\_OK or bUIS\_TOG\_OK

Determine whether the synchronization trigger bit of the currently received data packet matches the synchronization trigger bit of the endpoint. If the data is synchronized, the data

If the data is not synchronized, it should be discarded. After each USB send or receive interrupt is processed, the

Change the synchronization trigger bit of the corresponding endpoint to synchronize the data packet sent next time and detect whether the data packet received next time is synchronized;

In addition, by setting bUEP\_AUTO\_TOG, the corresponding synchronization trigger bit can be automatically flipped after successful transmission or reception.

The data to be sent by each endpoint is in its own buffer, and the length of the data to be sent is independently set in UEPn\_T\_LEN

The data received by each endpoint is in its own buffer, but the length of the received data is in the USB receive length register.

In USB\_RX\_LEN, it can be distinguished according to the current endpoint number when the USB receive interrupt occurs.

Table 16.3.1 USB device endpoint related register list (grayed out registers are reset by bUC\_RESET\_SIE)

name	address	describe	Reset value
UDEV_CTRL	D1h	USB device physical port control register	10xx 0000b
UEP1_CTRL	D2h	Endpoint 1 Control Register	0000 0000b
UEP1_T_LEN	D3h	Endpoint 1 Send Length Register	0xxx xxxx b
UEP2_CTRL	D4h	Endpoint 2 Control Register	0000 0000b
UEP2_T_LEN	D5h	Endpoint 2 Send Length Register	0000 0000b
UEP3_CTRL	D6h	Endpoint 3 Control Register	0000 0000b
UEP3_T_LEN	D7h	Endpoint 3 Send Length Register	0xxx xxxx b
UEP0_CTRL	DCh	Endpoint 0 Control Register	0000 0000b
UEP0_T_LEN	DDh	Endpoint 0 Send Length Register	0xxx xxxx b
UEP4_CTRL	DEh	Endpoint 4 Control Register	0000 0000b
UEP4_T_LEN	DFh	Endpoint 4 Send Length Register	0xxx xxxx b
UEP4_1_MOD	EAh	Endpoint 1, 4 mode control register	0000 0000b
UEP2_3_MOD	EBh	Endpoint 2, 3 mode control register	0000 0000b
UEP0_DMA_H	EDh	Endpoint 0 and 4 buffer start address high byte	0000 00xx b
UEP0_DMA_L	ECh	Endpoint 0 and 4 buffer start address low byte	xxxx xxxx b
UEP0_DMA	ECh	UEP0_DMA_L and UEP0_DMA_H form a 16-bit SFR	0xxx h
UEP1_DMA_H	EFh	Endpoint 1 buffer start address high byte	0000 00xx b
UEP1_DMA_L	EEh	Endpoint 1 buffer start address low byte	xxxx xxxx b
UEP1_DMA	EEh	UEP1_DMA_L and UEP1_DMA_H form a 16-bit SFR	0xxx h
UEP2_DMA_H	E5h	Endpoint 2 buffer start address high byte	0000 00xx b
UEP2_DMA_L	E4h	Endpoint 2 buffer start address low byte	xxxx xxxx b

UEP2_DMA	E4h UEP2	DMA_L and UEP2_DMA_H form a 16-bit SFR	0xxxh
UEP3_DMA_H	E7h Endpoint 3 buffer start address high byte		0000 00xxb
UEP3_DMA_L	E6h Endpoint 3 buffer start address low byte		xxxx xxxxh
UEP3_DMA	E6h UEP3	DMA_L and UEP3_DMA_H form a 16-bit SFR	0xxxh

USB device physical port control register (UDEV\_CTRL), reset controlled by bUC\_RESET\_SIE:

Bit name access				Reset value
7 bUD_PD_DIS	RW	Describes the internal pull-down resistor disable bit of the USB device port UDP/UDM pin. This bit is 1. Disable the internal pull-down resistor; this bit is 0 to enable the internal pull-down resistor. Controlled by bUSB_IO_EN, it can also be used in GPIO mode to provide a pull-down resistor		1
6 reserve	RO Reserved			0
5 bUD_DP_PIN	RO Current	Current UDP pin status, 0 indicates low level; 1 indicates high level		
4 bUD_DM_PIN	RO Current	Current UDM pin status, 0 indicates low level; 1 indicates high level		
3 Reserved	RO Reserved			0
2 bUD_LOW_SPEED	RW	USB device physical port low speed mode enable bit, this bit is 1 to select 1.5Mbps Low speed mode; this bit is 0 to select 12Mbps full speed mode		0
1 bUD_GP_BIT	RW Device	general flag bit: User can define it by himself, and software can clear or set it to 0 USB device physical		
0 bUD_PORT_EN	RW	port enable bit. This bit is 1 to enable the physical port; this bit is 0 Disable the physical port		0

Endpoint n Control Register (UEPn\_CTRL):

Bit name access				Reset value
7 bUEP_R_TOG	RW	Describes the synchronous trigger expected by the receiver of USB endpoint n (handling SETUP/OUT transactions) Bit, this bit is 0, indicating that DATA0 is expected; it is 1, indicating that DATA1 is		0
6 bUEP_T_TOG	RW	expected. The transmitter of USB endpoint n (processing IN transaction) prepares the synchronization trigger bit. 0 means sending DATA0; 1 means sending DATA1 RO reserves the		0
5 reserve	synchronization			0
4 bUEP_AUTO_TOG	RW	trigger bit automatic flip enable control bit. When the bit is 1, it means sending DATA1. After the success or reception, the corresponding synchronization trigger bit will be automatically flipped; 0 means no Automatic flip, but can be switched manually. Only supports endpoints 1/2/3		0
3 bUEP_R_RES1	RW Endpoint n receiver response to SETUP/OUT transaction control high RW Endpoint n			0
2 bUEP_R_RES0	receiver response to SETUP/OUT transaction control low RW Endpoint n transmitter response			0
1 bUEP_T_RES1	to IN transaction control high RW Endpoint n transmitter response to IN			0
0 bUEP_T_RES0	transaction control low MASK_UEP_R_RES composed of bUEP_R_RES1 and			0

bUEP\_R\_RES0 is used to control the endpoint n receiver response to SETUP/OUT

Transaction response mode: 00 means ACK or ready; 01 means timeout/no response, used to implement real-time/synchronous transmission of non-endpoint 0

10 means the response is NAK or busy; 11 means the response is STALL or error.

MASK\_UEP\_T\_RES, which is composed of bUEP\_T\_RES1 and bUEP\_T\_RES0, is used to control the transmitter of endpoint n to IN transactions.

Response mode: 00 means response to DATA0/DATA1 or data ready and expect ACK; 01 means response to DATA0/DATA1 and expect no response

10 indicates a response of NAK or busy; 11 indicates a response of STALL or error.

Endpoint n send length register (UEPn\_T\_LEN):

Bits	Name access		describe	Reset value
[7:0]	bUEPn_T_LEN	RW Set	the number of data bytes that USB endpoint n is ready to send (n=0/1/3/4)	xxh

	bUEP2_T_LEN		Set the number of data bytes that USB endpoint 2 is ready to send	00h
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USB endpoint 1, 4 mode control register (UEP4\_1\_MOD):

Bit	Name access		describe	Reset value
7	bUEP1_RX_EN	RW This	bit is 0 to disable endpoint 1 reception; 1 to enable endpoint 1 reception (OUT)	0
6	bUEP1_TX_EN Reserved	RW This	bit is 0 to disable endpoint 1 transmission; 1 to enable endpoint 1 transmission (IN)	0
5		RO Reserved		0
4	bUEP1_BUF_MOD	RW Endpoint 1 data buffer mode control bit		0
3	bUEP4_RX_EN	RO This	bit is 0 to disable endpoint 4 reception; 1 to enable endpoint 4 reception (OUT)	0
2	bUEP4_TX_EN Reserved	RW This	bit is 0 to disable endpoint 4 transmission; 1 to enable endpoint 4 transmission (IN)	0
[1:0] The		RO Reserved		00b

data buffer mode of USB endpoints 0 and 4 is controlled by the combination of bUEP4\_RX\_EN and bUEP4\_TX\_EN. Refer to the table below.

Table 16.3.2 Endpoint 0 and 4 Buffer Mode

bUEP4_RX_EN bUEP4_TX_EN 0 Endpoint 0		Structure description: Arrange from low to high with UEP0_DMA as the starting address
0	single 64-byte	transmit and receive shared buffer (IN and OUT) 0 Endpoint 0 single 64-byte
1	transmit and receive shared buffer; Endpoint 4 single 64-byte receive buffer (OUT)	
0	1 Endpoint 0	single 64-byte send and receive shared buffer; Endpoint 4 single 64-byte send buffer (IN)
		Endpoint 0 single 64-byte send and receive shared buffer; Endpoint 4 single 64-byte receive buffer (OUT); Endpoint 4 has a single 64-byte transmit buffer (IN). The entire 192 bytes are arranged as follows: UEP0_DMA+0 address: endpoint 0 is shared by both sending and receiving; UEP0_DMA+64 address: endpoint 4 receive; UEP0_DMA+128 Address: Endpoint 4 Send

USB endpoint 2, 3 mode control register (UEP2\_3\_MOD):

Bit name	access		describe	Reset value
7	bUEP3_RX_EN	RW This	bit is 0 to disable endpoint 3 reception; 1 to enable endpoint 3 reception (OUT)	0
6	bUEP3_TX_EN Reserved	RW This	bit is 0 to disable endpoint 3 transmission; 1 to enable endpoint 3 transmission (IN)	0
5		RO Reserved		0
4	bUEP3_BUF_MOD	RW Endpoint 3 data buffer mode control bit		0
3	bUEP2_RX_EN	RO This	bit is 0 to disable endpoint 2 reception; 1 to enable endpoint 2 reception (OUT)	0
2	bUEP2_TX_EN Reserved	RW This	bit is 0 to disable endpoint 2 transmission; 1 to enable endpoint 2 transmission (IN)	0
1		RO Reserved		0
0	bUEP2_BUF_MOD	RW Endpoint 2 data buffer mode control bit		0

The combination of bUEPn\_RX\_EN, bUEPn\_TX\_EN and bUEPn\_BUF\_MOD (n=1/2/3) controls USB endpoints 1, 2, and 3 respectively.

Refer to the table below for the data buffer mode. In the dual 64-byte buffer mode, USB data transmission will be based on bUEP\_\*\_TOG=0.

Select the first 64-byte buffer and select the second 64-byte buffer according to bUEP\_\*\_TOG=1 to achieve automatic switching.

Table 16.3.3 Endpoint n buffer mode (n=1/2/3)

bUEPn_RX_EN bUEPn_TX_EN bUEPn_BUF_MOD				Structure description: Arrange from low to high with UEPn_DMA as the starting address
0	0	x	endpoint is disabled and the UEPn_DMA buffer is not used	
1	0	0	Single 64-byte receive buffer (OUT) Dual 64-byte	
1	0	1	receive buffer, selected by bUEP_R_TOG	
0	1	0	Single 64-byte transmit buffer (IN) Dual 64-byte	
0	1	1	transmit buffer, selected by bUEP_T_TOG	

1	1	0	Single 64-byte receive buffer; single 64-byte send buffer
1	1	1	<p>Dual 64-byte receive buffer, selected by bUEP_R_TOG; Dual 64 Byte transmit buffer, selected by bUEP_T_TOG.</p> <p>All 256 bytes are arranged as follows:</p> <p>UEPn_DMA+0 address: endpoint receive when bUEP_R_TOG=0;</p> <p>UEPn_DMA+64 address: endpoint receive when bUEP_R_TOG=1;</p> <p>UEPn_DMA+128 address: endpoint sends when bUEP_T_TOG=0;</p> <p>UEPn_DMA+192 Address: Endpoint sends when bUEP_T_TOG=1</p>

USB endpoint n buffer start address (UEPn\_DMA) (n=0/1/2/3):

Bit	Name access			Reset value
[7:0]	UEPn_DMA_H	RW	Describes endpoint n buffer start address high byte, only the lower 2 bits are valid, the upper 6 bits are valid Fixed to 0	0xh
[7:0]	UEPn_DMA_L	RW	Endpoint n buffer start address low byte	xxh

Note: The length of the buffer for receiving data >= min (the maximum length of the data packet that may be received + 2 bytes, 64 bytes)

## 17. Touch-Key

### 17.1 Touch-Key Introduction

The CH552 chip provides a capacitance detection module and related timers, with 6 input channels, supporting a capacitance range of 5pF–150pF. The self-capacitance method can support up to 6 touch buttons, and the mutual capacitance method can support up to 15 touch buttons.

### 17.2 Touch-Key Registers

Table 17.2.1 Touch-Key related register list

name	address	describe		Reset value
TKEY_CTRL	C3h	TKEY_CTRL		x0h
TKEY_DATH	C5h	TKEY data high byte (read only)		00h
TKEY_DATL	C4h	TKEY data low byte (read only)		xxh
TKEY_DAT	C4h	TKEY_DATL and TKEY_DATH form a 16-bit SFR		00xxh

Touch-Key Control Register (TKEY\_CTRL):

Bit	name	access		Reset value
7	bTKC_IF	RO	Describes the timing interrupt flag. If bTKD_CHG=0, then in the current timing cycle The interrupt request is automatically set to 1 when the preparation phase ends. It can be cleared automatically or by writing TKEY_CTRL. bTKD_CHG=1 will automatically clear to zero, do not request interrupt, and skip the current cycle period, and then re-prepare and test in the next cycle, and Automatically set to 1 at the end of each cycle to request an interrupt	x
[6:5]	reserve	RO	Reserved	00b
4	bTKC_2MS	RW	Capacitance detection timer period selection: 0-1mS; 1-2mS. The first 87uS of each cycle is the preparation phase, and the remaining time is the detection phase. The above time is based on Fosc=24MHz	0
3	reserve	RO	Reserved	0
2	bTKC_CHAN2	RW	Touch button capacitance detection input selection high	0

1	bTKC_CHAN1	RW Touch button capacitance detection input selection center	0
0	bTKC_CHAN0	RW Touch button capacitance detection input selection low	0

selects the touch button capacitance detection input channel from bTKC\_CHAN2 to bTKC\_CHAN0.

bTKC_CHAN2	bTKC_CHAN1	bTKC_CHAN0	Select the touch button capacitance detection input channel
0	0	0	Turn off the power of the capacitance detection module. Only used as an independent timer interrupt with a period of 1mS or 2mS
0	0	1	TIN0 (P1.0)
0	1	0	TIN1 (P1.1)
0	1	1	TIN2 (P1.4)
1	0	0	TIN3~P1.5~
1	0	1	TIN4 (P1.6)
1	1	0	TIN5~P1.7~
1	1	1	1. Turn on the power of the capacitance detection module but do not connect any channels.

Touch-Key Data Register (TKEY\_DAT):

Bit	Name access		describe	Reset value
7	bTKD_CHG TKEY_DATH[7]	RO	Touch-Key control change flag. If this bit is 1, it means TKEY_CTRL is in  The capacitance detection phase is rewritten, which may cause TKEY_DAT data to be invalid.  And bTKC_IF will not be set at the end of the current cycle.  It is automatically cleared at the end of the preparation phase of the time cycle. This bit needs to be masked when getting data.	0
6	reserve	RO Reserved		0
[5:0]	TKEY_DATH	RO	Touch-Key data high byte.  Automatically cleared when the capacitor is connected; automatically counted during the capacitance detection phase; 00h  Keep the data unchanged so that the timer interrupt program can read it	
[7:0]	TKEY_DATL	RO	Touch-Key data low byte.  Automatically cleared when the capacitor is connected; automatically counted during the capacitance detection phase; xxh  Keep the data unchanged so that the timer interrupt program can read it	

## 17.3 Touch-Key Function

Capacitance detection steps:

(1) Set bTKC\_2MS and bTKC\_CHAN2~bTKC\_CHAN0 in the TKEY\_CTRL register to select the cycle and input channel.

The selected input channel, the GPIO pin where it is located must be set to high-impedance input mode, or open-drain output mode and in input mode.

Output 1 state (equivalent to high impedance input), Pn\_DIR\_PU[x]=0.

(2) Clear bTKC\_IF and enable interrupt IE\_TKEY to wait for the timer interrupt, or enter the interrupt program by actively querying bTKC\_IF.

(3) After the capacitance detection of the current channel is completed, the bTKC\_IF request interrupt will be automatically set, and the preparation phase for the next cycle will be entered.

And keep TKEY\_DAT data unchanged for about 87uS.

(4) Enter the interrupt program, first read the capacitance data of the current channel from TKEY\_DAT, and mask the highest bit bTKD\_CHG.

The data is a relative value and is inversely proportional to the capacitance. The data when the touch button is pressed is smaller than when it is not pressed.

(5) Set bTKC\_2MS and bTKC\_CHAN2~bTKC\_CHAN0 in the TKEY\_CTRL register to select the next input channel.

The write operation will automatically clear bTKC\_IF, ending the interrupt request.

(6) Compare the TKEY\_DAT data read in step (4) with the previously saved data when no key is pressed on the channel to determine whether the capacitance has changed.

and whether a key is pressed.

(7) Interrupt return, and when the capacitance detection of the next channel is completed, it will go to step (3).

## 18. Parameters

18.1 Absolute Maximum Ratings (Critical or exceeding the absolute maximum ratings may cause the chip to malfunction or even be damaged)

name	Parameter	Minimum	Maximum	Unit
FACING	Description Operating	-40	85	°C
TS	Temperature Storage	-55	125	°C
VCC	Temperature Power Supply Voltage (VCC connected to power supply, GND connected to ground)	0.4	5.8	In
VIO	Voltage on other input or output pins except P3.6/P3.7 -0.4 Voltage on P3.6/P3.7 input or output pin	VCC+0.4		In
VIOU		-0.4	V33+0.4	In

18.2 Electrical Parameters 5V (Test Conditions: TA = 25°C, VCC = 5V, Fsys = 6MHz)

name	Parameter Description	Min.	Typ.	Max.	Unit	
VCC5	VCC pin power supply voltage V33 Only external capacitor	3.7	Internal	5	5.5	In
V33	USB power regulator output voltage	3.14		3.27	3.4	In
ICC24M5	Fsys=24MHz Total power supply current when working	8		11		m.a.
ICC6M5	Total power supply current when Fsys=6MHz working	4		6		m.a.
ICC750K5	Fsys=750KHz total power current when working	2		3		m.a.
ISLP5	Total power current after sleep			0.1	0.2	m.a.
ISLP5L	VCC=V33=5V, and select external crystal clock, And bLDO3V3_OFF=1 turns off LDO, Total supply current after full sleep			0.008	0.025	m.a.
IADC5	ADC analog-to-digital conversion module operating			200	800	a
ICMP5	current Voltage comparator module operating current			100	500	a
ITKEY5	Touch Button Capacitance Detection Module Operating			150	250	a
VIL5	Current Low-Level	-0.4			1.2	In
VIH5	Input Voltage High-	2.4			VCC+0.4	In
VOL5	Level Input Voltage Low-Level Output Voltage				0.4	In
VOH5	(12mA Sink Current) High-Level Output Voltage (8mA Output Current)					In
VOH5U	P3.6/P3.7 High-level output voltage (8mA output current) V33-0.4 Input current					In
IIN	without pull-up input Input current	-5		0	5	a
IDN5	with pull-down resistor Input current with	-35		-70	-140	a
IUP5	pull-up resistor	35		70	140	a
IUP5X	Input current when pull-up input flips from low to high 250 Power on reset			400	600	a
Vpot	threshold voltage	2.1		2.3	2.5	In

18.3 Electrical Parameters 3.3V (Test Conditions: TA = 25°C, VCC = V33 = 3.3V, Fsys = 6MHz)

name	Parameter Description		Min.	Typ.	Max.	Unit	
VCC3	VCC pin Power supply voltage		Short V33 to VCC to enable USB	3.0	3.3	3.6	In
	V33 is shorted to VCC, turning off USB			2.8	3.3	3.6	In
ICC12M3	Fsys=total power supply current when operating at 12MHz		3		5		m.a.
ICC6M3	Total power supply current when Fsys=6MHz working		2		4		m.a.
ICC750K3	Fsys=750KHz total power current when working		1		2		m.a.
ISLP3	Total power current after sleep			0.07	0.15		m.a.

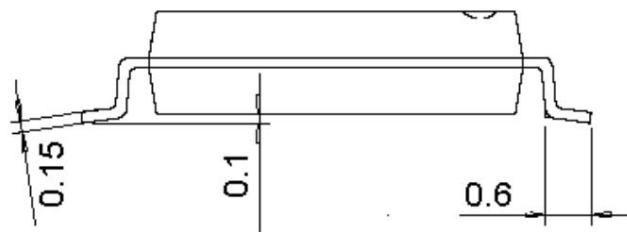
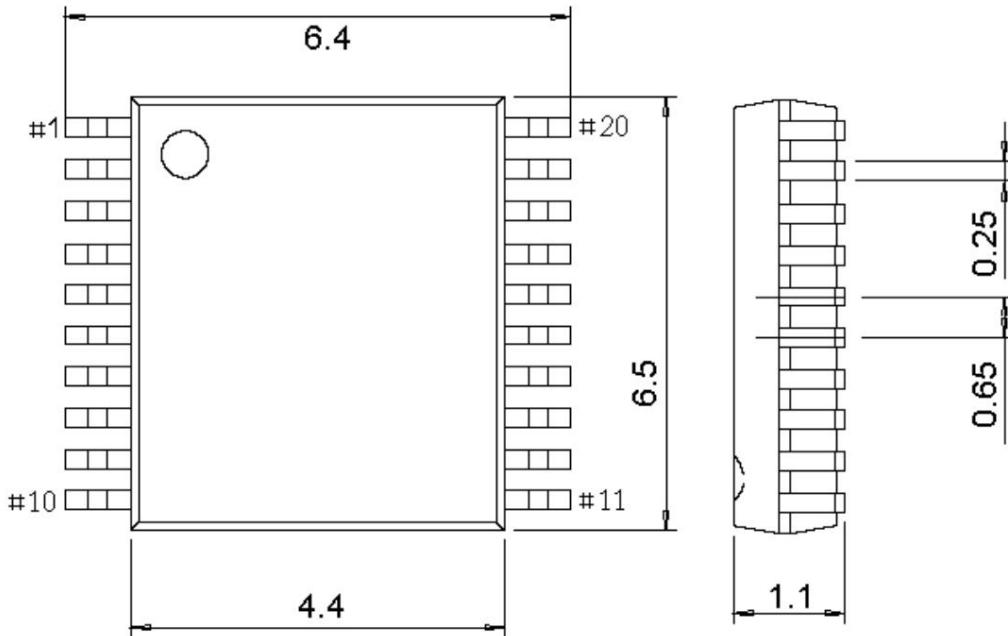
ISLP3L	bLDO3V3_OFF=1 turns off LDO, Total supply current after full sleep		0.004	0.015	m.a.
IADC3	ADC analog-to-digital conversion module operating		150	500	a
ICMP3	current Voltage comparator module operating current		70	300	a
ITKEY3 Touch Button Capacitance Detection Module Operating			130	200	a
VIL3	Current Low-Level	-0.4		0.8	In
HIV3	Input Voltage High-	1.9		VCC+0.4	In
VOL3	Level Input Voltage Low-Level Output Voltage			0.4	In
VOH3	(8mA Sink Current) High-Level Output Voltage (5mA Output Current)				In
VOH3U P3.6/P3.7 high level output voltage (8mA output current) V33-0.4					In
IIN	Input current without pull-up input	-5	0	5	a
IDN3	current with pull-down resistor Input	-15	-30	-60	a
IUP3	current with pull-up resistor	15	30	60	a
IUP3X	Input current when the pull-up input is flipped from low to high 100 Power on		170	250	a
Vpot	reset threshold voltage	2.1	2.3	2.5	In

18.4 Timing Parameters (Test Conditions: TA = 25°C, VCC = 5V or VCC = V33 = 3.3V, Fsys = 6MHz) Min. Typ. Max.

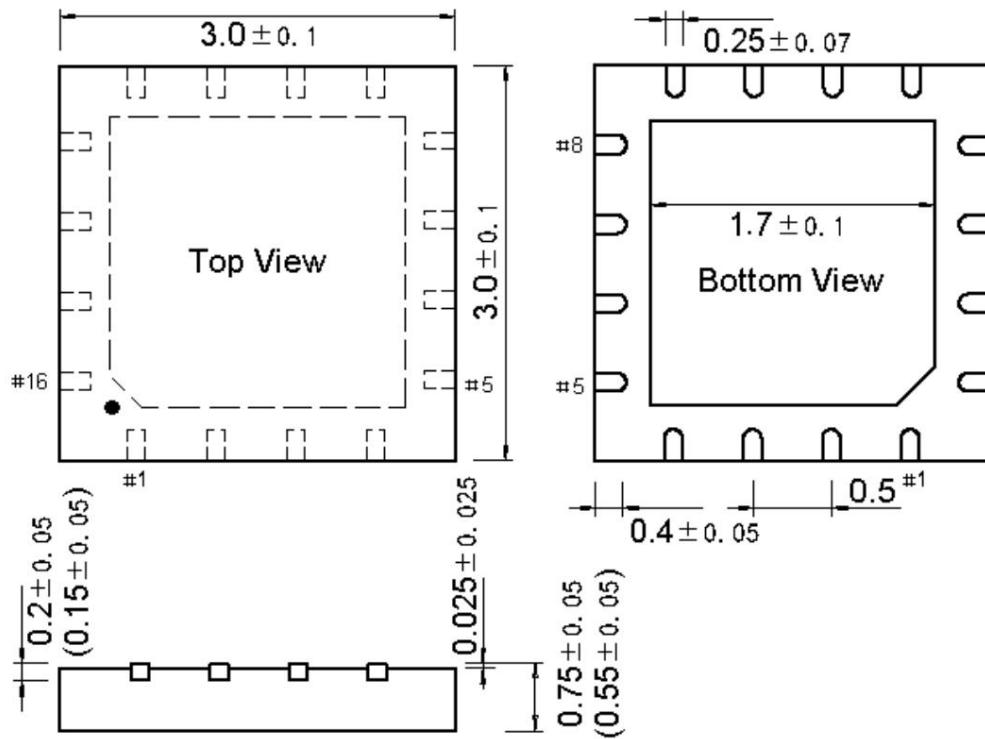
Name	Parameter Description	Unit			
Fxt	External crystal frequency or XI input clock frequency Fosc	6	24	25	MHz
Calibrated	internal clock frequency 23.52 when V33=3V~3.6V Fosc28 Calibrated internal		24	24.48	MHz
clock frequency	23 when V33=2.8V~3V Calibrated internal clock frequency 21 when		24	24.72	MHz
Fosc27	V33<2.8V PLL frequency after internal multiplication Fusb4x When		24	25	MHz
Fpll	using USB device function, USB	24	96	100	MHz
sampling clock frequency	47.04		48	48.96	MHz
Fsys	System main clock frequency (VCC>=4.5V)	0.1	6	24	MHz
	System main clock frequency (4.5V>VCC>=3.8V)	0.1	6	16	MHz
	System main clock frequency (VCC<3.8V)	0.1	6	12	MHz
Tpor	Power-on reset delay	9	11	15	μs
Trst:	The width of the valid reset signal input from RST externally.	70			ns
Trdl		30	45	60	μs
Twdc	Watchdog overflow period / timing period calculation formula $65536 * (0x100 - \text{WDOG\_COUNT}) / \text{Fsys}$				
Tusp	Detect USB auto-suspend time	4	5	6	ms
Twak	Chip wake-up completion time after sleep	1	2	10	μs

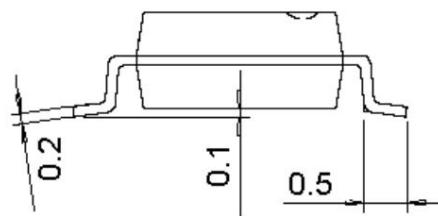
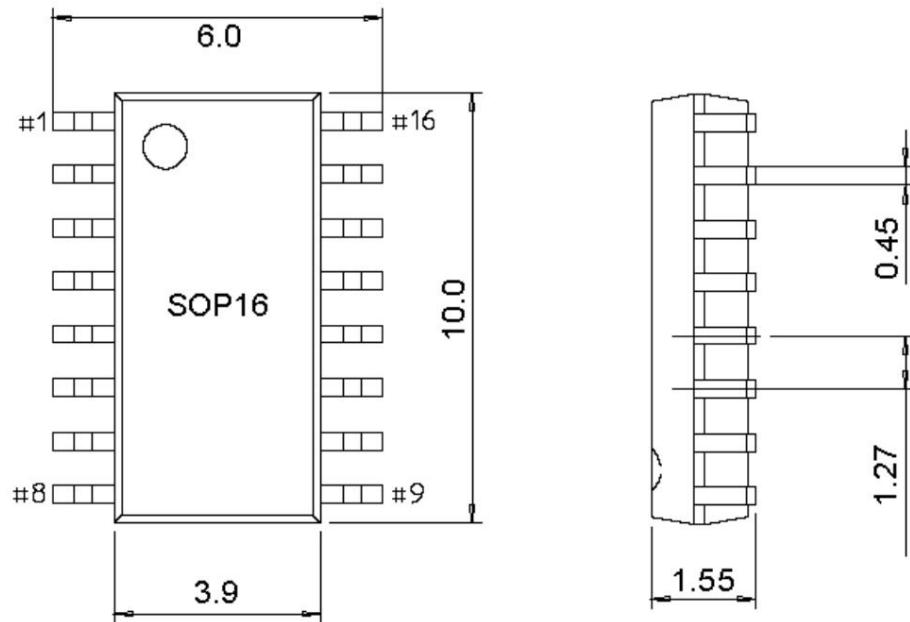
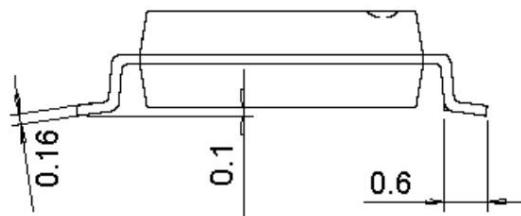
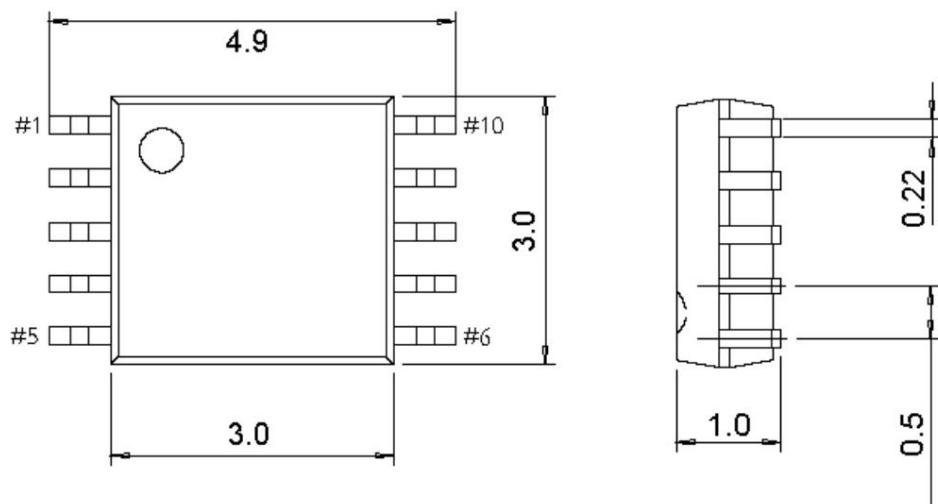
## 19. Package size

### 19.1 TSSOP20



### 19.2 QFN16-3\*3



**19.3 SOP16-150mil****19.4 MSOP10**

**20. Modification Record**

Version	date	illustrate
V1.0	2016.12.20	First edition released
V1.1	2017.09.12	<b>The highest system frequency is adjusted to 24MHz, updated 8.2, 18.4</b>
V1.2	2017.12.16	Added CH552/CH551 difference table in overview and modified some table headers
V1.3	2018.03.20	1. The CH552/1 distinction table in the overview has been modified. Table 18.4 has been modified. 5.3 Stack Pointer (SP) typo correction, 6.2 Add Data Flash suggestion
V1.4	2018.08.28	<b>Updated Fosc27 in 18.4 to</b>
V1.5	2019.06.17	add QFN16 package, updated 3, 4, and added Chapter 19 Package Dimensions
V1.6	2022.01.05	Remind that no external resistor should be connected in series with the USB pin. Optimize the bit clearing expression: directly write 0 to clear or write 1 to the corresponding bit of the register to clear
V1.7	2023.05.11	<b>Tip: Use CH54X chip for new design (supports 12-bit ADC and 3.3V programming).</b> Reminder: System main frequency and FLASH programming are related to power supply voltage, fine-tune parameters
V1.8	2024.04.19 New design	uses CH543, adjusts the internal clock frequency and the system main frequency adaptation voltage