Nandan U

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LinkedIn | GitHub | Instagram

SKILLS

Programming: Verilog, VHDL, SystemVerilog, C, C++, Python
EDA Tools: ModelSim, Cadence Virtuoso, LTspice, EDA Playground, MultiSIM, MATLAB, Keil µVision, Scilab, CST Studio
Technical: RTL, UVM, DFT, IoT, ASIC, FPGA, Embedded C
Concepts: Digital Electronics, MOS, Circuit Design, Architecture
Creative Exploratory: Content Creation, Video Editing, Public Speaking, Exploring New Technologies

EDUCATION

B.E. – ECE
VVIET, Mysuru — 2021–2025
CGPA: 8.73 — 82.93%

PUC – PCMB
Daksha PU College, Mysuru
2019–2021 — 89.66%

SSLC
Sri Vasavi Vidya Kendra, Kollegala
2018–2019 — 86.40%

CERTIFICATIONS

VLSI Design Engineer – Rooman Technology [link]
VLSI Design Engineer – Skill India, ESSCI, NSDC, PMKVY [link]
Life Skills (Jeevan Kaushal) 2.0 – Wadhwani Foundation [link]
Embedded – NIELIT [link]
Cybersecurity – Infosys [link]
Python – NIELIT [link]
UVM + RTL – IEEE CASS [link]
ML using Python – NIELIT [link]
MATLAB – NIELIT [link]

LANGUAGES

English, Kannada, Telugu, Hindi

ACHIEVEMENTS

- Runner-up – Project Expo (IEEE MCE ComSoc Chapter)
- Papers published – NCSSPES IJCRT, 2024 [link]

LEADERSHIP

- Coordinator – "Master of Drones" Hackathon (IEEE Bangalore Section), July 2024

EXPERIENCE

Intern – VLSI Design Engineer (Skill India, ESSCI)
Issued by: VVIET Mysuru — Duration: 780 Hours
Oct 2024 - May 2025
[Skill India] [Romon Technology] [Report]

- Certified by Electronics Sector Skills Council of India (ESSCI) under NSDC – Skill India
- Gained hands-on training in VLSI design, simulation, verification, and tool usage
- Evaluated at NSQF Level 5 with Grade B; included RTL, physical design, and DFT concepts

Intern – ORGANIZATION FOR THE DEVELOPMENT OF PEOPLE (ODP), Mysuru
Nov – Dec 2023
[Report] [Certificate] [Activities @ ODP]

- Delivered seminars on cancer awareness
- Observed sustainable and microfinance models

PROJECTS

ECOMATIC – Automated Robot for Cleaning Surroundings and Waste Collection with Segregation
IoT, Embedded
[Report] [KSCST] [Images-Project]

- Waste Collection with Segregation Robot
- Image + weight sensor-based classification
- KSCST Funding

8-bit Magnitude Comparator
[Report]

- Designed in Verilog, verified in UVM
- GDS-II generated using OpenROAD

Helical Antenna for CubeSat

- Designed 2.45 GHz RF antenna using CST
- Published in IJCRT
  [Certificate-IJCRT] [REPORT-IJCRT]

Dielectric Antenna for 5G

- 15 GHz high-gain DRA (10.4 dBi)
- Optimized bandwidth, published in IJCRT
  [Certificate-IJCRT] [REPORT-IJCRT]

FlexiHand Assist Glove

- Motion-sensing prosthetic glove
- Real-time feedback to caregivers
  [Report-Certificate]