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EE461 - Digital Design and HDL
Quiz #1

1. **Cmos switch implementation**

```verilog
`timescale 1ns / 1ps

module mux4to1(
    input wire X0, X1, X2, X3,  // Input signals
    input wire S0, S1,        // Select lines
    output wire out           // Output
);

    wire notS0, notS1;
    wire w0, w1, w2, w3;

    // NOT gates for the select lines
    not (notS0, S0);
    not (notS1, S1);

    // Transmission gates (mux logic)
    and (w0, X0, notS1, notS0);  // Select X0
    and (w1, X1, notS1, S0);     // Select X1
    and (w2, X2, S1, notS0);     // Select X2
    and (w3, X3, S1, S0);        // Select X3

    // OR gate to combine all the paths
    or (out, w0, w1, w2, w3);

endmodule
```

Testbench

```verilog
`timescale 1ns / 1ps

module testbench();

    reg X0, X1, X2, X3;  // Input signals
    reg S0, S1;          // Select lines
    wire out;            // Output wire
```

```verilog
// Instantiate the 4-to-1 MUX
mux4to1 uut (
    .X0(X0), .X1(X1), .X2(X2), .X3(X3),
    .S0(S0), .S1(S1),
    .out(out)
);

// Generate the waveform file
initial begin
    $dumpfile("dump.vcd");
    $dumpvars(0, testbench);

    // Test case 1
    S1 = 0; S0 = 0; X0 = 1; X1 = 0; X2 = 0; X3 = 0; #10;
    $display("At time %dns, S1 = %b, S0 = %b, X0 = %b, X1 = %b, X2 = %b, X3 =
%b, Out = %b",
            $time, S1, S0, X0, X1, X2, X3, out);

    // Test case 2
    S1 = 0; S0 = 0; X0 = 0; X1 = 1; X2 = 0; X3 = 0; #10;
    $display("At time %dns, S1 = %b, S0 = %b, X0 = %b, X1 = %b, X2 = %b, X3 =
%b, Out = %b",
            $time, S1, S0, X0, X1, X2, X3, out);

    // Test case 3
    S1 = 0; S0 = 1; X0 = 0; X1 = 1; X2 = 0; X3 = 0; #10;
    $display("At time %dns, S1 = %b, S0 = %b, X0 = %b, X1 = %b, X2 = %b, X3 =
%b, Out = %b",
            $time, S1, S0, X0, X1, X2, X3, out);

    // Test case 4
    S1 = 0; S0 = 1; X0 = 0; X1 = 0; X2 = 1; X3 = 0; #10;
    $display("At time %dns, S1 = %b, S0 = %b, X0 = %b, X1 = %b, X2 = %b, X3 =
%b, Out = %b",
            $time, S1, S0, X0, X1, X2, X3, out);

    // Test case 5
    S1 = 1; S0 = 0; X0 = 0; X1 = 0; X2 = 1; X3 = 0; #10;
```

```verilog
    $display("At time %dns, S1 = %b, S0 = %b, X0 = %b, X1 = %b, X2 = %b, X3 =
%b, Out = %b",
        $time, S1, S0, X0, X1, X2, X3, out);

    // Test case 6
    S1 = 1; S0 = 0; X0 = 0; X1 = 0; X2 = 0; X3 = 1; #10;
    $display("At time %dns, S1 = %b, S0 = %b, X0 = %b, X1 = %b, X2 = %b, X3 =
%b, Out = %b",
        $time, S1, S0, X0, X1, X2, X3, out);

    // Test case 7
    S1 = 1; S0 = 1; X0 = 0; X1 = 0; X2 = 0; X3 = 1; #10;
    $display("At time %dns, S1 = %b, S0 = %b, X0 = %b, X1 = %b, X2 = %b, X3 =
%b, Out = %b",
        $time, S1, S0, X0, X1, X2, X3, out);

    #10 $finish;
  end

endmodule
```

Results

VCD info: dumpfile dump.vcd opened for output.
At time   10ns, S1 = 0, S0 = 0, X0 = 1, X1 = 0, X2 = 0, X3 = 0,
Out = 1
At time   20ns, S1 = 0, S0 = 0, X0 = 0, X1 = 1, X2 = 0, X3 = 0,
Out = 0
At time   30ns, S1 = 0, S0 = 1, X0 = 0, X1 = 1, X2 = 0, X3 = 0,
Out = 1
At time   40ns, S1 = 0, S0 = 1, X0 = 0, X1 = 0, X2 = 1, X3 = 0,
Out = 0
At time   50ns, S1 = 1, S0 = 0, X0 = 0, X1 = 0, X2 = 1, X3 = 0,
Out = 1
At time   60ns, S1 = 1, S0 = 0, X0 = 0, X1 = 0, X2 = 0, X3 = 1,
Out = 0
At time   70ns, S1 = 1, S0 = 1, X0 = 0, X1 = 0, X2 = 0, X3 = 1,
Out = 1
testbench.sv:56: $finish called at 80000 (1ps)
Done