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Week#6 "if/case/casex/casez" Conditional Statements

1. **"if" Conditional Statements**

   Module ifTest

```verilog
module IfTest();
   reg [3:0] X;
   reg [3:0] Y;

   initial begin
      X = 4'b101x;
      Y = 4'b101z;

      if(X === 4'b101z) begin
         $display("Statement 1 has been selected!");
      end

      if(X === Y) begin
         $display("Statement 2 has been selected!");
      end

      if(X !== Y) begin
         $display("Statement 3 has been selected!");
      end

      if(X === X) begin
         $display("Statement 4 has been selected!");
      end

      $display("No one has been selected!");
   end
endmodule
```

   Module Testbench

```verilog
module IfTest_tb;
   // Instantiate the module under test
   IfTest iftest_instance();
```

```
initial begin
    // Run the simulation
    #10; // Wait a few time units to observe output
    $finish; // End the simulation
end
endmodule
```

<u>Results</u>

```
Statement 3 has been selected!
Statement 4 has been selected!
No one has been selected!
testbench.sv:8: $finish called at 10 (1s)
```

2. Continuous Assignment with Conditional Operator

<u>Module condOp</u>

```
module CondOp();
    reg [3:0] X;
    reg [3:0] Y;
    wire Z;

    assign Z = (X == Y) ? 1'b1 : 1'b0;

    initial begin
        X = 4'b101x;
        Y = 4'b101z;
        $monitor("Z's value: %d", Z);
    end
endmodule
```

<u>Module testbench</u>

```
module CondOp_tb;
    // Instantiate the module under test
    CondOp condop_instance();

    initial begin
        #10; // Allow time for simulation to observe Z's value
        $finish; // End the simulation
    end
endmodule
```

Results

```
Z's value: x
testbench.sv:7: $finish called at 10 (1s)
```
Done

3. Case conditional statement

Module caseTest
```
module caseTest();
    reg [3:0] X;

    initial begin
        X = 4'b101x;

        case(X)
            4'b1010: $display("Statement 1 has been selected!");
            4'b101x: $display("Statement 2 has been selected!");
            4'b101z: $display("Statement 3 has been selected!");
            4'bxxxx: $display("Statement 4 has been selected!");
            4'bzzzz: $display("Statement 5 has been selected!");
            default: $display("Default has been selected!");
        endcase
    end
endmodule
```

Module testbench
```
module caseTest_tb;
    // Instantiate the module under test
    caseTest case_test_instance();

    initial begin
        #10; // Wait to observe which statement is selected
        $finish; // End the simulation
    end
endmodule
```

Results

```
Statement 2 has been selected!
design.sv:24: $finish called at 10 (1s)
```
Done

4. "casex" Conditional Statement

Module casexTest

```
module casexTest();
    reg [3:0] X;

    initial begin
        X = 4'b101x;

        casex(X)
            4'b100z: $display("Statement 1 has been selected!");
            4'b10xx: $display("Statement 2 has been selected!");
            4'b11xz: $display("Statement 3 has been selected!");
            4'bxxxx: $display("Statement 4 has been selected!");
            4'bzzzz: $display("Statement 5 has been selected!");
            default: $display("Default has been selected!");
        endcase
    end
endmodule
```

Module testbench

```
module casexTest_tb;
    // Instantiate the module under test
    casexTest casex_test_instance();

    initial begin
        #10; // Allow time for simulation
        $finish; // End the simulation
    end
endmodule
```

Result

```
[2024-11-10 03:15:54 UTC] iverilog '-Wall' '-g2012' design.sv testbench.sv  &&
unbuffer vvp a.out
Statement 2 has been selected!
design.sv:24: $finish called at 10 (1s)
Done
```

5. "casez" Conditional Statement

Module casezTest

```
module casezTest();
    reg [3:0] X;
```

```verilog
    initial begin
        X = 4'b1x00;

        casez(X)
            4'b100z: $display("Statement 1 has been selected!");
            4'b10xx: $display("Statement 2 has been selected!");
            4'b11xz: $display("Statement 3 has been selected!");
            4'bxxxx: $display("Statement 4 has been selected!");
            4'b0zzz: $display("Statement 5 has been selected!");
            default: $display("Default has been selected!");
        endcase
    end
endmodule
```

Module testbench

```verilog
module casezTest_tb;
    // Instantiate the module under test
    casezTest casez_test_instance();

    initial begin
        #10; // Wait for simulation
        $finish; // End simulation
    end
endmodule
```

Result

```
[2024-11-10 03:20:33 UTC] iverilog '-Wall' '-g2012' design.sv testbench.sv  &&
unbuffer vvp a.out
Default has been selected!
design.sv:24: $finish called at 10 (1s)
Done
```