R-type

|  |  |  |  |
| --- | --- | --- | --- |
| Opcode 5bits(15:11) | rs 3bits(10:8) | rt 3bits(7:5) | rd 5bits(4:0) |

I-type

|  |  |  |  |
| --- | --- | --- | --- |
| Opcode 5bits(15:11) | rs 3bits(10:8) | rt 3bits(7:5) | Immediate num 5bits(4:0) |

J-type

|  |  |  |
| --- | --- | --- |
| Opcode 5bits(15:11) | Unuse 6bits(10:5) | Immediate num 5bits(4:0) |

1. Please explain the format of each instruction (including the format of this instruction and its operation codes, and other information if needed).

|  |  |
| --- | --- |
| li r1 n | 00000 xxx rrr iiiii  ALUControl:0000  RegDst:0  RegWrite:1  ALUSrc:1  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:0 |
| Add r1 r2 r3 | 00001 r2r2r2 r3r3r3 00r1r1r1  ALUControl:0001  RegDst:1  RegWrite:1  ALUSrc:0  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:0 |
| and r1 r2 r3 | 00010 r2r2r2 r3r3r3 00r1r1r1  ALUControl:0010  RegDst:1  RegWrite:1  ALUSrc:1  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:0 |
| or r1 r2 r3 | 00011 r2r2r2 r3r3r3 00r1r1r1  ALUControl:0011  RegDst:1  RegWrite:1  ALUSrc:1  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:0 |
| Neg r1 r2 | 00100 r2r2r2 r1r1r1 xxxxx  ALUcontrol:0100  RegDst:0  RegWrite:1  ALUSrc:0  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:0 |
| Load r1 r2 | 00101 r2r2r2 r1r1r1 xxxxx  ALUcontrol:1001  RegDst:0  RegWrite:1  ALUSrc:0  Branch:0  MemRead:1  MenWrite:0  MemtoReg:1  Li:1  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:0 |
| store r1 r2 | 00110 r2r2r2 r1r1r1 xxxxx  ALUcontrol:1001  RegDst:0  RegWrite:1  ALUSrc:0  Branch:0  MemRead:0  MenWrite:1  MemtoReg:0  Li:1  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:0 |
| move r1 r2 | 00111 r2r2r2 r1r1r1 xxxxx  ALUcontrol:1001  RegDst:0  RegWrite:1  ALUSrc:0  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:0 |
| addi r1 r2 n | 01000 r2r2r2 r1r1r1 iiiii  ALUcontrol:0001  RegDst:0  RegWrite:1  ALUSrc:1  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:0 |
| andi r1 r2 n | 01001 r2r2r2 r1r1r1 iiiii  ALUcontrol:0010  RegDst:0  RegWrite:1  ALUSrc:1  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:0 |
| ori r1 r2 n | 01010 r2r2r2 r1r1r1 iiiii  ALUcontrol:0011  RegDst:0  RegWrite:1  ALUSrc:1  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:0 |
| ble r1 r2 n | 01011 r1r1r1 r2r2r2 iiiii  ALUcontrol:0101  RegDst:0  RegWrite:1  ALUSrc:1  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:0 |
| slt r1 r2 r3 | 01100 r2r2r2 r3r3r3 00r1r1r1  ALUcontrol:0110  RegDst:1  RegWrite:1  ALUSrc:0  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:0 |
| lsl r1 r2 r3 | 01101 r2r2r2 r3r3r3 00r1r1r1  ALUcontrol:0111  RegDst:1  RegWrite:1  ALUSrc:0  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:0 |
| lsr r1 r2 r3 | 01110 r2r2r2 r3r3r3 00r1r1r1  ALUcontrol:1000  RegDst:1  RegWrite:1  ALUSrc:0  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:0  Enjump:0 |
| jump n | 01111 xxxxxx iiiii  ALUcontrol:xxxx  RegWrite:0  ALUSrc:0  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:1 |
| call n | 10000 xxxxxx iiiii  ALUcontrol:xxxx  RegWrite:0  ALUSrc:0  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:1  Read$ra:0  EnReboot:0  Enjump:1 |
| rtn | 10001 xxxxxxxxxx  ALUcontrol:xxxx  RegWrite:0  ALUSrc:0  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:0  Read$ra:1  EnReboot:0  Enjump:0 |
| reboot | 10010 xxxxxxxxxxx  RegWrite:0  ALUSrc:0  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:1  Write$ra:0  Read$ra:0  EnReboot:1  Enjump:0 |
| halt | 10011 xxxxxxxxxxx  RegWrite:0  ALUSrc:0  Branch:0  MemRead:0  MenWrite:0  MemtoReg:0  Li:0  Write$ra:0  Read$ra:0  EnReboot:0  Enjump:0 |

1. Fill the following tables with the machine codes of each instruction of the testing programs:

**Test program 1:**

|  |  |  |
| --- | --- | --- |
| instruction | machine code (binary) | machine code (hex) |
| li $r1, 1 | 00000 xxx rrr iiiii  00000 000 000 00001 | 0001 |
| li $r2, 2 | 00000 xxx rrr iiiii  00000 000 001 00010 | 0022 |
| li $r3, 10 | 00000 000 010 01010 | 004A |
| add $r2, $r1, $r2 | 00001 r2r2r2 r3r3r3 00r1r1r1  00001 000 001 00001 | 0821 |
| ble $r2, $r3, -1 | 01011 r1r1r1 r2r2r2 iiiii  01011 001 010 11111 | 595F |
| slt $r4, $r3, $r2 | 01100 r2r2r2 r3r3r3 00r1r1r1  01100 010 001 00011 | 6223 |
| halt | 10011 xxxxxxxxxxxx  10011 00000000000 | 9800 |

**Test program 2:**

|  |  |  |
| --- | --- | --- |
| instruction | machine code (binary) | machine code (hex) |
| li $r1, 3 | 00000 xxx rrr iiiii  00000 000 000 00011 | 0003 |
| li $r2, 5 | 00000 000 001 00101 | 0025 |
| andi $r3, $r1, 3 | 01001 r2r2r2 r1r1r1 iiiii  01001 000 010 00011 | 4843 |
| ori $r4, $r3, 8 | 01010 r2r2r2 r1r1r1 iiiii  01010 010 011 01000 | 5268 |
| neg $r5, $r4 | 00100 r2r2r2 r1r1r1 xxxxx  00100 011 100 00000 | 2380 |
| lsl $r6, $r5, $r1 | 01101 r2r2r2 r3r3r3 00r1r1r1  01101 100 000 00101 | 6C05 |
| lsr $r7, $r5, $r2 | 01110 r2r2r2 r3r3r3 00r1r1r1  01110 100 001 00110 | 7426 |
| halt | 10011 00000000000 | 9800 |

**Test program 3:**

|  |  |  |
| --- | --- | --- |
| instruction | machine code (binary) | machine code (hex) |
| li $r1, 6 | 00000 xxx rrr iiiii  00000 000 000 00110 | 0006 |
| li $r2, 5 | 00000 000 001 00101 | 0025 |
| and $r3, $r1, $r2 | 00010 r2r2r2 r3r3r3 00r1r1r1  00010 000 001 00010 | 1022 |
| li $r8, 0 | 00000 000 111 00000 | 00E0 |
| store $r3, $r8 | 00110 r2r2r2 r1r1r1 xxxxx  00110 111 010 00000 | 3740 |
| or $r4, $r1, $r2 | 00011 r2r2r2 r3r3r3 00r1r1r1  00011 000 001 00011 | 1823 |
| li $r8, 1 | 00000 000 111 00001 | 00E1 |
| store $r4, $r8 | 00110 111 011 00000 | 3760 |
| li $r8, 1 | 00000 000 111 00001 | 00E1 |
| load $r7, $r8 | 00101 r2r2r2 r1r1r1 xxxxx  00101 111 110 00000 | 2FC0 |
| reboot | 10010 xxxxxxxxxx  10010 0000000000 | 9000 |
| halt | 10011 00000000000 | 9800 |

**Test program 4:**

|  |  |  |
| --- | --- | --- |
| instruction | machine code (binary) | machine code (hex) |
| li $r1, 6 | 00000 000 000 00110 | 0006 |
| li $r2, 4 | 00000 000 001 00100 | 0024 |
| call 7 | 10000 xxxxxx iiiii  10000 000000 00111 | 8007 |
| move $r4, $r3 | 00111 r2r2r2 r1r1r1 xxxxx  00111 010 011 00000 | 3A60 |
| li $r1, 7 | 00000 000 000 00111 | 0007 |
| li $r2, 8 | 00000 000 001 01000 | 0028 |
| call 3 | 10000 000000 00011 | 8003 |
| move $r5, $r3 | 00111 010 100 00000 | 3A80 |
| jump 3 | 01111 xxxxxx iiiii  01111 000000 00011 | 7803 |
| add $r3, $r1, $r2 | 00001 r2r2r2 r3r3r3 00r1r1r1  00001 000 001 00010 | 0822 |
| rtn | 10001 xxxxxxxxxx  10001 00000000000 | 8800 |
| halt | 10011 00000000000 | 9800 |