TC APPLIED TECHNOLOGIES

TCD2210/2220(-E)

Digital Interface Communications Engine

Hardware Guide

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Chapter 1 About DICE TCD22xx

DICE 22xx family of chips contains the following members:

- **TCD2220** Full version with dual audio port, this chip is in a LQFP 144 package. This chip is also known as **DICE JR**

- **TCD2210** Reduced version with one audio port, this chip is in a QFP 128 package. This chip is also known as **DICE Mini.**

Both devices are in a **LEAD FREE** package and are **RHOS** compliant.

Ordering information

ID	RHOS	Temp.	Package
TCD2210	√	0 **°C** to 70 **°C**	QFP 128
TCD2210-E	√	-40 **°C** to 85 **°C**	QFP 128
TCD2220	√	-0 **°C** to 70 **°C**	LQFP 144
TCD2220-E	√	-40 **°C** to 85 **°C**	LQFP 144

Table 1: Ordering Information

1.1 Introduction

The TCD22xx chip family covers a wide range of audio applications, professional as well as consumer. Apart from its IEEE1394 audio streaming capability the chip features all common digital audio interfaces and a 50MHz 32 bit RISC processor including a wide range of peripherals. The DICE cross bar router allows any audio sink to connect to any audio source on a per channel basis. The IEEE1394 streaming engine can handle a total of 32 input channels and 32 output channels distributed on several isochronous channels.

1.2 Block Diagram

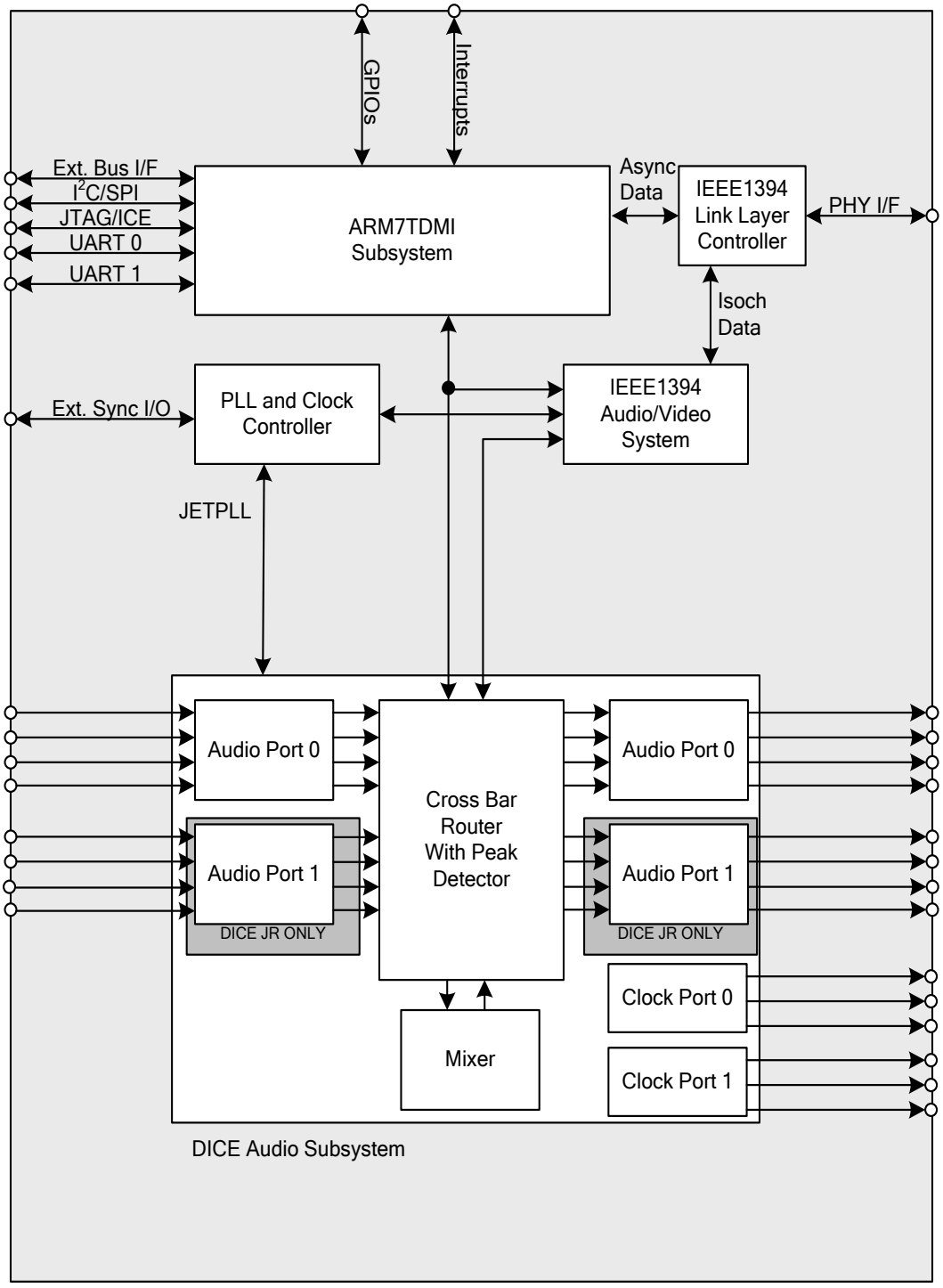


Figure 1: DICE 22xx Block Diagram

1.3 Chip Features

CPU core

- Full 32-bit ARM7TDMI RISC processor
- 32-bit internal bus
- 16-bit Thumb mode
- 16 Kb 0 wait state RAM
- 15 general-purpose 32-bit registers
- 32-bit program counter and status register
- 5 supervisor modes, 1 user mode
- External Bus Interface (EBI)
- Remap of Internal RAM during boot.

I2C Interface

- Standard and Full Speed support
- Slave mode with address match logic
- Master Mode
- 10 bit and 7 bit addressing mode
- 16 deep FIFO buffer

SPI Interface

- Master and Slave mode
- GPIO used for Slave Select
- Interrupt on Byte transfer complete

Dual Timer Unit

- 32 bit counter
- Free running and user-defined count
- Interrupt on counter wrap
- Clocked by CPU clock

Watch Dog

Dual Universal Asynchronous Receiver Transmitter (UART)

- Industry standard 16550 Compliant
- 16 deep receive and transmit FIFOs
- Supports all standard RS232 Rates
- Supports MIDI rate

General Purpose Input Output (GPIO)

- 15 individual ports

- Each port configurable as input or output
- Each port configurable for level or edge sensitive interrupts
- Configurable deglitching logic for each port

Dual Rotary Encoder Interface (Gray Decoder)

- individual rotary encoder counters
- 8 bit signed counter per port
- Configurable interrupt on value change

IEEE 1394 Link Layer Controller (LLC)

- IEEE 1394a compliant LLC
- Compliant PHY interface
- Support for isolation barrier
- 512x32 FIFO for asynchronous communication

Digital Interface Communication Engine (DICE)

- **Jet™ PLL**
- Cross-bar router with peak detector.
- 2 (1) generic audio port.
  - 4 x 2 ch. of I2S Per port (32KHz to 192KHz)
  - 4 x 4 ch. of I4S per port (32KHz to 192KHz)
  - 2 x 8 ch. of I8S per port (32KHz to 96KHz)
  - 4 x 2 ch. of AES, port 1 or port 2 (32KHz to 192KHz)
  - 2 x 8 ch. of ADAT, port 1 only (8 ch. @96KHz, 4 ch @ 192KHz)
- ARM Audio Receiver/Transmitter, 8 channels (4 ch @ 192KHz)
- IEC 61883-6 Isoc. Receiver, 32 channels (16 ch @ 192KHz)
- IEC 61883-6 Isoc. Transmitter, 32 channels (16 ch @ 192KHz)

Power and operating voltage

- 950 mW maximum, 500 mW typical (TBD)
- 3.3 volts - I/O
- 1.8 volts – core

1.4 Package

Product TCD2220 is only available in LQFP144 package. Product TCD2210 is only available in QFP128 package. Both packages are LEAD FREE:

Dimensions in Millimeters

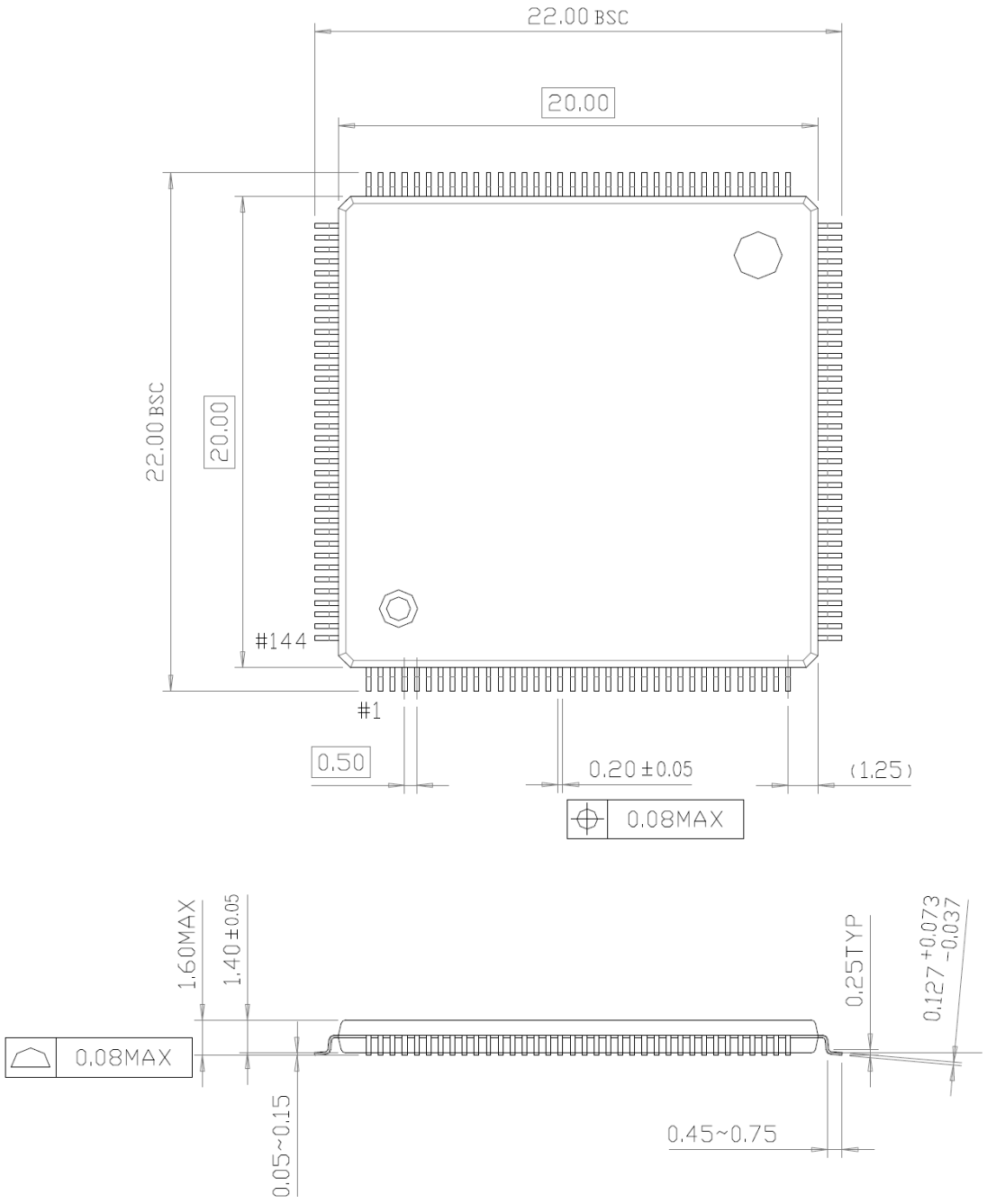
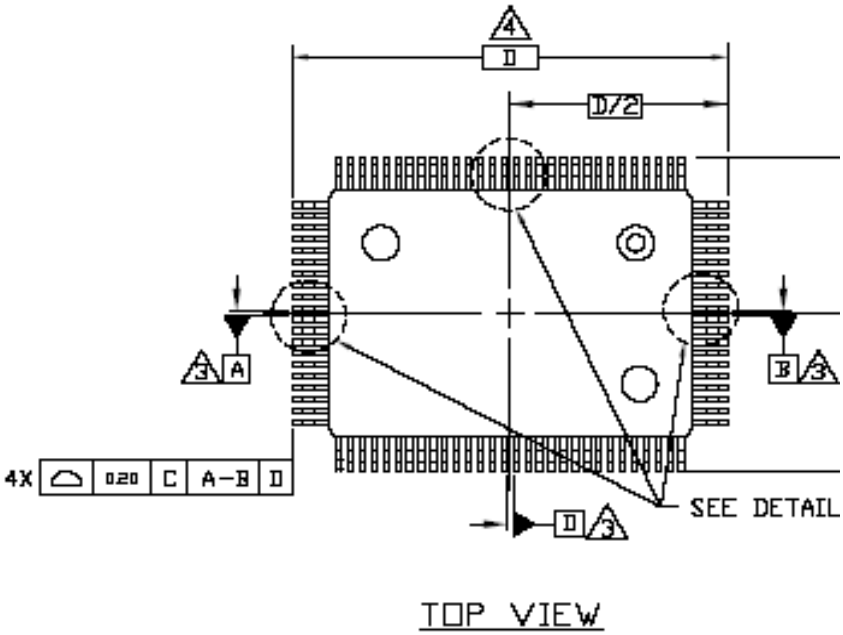
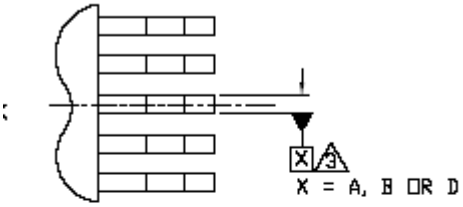


Figure 2: TCD2220, LQFP144 Dimensions

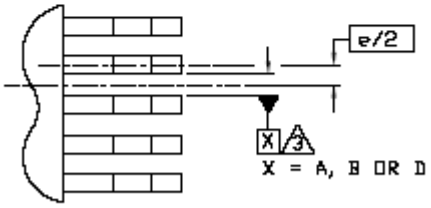


TOP VIEW

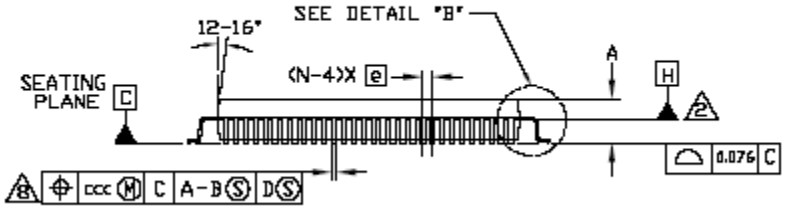
ODD LEAD SIDES

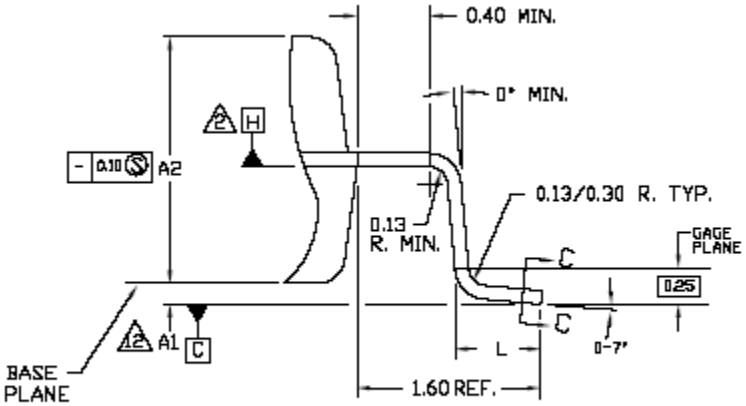


EVEN LEAD SIDES

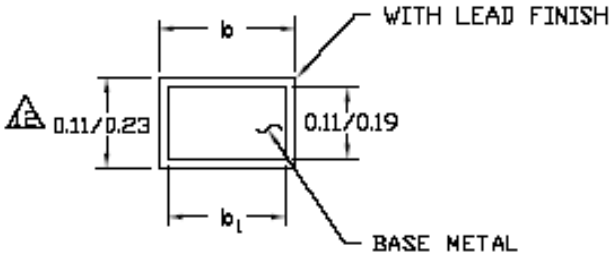


DETAIL "A"





DETAIL "B"



SECTION C-C

Figure 3: TCD2210, QFP128 Dimensions

Symbol	Variations ALL DIMENTIONS IN MILLIMITERS			
	MIN	NOM	MAX	Note
A		3.04	3.40	
A_1	0.25	0.33		
A_2	2.57	2.70	2.87	
D		23.20 BASIC		4
D_1		20.00 BASIC		5
D_2		18.5 REF.		
Z_D		0.75 REF.		
E		17.20 BASIC		4
E_1		14.00 BASIC		5
E_2		12.5 REF.		
Z_E		0.75 REF.		
L	0.73	0.88	1.03	
N		128		6
e		0.50 BSC		
b	0.13		0.28	8
b_1	0.13	0.20	0.25	
ccc		0.12		
N_D		38		
N_E		26		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5-1994.
2. DATUM PLANE H LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS A-B AND D TO BE DETERMINED WHERE CENTERLINE BETWEEN LEADS EXITS PLASTIC BODY AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H .
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.

8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
9. ALL DIMENSIONS ARE IN MILLIMETERS.
10. THIS DRAWING CONFORMS TO JEDEC REGISTERED OUTLINE MS-022.
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PKG. FAMILY IS 0.635 MM.
12. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.

1.5 Signal Description

The following table lists each I/O signal for the TCD2210 and TCD2220. Note that the chips use a number of shared pins, whereby each shared pin can be configured to contain different signals. The GPCSR module is used to configure the shared pins for a particular signal. The shared pins and their multiple functions are also listed in a table that follows the table below. Note that all the shared pins are bi-directional.

Pins that not available in TCD2210 (QFP128) are marked as N/A in the following table.

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
Data Bus					
D0	144	1	I/O (S[1])	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU[2],5V[3])
D1	1	2	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D2	2	3	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D3	3	4	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D4	4	5	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D5	5	6	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D6	6	7	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D7	7	8	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D8	8	9	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D9	9	10	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static

[1] S indicates Schmitt Trigger Input

[2] PU indicates that internal Pull-Up resistor is present on PAD

[3] 5V indicates that the input is 5V tolerant

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
					memory. (PU,5V)
D10	10	11	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D11	13	14	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D12	14	15	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D13	15	16	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D14	16	17	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D15	17	18	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
Address Bus					
A0	18	19	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A1	19	20	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A2	20	21	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A3	21	22	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A4	22	23	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A5	23	24	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A6	26	27	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A7	27	28	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A8	28	29	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A9	29	30	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A10	30	31	O	8	Address Bus. Shared address pins

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
					for SDRAM and Static memory.
A11	31	32	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A12	32	33	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A13	33	34	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A14	34	35	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A15	35	36	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A16	36	37	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A17	37	38	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A18	38	39	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A19	39	40	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
Chip Selects					
CS0*	136	121	O	4	Shared SDRAM and Static Memory Chip Selects
CS1*	46	45	O	4	Shared SDRAM and Static Memory Chip Selects
CS2*	138 (shared)	123 (shared)	O	6	Shared SDRAM and Static Memory Chip Selects
CS3*	139 (shared)	124 (shared)	O	6	Shared SDRAM and Static Memory Chip Selects
Grey Code Rotary Encoder					
EN1_A	138 (shared)	123 (shared)	I (S)	6	Rotary Encoder Input (5V)
EN1_B	139 (shared)	124 (shared)	I (S)	6	Rotary Encoder Input (5V)
EN2_A	65 (shared)	N/A	I (S)	6	Rotary Encoder Input (5V)
EN2_B	66 (shared)	N/A	I (S)	6	Rotary Encoder Input (5V)
General Purpose I/O					
GPIO0	42 (shared)	N/A	I/O (S)	6	General Purpose I/O (5V)
GPIO1	138 (shared)	123 (shared)	I/O (S)	6	General Purpose I/O (5V)

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
GPIO2	139 (shared)	124 (shared)	I/O (S)	6	General Purpose I/O (5V)
GPIO3	137 (shared)	122 (shared)	I/O (S)	6	General Purpose I/O (5V)
GPIO4	85 (shared)	78 (shared)	I/O (S)	6	General Purpose I/O (5V)
GPIO5	86 (shared)	79 (shared)	I/O (S)	6	General Purpose I/O (5V)
GPIO6	117 (shared)	106 (shared)	I/O (S)	6	General Purpose I/O (5V)
GPIO7	118 (shared)	107 (shared)	I/O (S)	6	General Purpose I/O (5V)
GPIO8	119 (shared)	108 (shared)	I/O (S)	6	General Purpose I/O (5V)
GPIO9	55	N/A	I/O (S)	6	General Purpose I/O (5V)
GPIO10	56	N/A	I/O (S)	6	General Purpose I/O (5V)
GPIO11	57 (shared)	N/A	I/O (S)	6	General Purpose I/O (5V)
GPIO12	65 (shared)	N/A	I/O (S)	6	General Purpose I/O (5V)
GPIO13	66 (shared)	N/A	I/O (S)	6	General Purpose I/O (5V)
GPIO14	67 (shared)	N/A	I/O (S)	6	General Purpose I/O (5V)
RAM Clock					
CLKO	40	41	O	8	SDRAM Interface AHB Bus Clock (Z[4])
SDRAM Dedicated Signals					
CLKE	42 (shared)	N/A	O	6	SDRAM Interface Clock Enable
RAS*	41	42	O	8	SDRAM Interface Row Address Strobe
CAS*	44	43	O	8	SDRAM Interface Column Address Strobe
SDRAM_WE	45	44	O	8	SDRAM Interface Write Enable
SDRAM_DQM0	47	46	O	8	SDRAM Interface Lower byte mask
SDRAM_DQM1	48	47	O	8	SDRAM Interface Upper byte mask
SDRAM_BNK0	52	51	O	8	SDRAM Interface Bank Address
SDRAM_BNK1	53	52	O	8	SDRAM Interface Bank Address
SDRAM_A10	43	N/A	O	8	SDRAM Precharge A10
SRAM Interface					

[4] Z indicates that the output is Z-stateable

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
SRAM_READY	137(shared)	122 (shared)	I	6	SRAM ready (5V)
SRAM_BS[0]	140	125	O	4	SRAM lower byte select
SRAM_BS[1]	141	126	O	4	SRAM upper byte select
SRAM_WE*	142	127	O	8	SRAM write enable
SRAM_OE*	143	128	O	8	SRAM output enable
Phy Interface					
SCLK	54	53	I (S)	-	49.152MHz PHY Clock input (5V)
PHD0	58	54	I/O (S)	8	PHY tristatable data line bit 0
PHD1	59	55	I/O (S)	8	PHY tristatable data line bit 1
PHD2	60	56	I/O (S)	8	PHY tristatable data line bit 2
PHD3	63	59	I/O (S)	8	PHY tristatable data line bit 3
PHD4	64	60	I/O (S)	8	PHY tristatable data line bit 4
PHD5	68	61	I/O (S)	8	PHY tristatable data line bit 5
PHD6	69	62	I/O (S)	8	PHY tristatable data line bit 6
PHD7	70	63	I/O (S)	8	PHY tristatable data line bit 7
PHCT0	71	64	I/O (S)	8	PHY tristatable control line bit 0
PHCT1	72	65	I/O (S)	8	PHY tristatable control line bit 1
PHDI	73	66	I (S)	-	A high indicates isolation barrier is not present (PU, 5V)
PHLR	74	67	O	8	Serial request output from S-LINK (Z)
PHLP	75	68	O	4	Link power status. Pulsing if isolation barrier present
PHLO	76	69	I (S)	-	Link on indication from PHY. Pulsing when asserted (PU, 5V)
Word Clock					
WCLK_IN0	85 (shared)	77 (shared)	I (S)		Word Clock In (5V)
WCLK_IN1	65 (shared)	N/A	I (S)		Word Clock In (5V)
WCLK_OUT0	86 (shared)	79 (shared)	O	6	Word Clock Out
WCLK_OUT1	66 (shared)	N/A	O	6	Word Clock Out
External Sample Clocks					
EXT_FBR	85 (shared)	78 (shared)	I/O (S)	6	External 1fs base rate clock (5V) (Can be used for WCKI)

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
EXT_512BR	86 (shared)	79(shared)	I/O (S)	6	External 512 x base rate clock (5V)
Audio Port 0					
DO0_0	122	111	O	2	Audio port 0 data out 0
DO0_1	123	112	O	2	Audio port 0 data out 1
DO0_2	124	113	O	2	Audio port 0 data out 2
DO0_3	125	114	O	2	Audio port 0 data out 3
DI0_0	109	102	I	-	Audio port 0 data in 0 (5V)
DI0_1	110	103	I	-	Audio port 0 data in 1 (5V)
DI0_2	111	104	I	-	Audio port 0 data in 2 (5V)
DI0_3	112	105	I	-	Audio port 0 data in 3 (5V)
Audio Port 1					
DO1_0	126	N/A	O	2	Audio port 1 data out 0
DO1_1	127	N/A	O	2	Audio port 1 data out 1
DO1_2	128	N/A	O	2	Audio port 1 data out 2
DO1_3	129	N/A	O	2	Audio port 1 data out 3
DI1_0	113	N/A	I	-	Audio port 1 data in 0 (PU, 5V)
DI1_1	114	N/A	I	-	Audio port 1 data in 1 (PU, 5V)
DI1_2	115	N/A	I	-	Audio port 1 data in 2 (PU, 5V)
DI1_3	116	N/A	I	-	Audio port 1 data in 3 (PU, 5V)
Audio Clock Ports					
MCK0	106	99	O	8	Master Clock 0
FCK0	107	100	O	8	Frame Clock 0 (LR Clock)
BCK0	108	101	O	8	Bit Clock 0
MCK1	117 (shared)	106 (shared)	O	6	Master Clock 1
FCK1	118 (shared)	107 (shared)	O	6	Frame Clock 1 (LR Clock)
BCK1	119 (shared)	108 (shared)	O	6	Bit Clock 1
XTAL					
XTAL2	102	95	O	-	XTAL for clock doubler/power manager/LLC
XTAL1	103	96	I	-	XTAL for clock doubler/power manager/LLC

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
Reset					
RESET*	79	72	I (S)	-	Reset – active low (PU, 5V)
PLL					
PLLE	51	50	I	-	PLL Enable (5V)
Test					
TEMO	77	70	I	-	Test mode pin (PD[5], 5V)
SCMO	78	71	I	-	Scan mode select: LO – boundary scan, HI - debug (PD, 5V)
JTAG Interface					
TMS	80	73	I	-	JTAG - Test mode select (PU, 5V)
TCK	81	74	I	-	JTAG - Test clock (5V)
TDI	82	75	I	-	JTAG - Test Data In (PU, 5V)
TDO	83	76	O	4	JTAG - Test Data Out (Z, 5V)
TRST*	84	77	I	-	JTAG – Test Reset (active low) (PD, 5V)
I2C Interface					
I2C_CLK	104 (shared)	97 (shared)	I/O (S)	6	I2C Clock (OD[6], 5V)
I2C_DATA	105 (shared)	98 (shared)	I/O (S)	6	I2C Data (OD, 5V)
SPI Interface					
SPIA_SS	138 (shared)	123 (shared)	I/O (S)	6	SPI Slave Select (5V)
SPIA_MISO	139 (shared)	124 (shared)	I/O (S)	6	SPI Master In, Slave Out (5V)
SPIA_MOSI	104 (shared)	97 (shared)	I/O (S)	6	SPI Master Out, Slave In (5V)
SPIA_CK	105 (shared)	98 (shared)	I/O (S)	6	SPI Clock (5V)
SPIB_SS	57 (shared)	N/A	I/O (S)	6	Alt. SPI Slave Select (5V)
SPIB_MISO	65 (shared)	N/A	I/O (S)	6	Alt. SPI Master. In, Slave Out (5V)
SPIB_MOSI	66 (shared)	N/A	I/O (S)	6	Alt. SPI Master. Out, Slave In (5V)
SPIB_CK	67 (shared)	N/A	I/O (S)	6	Alt. SPI Clock (5V)
UART Signals					

[5] PD indicates that internal Pull-Down resistor is present on pad.

[6] OD indicates Open Drain pad type. External Pull-Up resistor required.

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
UART0_TX	130	115	O	4	Serial output; active-high
UART0_RX	131	116	I	-	Serial input; active-high (5V)
UART1_TX	134	119	O	4	Serial output; active-high
UART1_RX	135	120	I	-	Serial input; active-high (5V)
Filters					
FILTER_AES	90	83	A	-	AES Receiver filter component connection
FILTER_CLK_DBL	95	88	A	-	Clock Doubler VCO filter component connection
FILTER_HPLL	98	91	A	-	Jet™ PLL filter component connection
PLL 1.8V					
PLL_1V8 (AES)	89	82	P	-	PLL 1.8 V
PLL_1V8 (CLK_DBL)	94	87	P	-	PLL 1.8 V
PLL_1V8 (HPLL)	99	92	P	-	PLL 1.8 V
PLL Bulk Bias					
PLL_BULK (CLK_DBL)	93	86	P	-	PLL Bulk Bias
PLL_BULK (HPLL)	97	90	P	-	PLL Bulk Bias
PLL Ground					
PLL_GND (AES)	91	84	P	-	PLL Ground
PLL_GND (CLK_DBL)	92	85	P	-	PLL Ground
PLL_GND (HPLL)	96	89	P	-	PLL Ground
Core 1.8V					
VDD1IH	24	25	P	-	Core 1.8 V
VDD1IH	61	57	P	-	Core 1.8 V
VDD1IH	100	93	P	-	Core 1.8 V
VDD1IH	132	117	P	-	Core 1.8 V
I/O 3.3V					
VDD3OP	11	12	P	-	I/O 3.3 V
VDD3OP	49	48	P	-	I/O 3.3 V

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
VDD3OP	87	80	P	-	I/O 3.3 V
VDD3OP	120	109	P	-	I/O 3.3 V
Core Ground					
VSS3I	25	26	P	-	Core Ground
VSS3I	62	58	P	-	Core Ground
VSS3I	101	94	P	-	Core Ground
VSS3I	133	118	P	-	Core Ground
I/O Ground					
VSS3OP	12	13	P	-	I/O Ground
VSS3OP	50	49	P	-	I/O Ground
VSS3OP	88	81	P	-	I/O Ground
VSS3OP	121	110	P	-	I/O Ground

Table 2: Signal Descriptions

1.5.1 Multi-function Pins

The following table lists all the multiple signal (shared) pins, along with the various signals assigned to each pin.

LQFP 144	QFP 128	Function 1		Function 2		Function 3		Function 4	
85	78	EXT_FBR	(I/O)	GPIO4	(I/O)	WCLK_IN0	(I)		
86	79	EXT_512BR	(I/O)	GPIO5	(I/O)	WCLK_OUT0	(O)		
104	97	I2C_CLK	(I/O)	SPIA_MOSI	(I/O)				
105	98	I2C_DATA	(I/O)	SPIA_CK	(I/O)				
117	106	MCK1	(I/O)	GPIO6	(I/O)				
118	107	FCK1	(I/O)	GPIO7	(I/O)				
119	108	BCK1	(O)	GPIO8	(I/O)				
137	122	SRAM_READY	(I)	GPIO3	(I/O)				
138	123	CS2*	(O)	GPIO1	(I/O)	EN1_A	(I)	SPIA_SS	(I/O)
139	124	CS3*	(O)	GPIO2	(I/O)	EN1_B	(I)	SPIA_MISO	(I/O)
42	N/A	CLKE	(O)	GPIO0	(I/O)				
57	N/A	SPIB_SS	(I/O)	GPIO11	(I/O)				
65	N/A	SPIB_MISO	(I/O)	GPIO12	(I/O)	EN2_A	(I)	WCLK_IN1	(I)
66	N/A	SPIB_MOSI	(I/O)	GPIO13	(I/O)	EN2_B	(I)	WCLK_OUT1	(O)
67	N/A	SPIB_CK	(I/O)	GPIO14	(I/O)				

Table 3: Shared Pins

1.5.2 TCD2220 Pins (not available on TCD2210)

Signal	TCD2220	I/O	Drive (mA)	Description
Data Bus				
EN2_A	65 (shared)	I (S)	6	Rotary Encoder Input (5V)
EN2_B	66 (shared)	I (S)	6	Rotary Encoder Input (5V)
General Purpose I/O				
GPIO0	42 (shared)	I/O (S)	6	General Purpose I/O (5V)
GPIO9	55	I/O (S)	6	General Purpose I/O (5V)
GPIO10	56	I/O (S)	6	General Purpose I/O (5V)

Signal	TCD2220	I/O	Drive (mA)	Description
GPIO11	57 (shared)	I/O (S)	6	General Purpose I/O (5V)
GPIO12	65 (shared)	I/O (S)	6	General Purpose I/O (5V)
GPIO13	66 (shared)	I/O (S)	6	General Purpose I/O (5V)
GPIO14	67 (shared)	I/O (S)	6	General Purpose I/O (5V)
SDRAM Dedicated Signals				
CLKE	42 (shared)	O	6	SDRAM Interface Clock Enable
SMPCHG	43	O	8	SDRAM Precharge A10
Word Clock				
WCLK_IN1	65 (shared)	I (S)	6	Word Clock In (5V), **Suggest using WCLK_IN0 as that is the default.**
WCLK_OUT1	66 (shared)	O	6	Word Clock Out, **Suggest using WCLK_IN0 as that is the default.**
Audio Port 1				
DO1_0	126	O	2	Audio port 1 data out 0
DO1_1	127	O	2	Audio port 1 data out 1
DO1_2	128	O	2	Audio port 1 data out 2
DO1_3	129	O	2	Audio port 1 data out 3
DI1_0	113	I	-	Audio port 1 data in 0
DI1_1	114	I	-	Audio port 1 data in 1
DI1_2	115	I	-	Audio port 1 data in 2
DI1_3	116	I	-	Audio port 1 data in 3
SPI Interface				**TCD2210 has alternative SPI Pins.**
SPIB_SS	57 (shared)	I/O (S)	6	Alt. SPI Slave Select
SPIB_MISO	65 (shared)	I/O (S)	6	Alt. SPI Master. In, Slave Out
SPIB_MOSI	66 (shared)	I/O (S)	6	Alt. SPI Master. Out, Slave In
SPIB_CK	67 (shared)	I/O (S)	6	Alt. SPI Clock

Table 4: TCD2220 Only

Chapter 2 Ground and Power supply

Extended copper planes must be used for the ground and power supplies.
Ground plane for each voltage domain should be separate and analog ground should be kept separate from digital to ensure PLL operation. We also recommend to use separate voltage regulator for 1.8V analog power supply for use by the three chip PLL's.
Designs should use an absolute minimum of 12 bypass capacitors (four 0.1 µF, four 10 nF and four 1 nF ceramic) for each VDD supply. More extensive bypassing may be required for some applications.
The capacitors should be placed as close to the package as possible, preferably on the bottom side of the board. The decoupling capacitors should be tied directly to the power and ground planes with vias that touch their solder pads. Surface-mount capacitors are recommended because of their lower series inductances (ESL) and higher series resonant frequency. Connect the power and ground planes to the TCD22xx pins directly with vias—do not use traces. The ground planes should not be densely perforated with vias or traces as this will reduce their effectiveness.
In addition, we recommend tantalum capacitors (or better) on the board to be used for decoupling.

Chapter 3 Crystal Oscillator

TCD22XX, like most digital chips, contains an on-board oscillator. The ARM7 RISC is clocked by this oscillator, as well as the other internal functions (DICE Router, start up state machines, etc.). The on-chip oscillator itself is not really an oscillator, but is an amplifier suitable for being used as the feedback amplifier in an oscillator circuit with off-chip components (crystal or ceramic resonator, resistors and capacitors). The figure below shows the typical connections to TCD22XX.

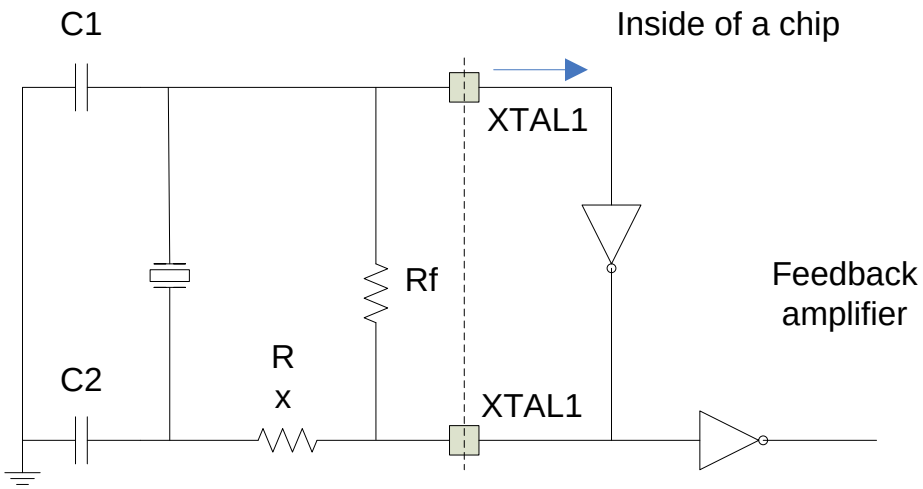


Figure 4: On-Chip oscillator typical connections

The tolerance of the crystal should be 100ppm or better if more precision is needed in customer application

The external components commonly used for the oscillator circuit are a positive reactance (normal crystal oscillator), two capacitors, C1 and C2 and two resistors, Rf and Rx.

3.1.1 Crystal Specifications

Specifications for an appropriate crystal are not very critical. Any fundamental mode crystal of medium or better quality can be used. Crystal resistance affects start-up time and steady state amplitude but can be compensated by the choice of C1 and C2, however, the lower the crystal resistance, the better. A discussion of external R and C components follows below.

3.1.1.1 Oscillation Frequency

The oscillation frequency is mainly determined by the crystal. To be able to support all possible applications of the chip, it is recommended to use bypass from 1394 PHY crystal. For non-1394 applications with no PHY recommended frequency is 24.576MHz. The on-chip oscillator has little effect on the frequency. The influence of the on-chip oscillator on frequency results from its input and output (pin-to-ground) capacitances which parallel C1 and C2, and the XTAL1-to- XTAL2 (pin-to-pin)

capacitance which parallels the crystal. The input and pin-topin capacitances are about 7pF each.

3.1.1.2 C1 and C2 Selection

Optimal values for C1 and C2 depend on whether a quartz crystal or ceramic resonator is used, and on application-specific requirements for start-up time and frequency tolerance. Start-up time is sometimes more critical in microcontroller systems than frequency stability because of various reset and initialization requirements. Accuracy of the oscillator frequency is less commonly critical, as when the oscillator is being used as a time base. As a general rule, fast start-up and stable frequency tend to pull the oscillator design in opposite directions. Considerations of both start-up time and frequency stability over temperature suggest that C1 and C2 should be about equal and at least 15pF (but they don't have to be either). Increasing the value of these capacitors above 40pF or 50pF improves frequency stability, but also increases the start-up time. If the capacitors are too large (several hundred pF), the oscillator won't start up at all.

3.1.1.3 Rf and Rx Selection

A large Rf (1M) holds the on-chip oscillator (a CMOS inverter) in its linear region allowing it to oscillate. The inverter has a fairly low output resistance which destabilizes the oscillator circuit. Rx size could be anywhere between 33Ohm and 100Ohm. This resistor is added to the feedback network, as shown in the **Figure 4**, to stabilize the oscillator circuit. At higher oscillator frequencies, a 20pF or 30pF capacitor is sometimes used in place of Rx to compensate for the internal propagation delay.

3.1.1.4 PCB CONSIDERATIONS

Noise glitches arising at XTAL1or XTAL2pins at the wrong time can cause a miscount in the internal clock-generating circuitry. These kinds of glitches can be produced through capacitive coupling between the oscillator components and PCB traces carrying digital signals with fast rise and fall times. For this reason, the oscillator components should be mounted close to the chip and have short, direct traces to the XTAL1, XTAL2, and V_{SS} pins. If possible, use dedicated V_{DD} and V_{SS} pins for the on-chip oscillator. In addition, surrounding oscillator components with "quiet" traces (V_{DD} and V_{SS}) will alleviate capacitive coupling to signals having fast edges. To minimize inductive coupling, the PCB layout should minimize lead, wire, and trace lengths for oscillator components.

For applications that have 1394 PHY on board, one crystal oscillator can be saved and XTAL1/XTAL2 pins can be fed directly from the PHY crystal. In this case the connection to the PHY crystal will look like the one on **Figure 5**. In this case the frequency used should be 24.576MHz. Also, XTAL2 (crystal output) should be left open

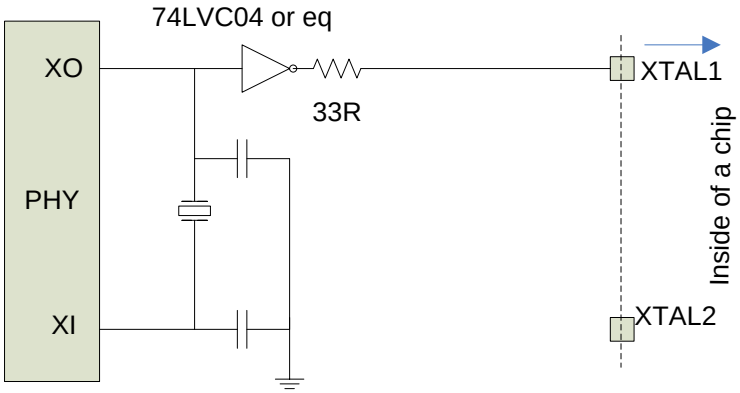


Figure 5: PHY crystal connection to TCD22xx

Chapter 4 Test and JTAG operation

TCD22xx JTAG interface could be used to implement boundary scan and to connect JTAG debugger for initial firmware development. **Table 5** holds the description of TCD22xx JTAG pins.

The general recommendation is to put an external pull-ups on TCK pin and to provide space for the JTAG connector on the board. **Figure 6** is a sample of JTAG connector schematics:

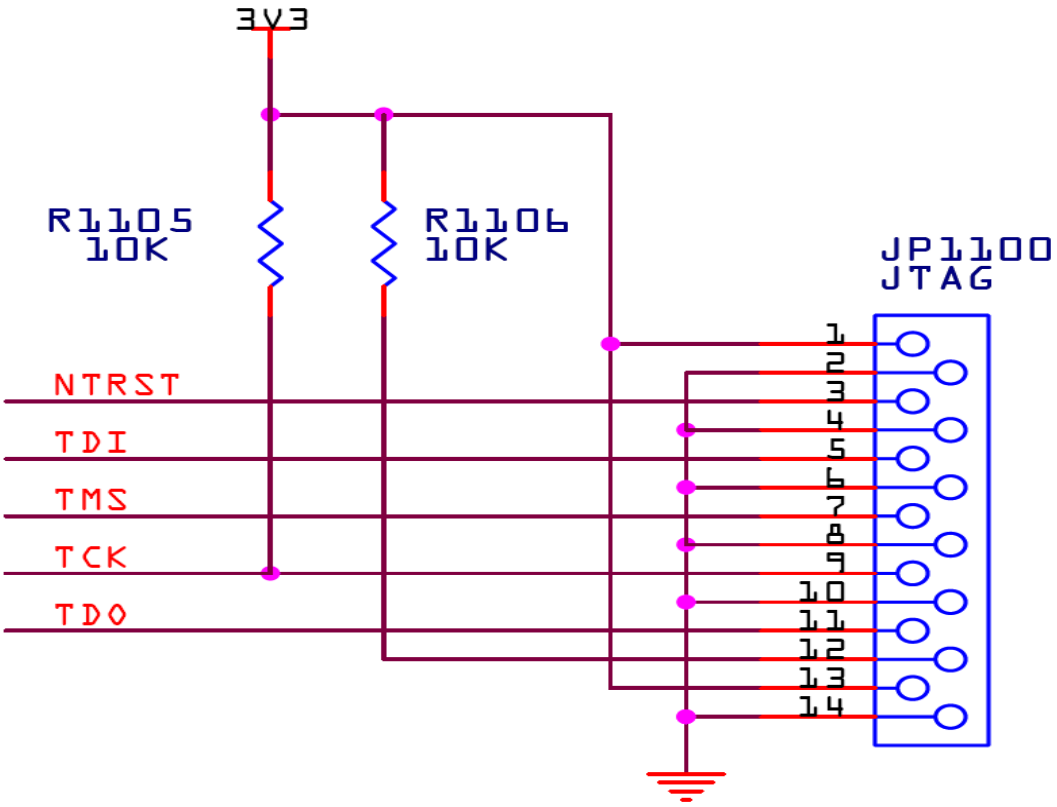


Figure 6: Sample of JTAG connection

Resistor R1106 is required by the specific connector and might not be needed if different JTAG hardware is used

Signal	TCD2220	TCD2210	I/O	Drive	Description
TEMO	77	70	I	-	Test mode pin (PD[7], 5V)
SCMO	78	71	I	-	Scan mode select: LO – boundary scan, HI - debug (PD, 5V)

Signal	TCD2220	TCD2210	I/O	Drive	Description
JTAG Interface					
TMS	80	73	I	-	JTAG - Test mode select (PU, 5V)
TCK	81	74	I	-	JTAG - Test clock (5V)
TDI	82	75	I	-	JTAG - Test Data In (PU, 5V)
TDO	83	76	O	4	JTAG - Test Data Out (Z, 5V)
TRST*	84	77	I	-	JTAG – Test Reset (active low) (PD, 5V)

Table 5: JTAG pin-out

Chapter 5 Memory Map and Interrupts

On chip processor (ARM7Tdmi) supports two memory maps distinguished by the value of Remap register. The Remap functionality is used during boot and normal operation. The ARM processor assumes that the exception vectors are placed from address 0x0000 0000 after reset and therefore it is essential that the external program memory (typically a flash) is mapped to this address after reset. In most applications it is necessary to be able to change exception vectors at runtime, and for that purpose the internal RAM can be mapped into the low address space. A reset will always force CS0 to be mapped to address 0x0000 0000. By writing a "1" to register 0xc0000008 in the Remap module the low portion of the address space can be replaced with the internal RAM. A shadow of the internal RAM will always be present at address 0x8000 0000 enabling the application to write to it before the remapping is done. The size of internal SRAM is 16KB; however, 16MB of address space is allocated to it. The address bits 14-24 are ignored when internal SRAM is accessed.

Note, that in regular DICE JR/Mini applications only boot mode is used. All applications run from SDRAM. ARM core remap function is only used for testing purposes and not recommended for the users. The SDRAM is mapped to location 0x0000 0000 by the boot code using a remap features in the memory controller and not using the ARM core remap function.

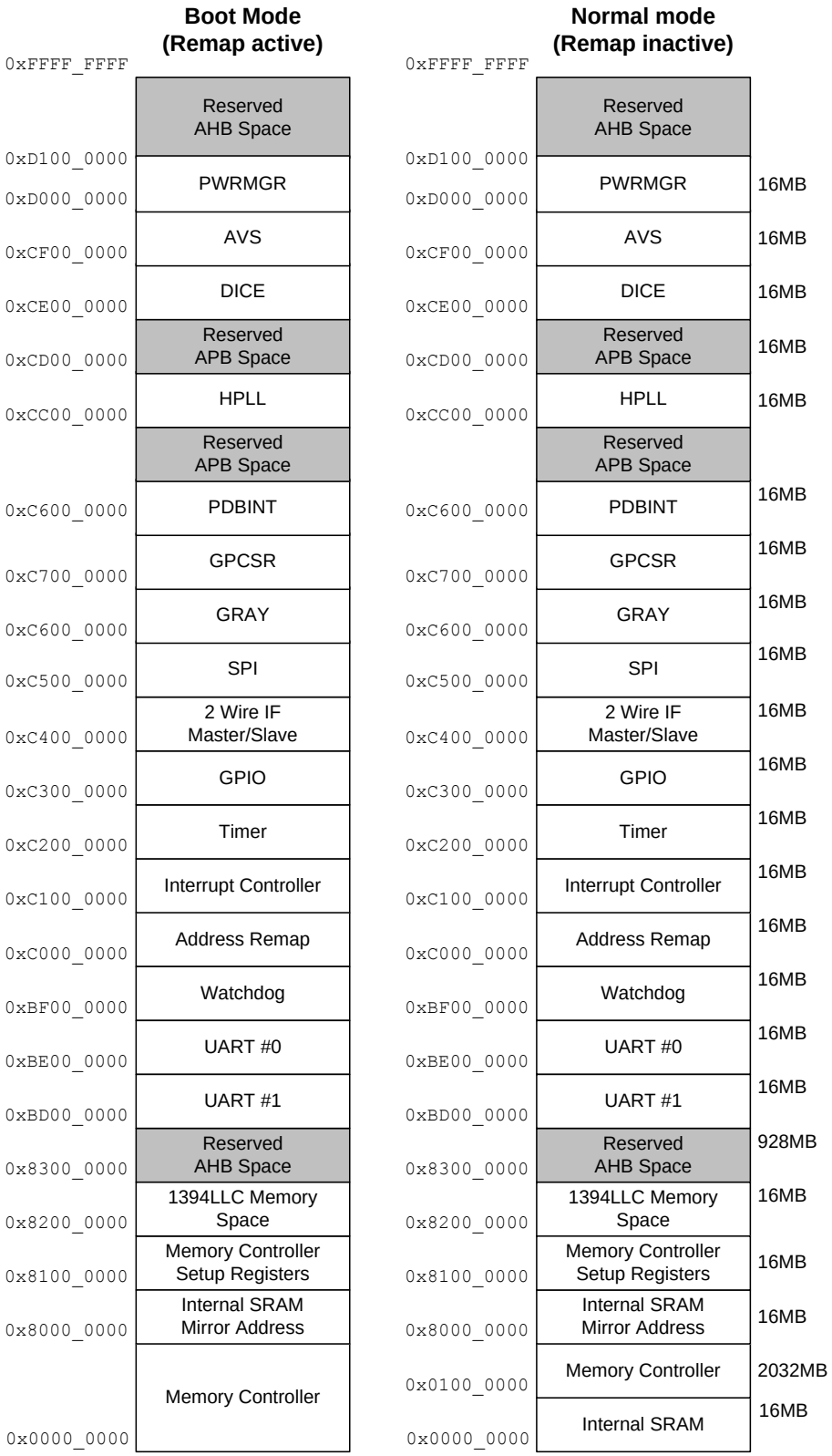


Figure 7: Global Memory Map (allocated address space)

Chapter 6 Reset circuitry

The TCD22xx chip receives its clock input from one or both of the following inputs XTAL1 pin from oscillator or SCLK from the 1394 PHY. The chip uses three on-chip PLLs to generate its internal clocks. Because the PLLs requires some time to achieve phase lock, XTAL1 and SCLK must be valid for a minimum time period during reset before the RESET signal can be de-asserted.

It is important that a TCD22xx chip have a reliable active RESET that is released once the power supplies and internal clock circuits have stabilized. The RESET signal should not only offer a suitable delay, but it should also have a clean monotonic edge.
External reset circuitry should be designed to hold system in reset enough time for the oscillator to settle down to a stable frequency and PLL to stabilize after the initial power surge. Recommended time is 0.2 s. Maximum rise time for reset signal should be one 50MHz clock (20ns).

Chapter 7 External Bus Interface

External memory is accessed via The External Bus Interface (EBI), a highly configurable generic memory interface supporting a wide variety of static and dynamic memories as well as memory mapped peripherals. The memory controller can be connected to 4 different memory devices at a time, with the choice of SDRAM, SRAM, FLASH or ROM for each. The memory type, size, addressing, and timing are all programmable. The data and address bus for both the SDRAM and static memories is shared between all the memories.

Below is a list of the main features:

- Memory interface Unit is clocked from the ARM system clock enabling 49.152MHz (typical) memory accesses.
- Support for 8 bit and 16 bit memories.
- Support for both SDRAM and static memory types
- 20 address bits (lsb addresses 16bit data word) and 16bit data on memory interface. Byte lane enables/masks are available for byte wide accesses into 16bit memory.
- Supports 4 chip selects. CS0 is dedicated to Boot FLASH. CS1 is traditionally connected to the SDRAM.
- Base address and block size for each chip select is configurable at runtime, except CS0 – it's base address is 0x0.
- ARM7TDmi and TCD22xx have a remap feature that allows mapping of the internal SRAM to address 0x0 at runtime. This feature is not recommended for the user.
- The memory map illustrated on the left of Figure 7 is the default after reset. The FLASH type access chosen as default for CS_0 is set-up using a very conservative timing. As CS_0 will have a default base address at 0x0000_0000 a 16bit FLASH/ROM or any similar for ARM SW booting should be mounted here.
- Chip select 2 and 3 (CS2-CS3) are by default programmed to have an alternative function as an input. If external memories or peripherals are connected to those pins, a pull-up should be added in order not to select those devices during boot. CS2 and CS3can be connected according to the specific requirements of a particular application to a SDRAM, SRAM, FLASH or ROM. Both chip select assignment and memory type timing characteristics for CS0/CS1/CS2/CS3 are runtime reconfigurable.
- TCD2220 has a dedicated SDRAM pre-charge pin. But due to historical reasons pre-charge is avoided through programming of the memory controller. So if user is planning to use the firmware application then this pin can be left dangling.

7.1.1 Signal Description

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
Data Bus					
D0	144	1	I/O (S[8])	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU[9],5V[10])
D1	1	2	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D2	2	3	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D3	3	4	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D4	4	5	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D5	5	6	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D6	6	7	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D7	7	8	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D8	8	9	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D9	9	10	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D10	10	11	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D11	13	14	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)

[8] S indicates Schmitt Trigger Input

[9] PU indicates that internal Pull-Up resistor is present on PAD

[10] 5V indicates that the input is 5V tolerant

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
D12	14	15	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D13	15	16	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D14	16	17	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
D15	17	18	I/O (S)	6	Data Bus. Shared read/write data for external SDRAM and Static memory. (PU,5V)
Address Bus					
A0	18	19	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A1	19	20	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A2	20	21	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A3	21	22	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A4	22	23	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A5	23	24	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A6	26	27	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A7	27	28	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A8	28	29	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A9	29	30	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A10	30	31	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A11	31	32	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A12	32	33	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A13	33	34	O	8	Address Bus. Shared address pins for SDRAM and Static memory.

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
A14	34	35	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A15	35	36	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A16	36	37	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A17	37	38	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A18	38	39	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
A19	39	40	O	8	Address Bus. Shared address pins for SDRAM and Static memory.
Chip Selects					
CS0*	136	121	O	4	BOOT chip select
CS1*	46	45	O	4	Shared SDRAM and Static Memory Chip Selects
CS2*	138 (shared)	123 (shared)	O	6	Shared SDRAM and Static Memory Chip Selects
CS3*	139 (shared)	124 (shared)	O	6	Shared SDRAM and Static Memory Chip Selects
RAM Clock					
CLKO	40	41	O	8	SDRAM Interface AHB Bus Clock (Z[11])
SDRAM Dedicated Signals					
CLKE	42 (shared)	N/A	O	6	SDRAM Interface Clock Enable
RAS*	41	42	O	8	SDRAM Interface Row Address Strobe
CAS*	44	43	O	8	SDRAM Interface Column Address Strobe
SDRAM_WE	45	44	O	8	SDRAM Interface Write Enable
SDRAM_DQM0	47	46	O	8	SDRAM Interface Lower byte mask
SDRAM_DQM1	48	47	O	8	SDRAM Interface Upper byte mask
SDRAM_BNK0	52	51	O	8	SDRAM Interface Bank Address
SDRAM_BNK1	53	52	O	8	SDRAM Interface Bank Address

[11] Z indicates that the output is Z-stateable

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
SDRAM_A10	43	N/A	O	8	SDRAM Precharge A10
SRAM Interface					
SRAM_READY	137(shared)	122 (shared)	I	6	SRAM ready (5V)
SRAM_BS[0]	140	125	O	4	SRAM lower byte select
SRAM_BS[1]	141	126	O	4	SRAM upper byte select
SRAM_WE*	142	127	O	8	SRAM write enable
SRAM_OE*	143	128	O	8	SRAM output enable

Table 6: External Bus interface

7.2 FLASH Memory access

7.2.1 Read Operation

In this document all timings are observed on the chip side. Access time (Tacc) is undefined as it depends on the type of FLASH used. By default TCD22xx firmware uses 15 wait states to access FLASH, but this number can be changed at runtime.

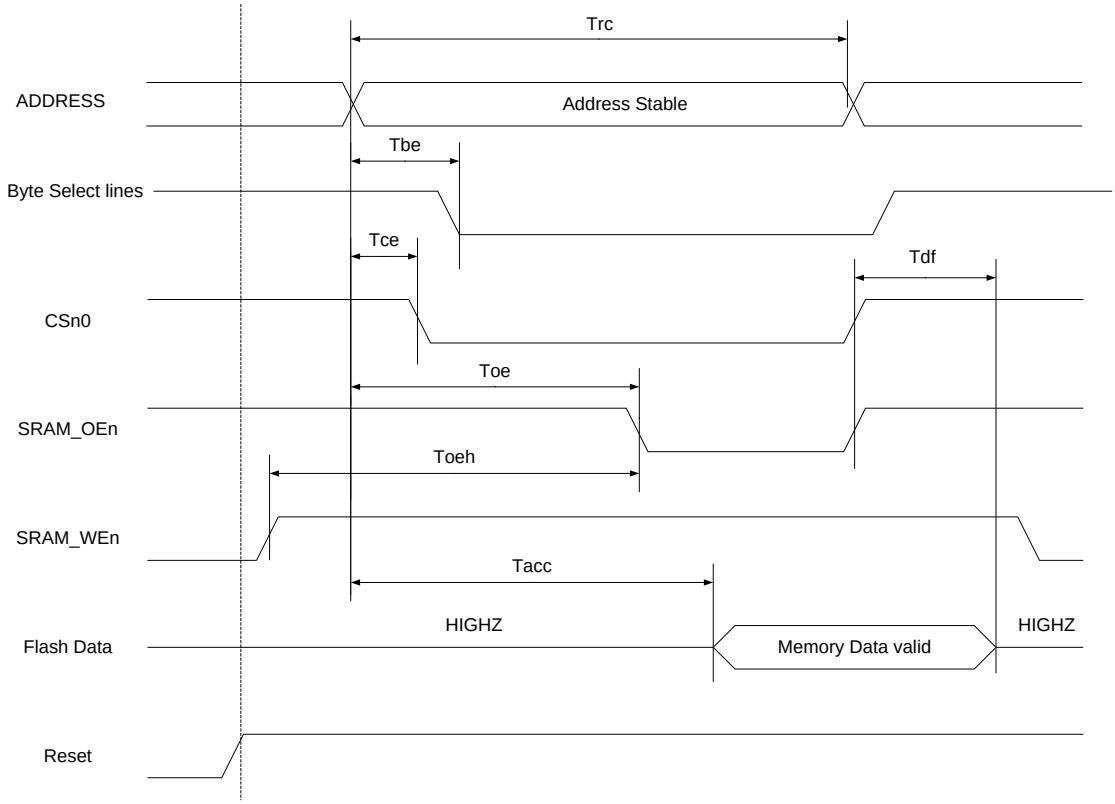


Figure 8: Flash Read

Timing const	Min	Max
Trc	20ns	320ns
Tbe (from address to byte selects)	1.55ns	8.49
Tce (from address to CSn0)	1.24ns	6.57ns
Toe (from address to OEn)	-0.27ns	2.63ns
Tdr (data stable before address changes)	14ns	-
Tdf(data hold after address invalid)	0ns	0ns

Table 7: Flash Read timing

7.2.2 Write Operation

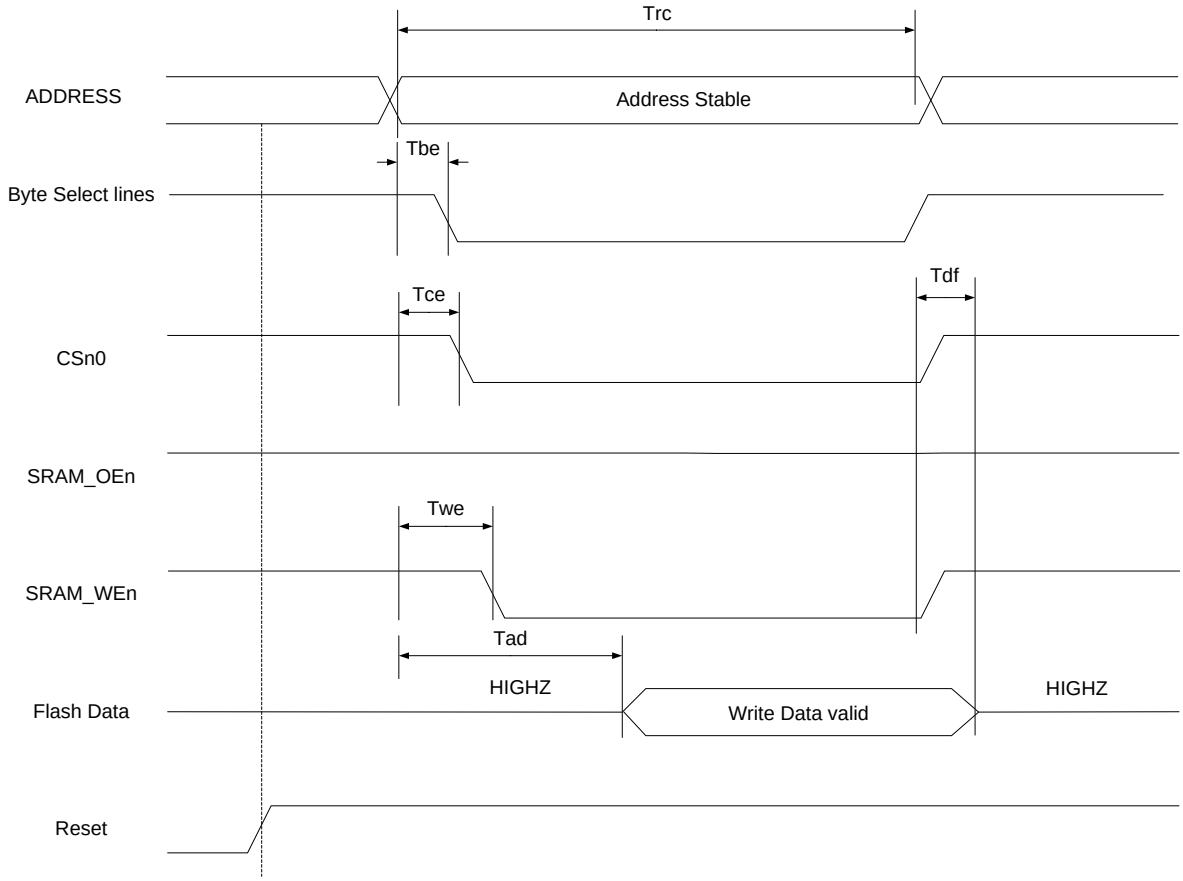


Figure 9: FLASH Write operation

Timing const	Min	Max
Trc	20ns	320ns
Tbe (from address to byte selects)	1.55ns	8.49
Tce (from address to CSn0)	1.24ns	5.79ns
Twe (from address to Wen)	-0.31ns	2.51ns

Tad (write data valid after address valid)	1.21ns	7.4ns
Tdf(data hold after address invalid)	0ns	0ns

Table 8: Flash write operation timing

7.2.3 Status Information

Some FLASH memories have a status pin that indicates the status of the internal state machine of the FLASH memory. TCD22xx does not have dedicated pins for the status inputs from the FLASH memories. However, you can connect the FLASH status pins to the GPIO pins of the chip and get the status information by reading corresponding bits in the GPIO register (see User Guide for further info).

7.2.4 Address bus interpretation

The address bus is automatically aligned depending on whether a 16 bit or 8 bit device is addressed. This means that if the controller is programmed for 16 bit, A0 should be connected to A0 of the device and not A1.

7.3 SDRAM Memory access

7.3.1 Read operation

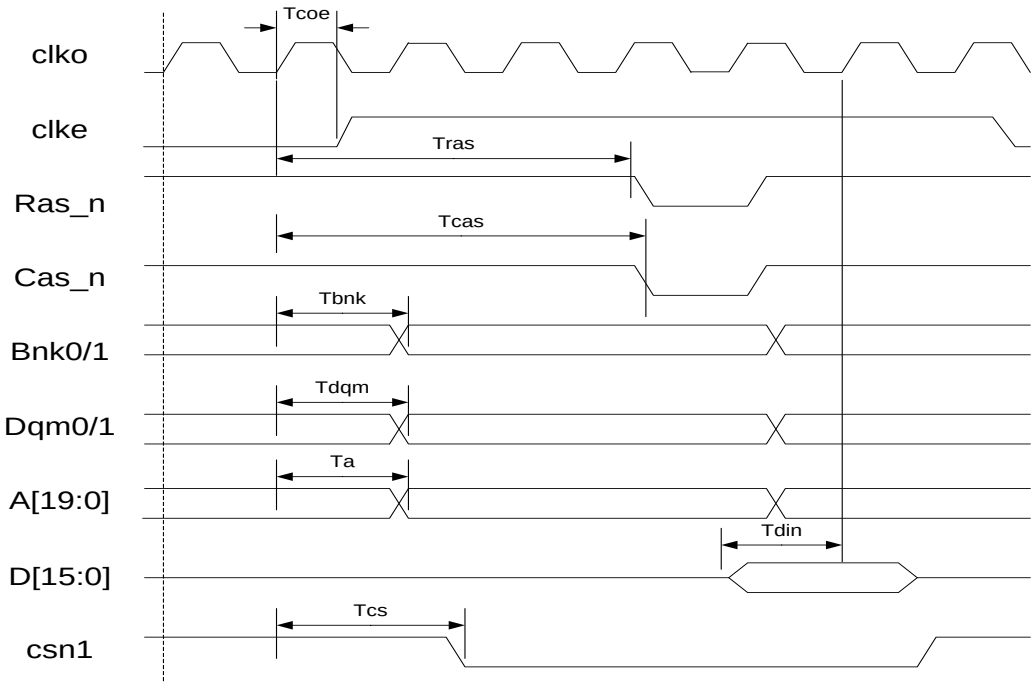


Figure 10: SDRAM read timing

Timing const	Min	Max
Tcoe(clko to clke)		2.24ns
Ta (clko to address)		3.37ns
Tras (clko to nras)		N wait states +0.43 ns
Tcas (clko to ncas)		N wait states + 0.36ns
Tbnk (clko to bnk0/1)		0.64ns
Tdqm (clko to dqm)		0.58ns
Tcs (clko to ncs1)		4.06ns
Tdin (din on chip input pins before rising edge of clko)	9.4ns	

Table 9: SDRAM read timing

7.3.2 Write Operation

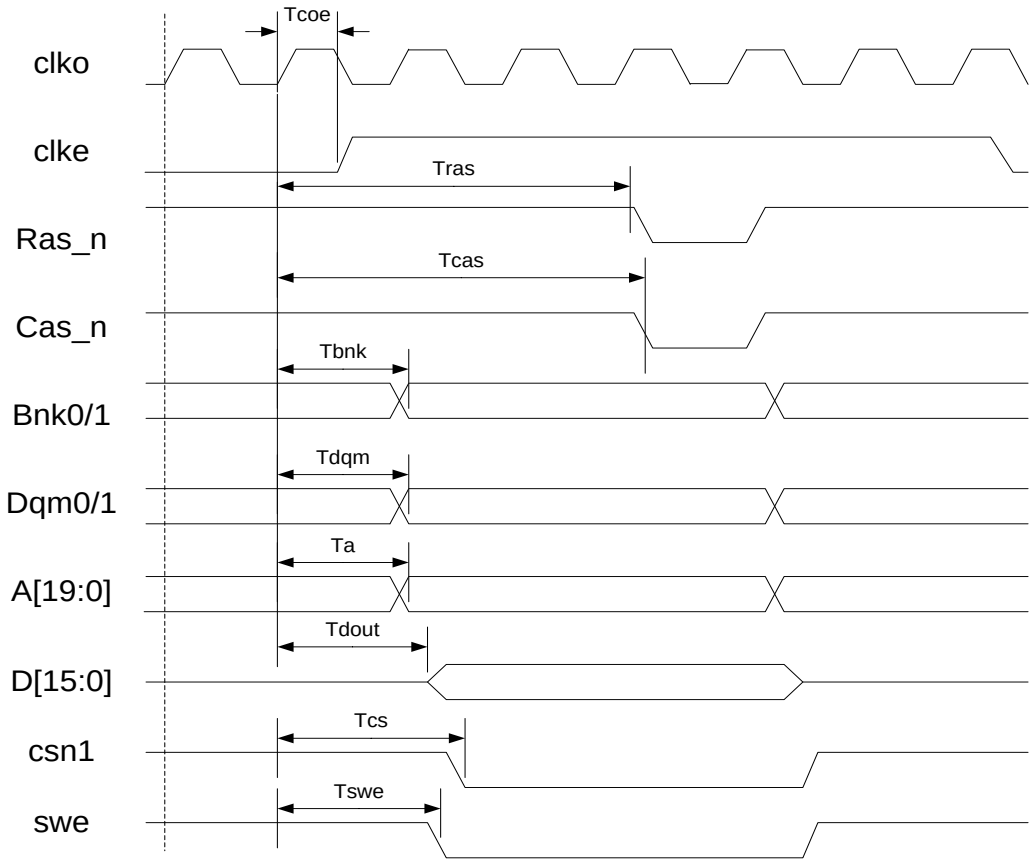


Figure 11: SDRAM Write timing

Timing const	Min	Max
Tdout (clko to data out)		5.12ns
Tswe		0.45ns

Table 10: SDRAM Write timing

7.3.3 Precharge timing

Timing const	Min	Max
T clko to precharge out		0.54ns

Table 11: SDRAM precharge timing

7.4 Interfacing to Non-Memory Devices with Ready Pin (DSP)

The Memory Controller supports non-memory devices with a ready pin, such as a DSP. This type of device has the same interface as an asynchronous SRAM, except that it has a ready pin to indicate that the read data is available on the data bus or that the write data is accepted by the device.

The ready pin of the device should be connected to the SRAM_READY pin on the DICEJR/Mini. Note that the SRAM_READY pin is a multi-function pin, so the SRAM_READY bit of the GPCSR_GPIO_SELECT register must be set to 1. If SRAM_READY is to be used it needs to be synced to the chip clock externally.

The READY_MODE bit of the Static Timing Register (SMTMGR_SET0/1/2 – bit 26) should be set to 1.

7.4.1 I/O Interface between Non-Memory Device and DICE JR/Mini

The following are conditions for interfacing Non-Memory device pins to the DICE JR/Mini Memory Controller pins:

- Address pins – Connect the address pins to the DICE JR/Mini SDRAM/SRAM shared address pins.
- Chip select pin – Connect the chip select pin to one of the chip select pins. Specify which chip select is connected to the Non-Memory device in the memory type bits (bits 6:5) of the mask register (SMSKR0-7) that correspond to a particular chip select.
- Output enable pin – Connect the output enable pin of the Non-Memory device to the SRAM_OE pin.
- Write enable pin – Connect the write enable pin of the Non-Memory device to the SRAM_WE pin.
- Byte control pins – Connect the byte enable pins to the SRAM_BS pins. The lower byte enable should be connected to SRAM_BS[0] and the upper byte enable should be connected to SRAM_BS[1]. This is only required if single byte writes are required on a 16 bit device.
- Data inputs/outputs – Drive the bidirectional data pins of the Non-Memory device using the DICE JR/Mini data bus pins.

Chapter 8 Audio ports

The DICE JR (2220) has 2 audio input ports and DICE Mini (2210) only has Port 0. Each port has 4 data lines. The ports can be routed to the INS receivers, AES receivers and ADAT receivers depending on the configuration setting. See AUDIO PORT register description in User Guide for specific settings.

The DICE JR (2220) has 2 audio input ports and DICE Mini (2210) only has Port 0. Each port has 4 data lines. The 4 data lines in each port can source from the corresponding InS, AES or ADAT interface. Only Port 0 can be configured for ADAT. See AUDIO PORT register description in User Guide for specific settings.

There are no specific recommendations for connection of the audio ports. To avoid ringing it might be feasible to add damping resistors to the audio data lines. The value would typically be in the range of 30Ohm-100Ohm depending on the trace length.

If audio ports are unused, then audio port data in lines should be grounded, and for TCD2220 where audio data in lines are muxed with GPIO it should be assured that they are not left floating either by programming them to be outputs right after boot or pulling them down using a resistor.

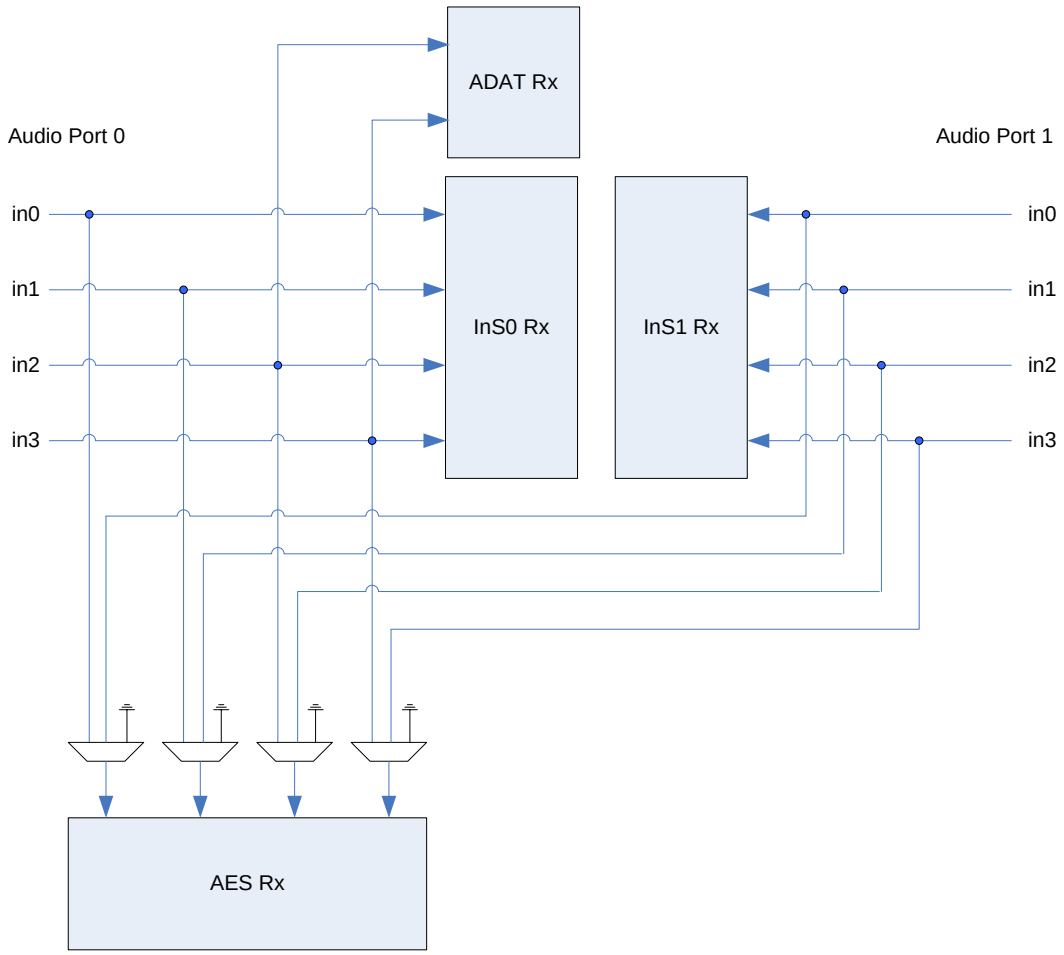


Figure 12: Audio Input Port connections

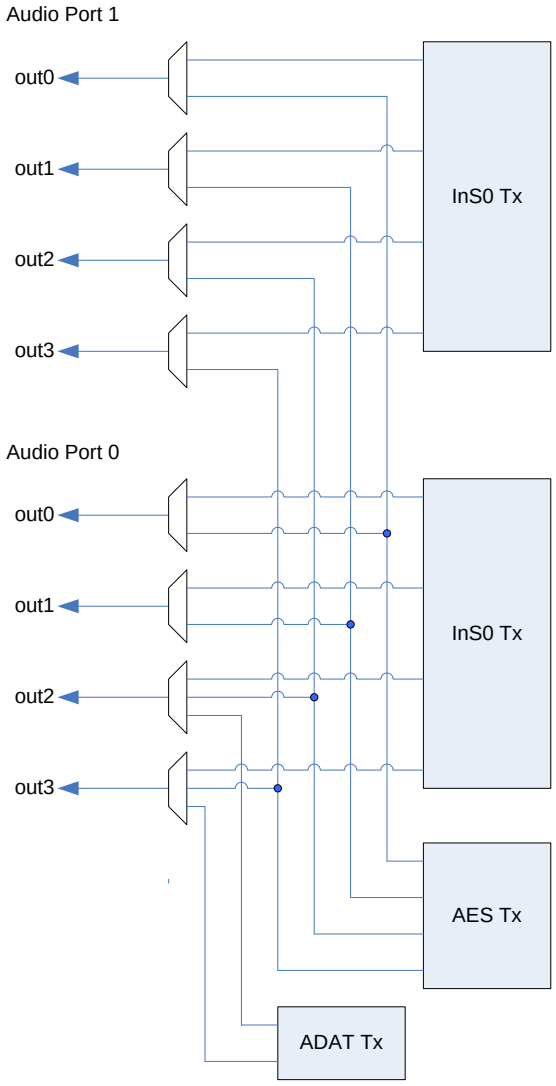


Figure 13: Audio Port Out connections

8.1 InS Interface

8.1.1 InS general description

InS is a highly configurable module that can be set to comply with a number of different formats, ensuring compatibility with most DAC's and SRC's as well as other serial audio devices. The TCD2220 contains two I^{n}S transmitter/receiver modules, the TCD2210 contains only one transmitter/receiver module. In all serial transactions trough InS TCD22xx is used as a master. There is no possibility to slave TCD22xx InS modules to external serial clocks.

The internal JET_PLL can however be slaved to an external clock so in that way the InS streams can be made synchronous to another system.

Each InS transmitter and receiver is build out of four transmitting or receiving blocks, thus allowing to receive/transmit up to 16 channels depending on configuration and system mode. For more information on configuration and programming of the InS interface please refer to Sections 5.6 & 5.7 of TCD22xx user Guide.

Timing is shown with non-inverted BCK, FCK and MCK. Timing is the same with inverted versions except for the change of edge.

8.1.2 InS Transmit timing

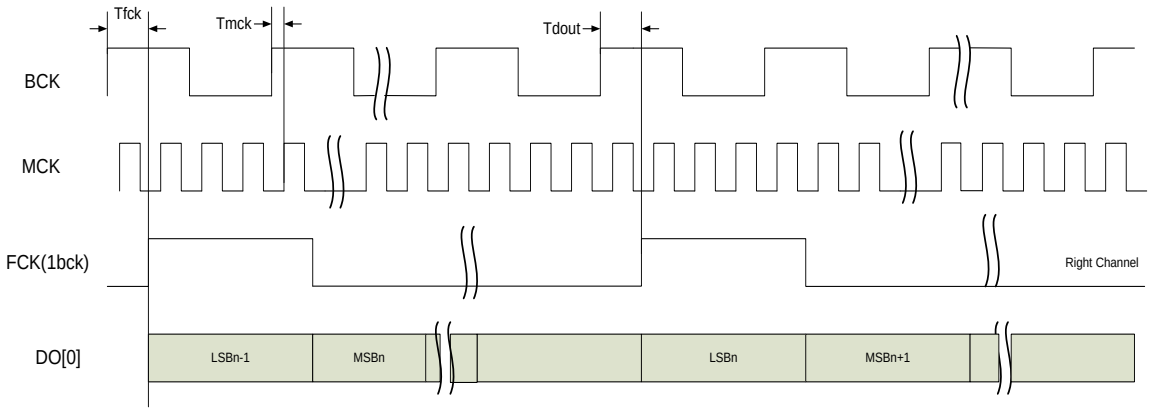


Figure 14: InS Timing Constants

Timing constant	Min	Max
Bck0 to Mck0 (Tmck)		0.48ns
Bck0 to Fck0 (Tfck)		4.68ns
Bck0 to Audio port 0/1 data out (Tdout)		4.81 ns
Bck1 to Mck1 (Tmck)		0.13ns

Timing constant	Min	Max
Bck1 to Fck1 (Tfck)		2.42ns
Bck1 to Audio port 0/1 data out (Tdout)		2.46ns

Table 12: InS Transmit timing

8.1.3 InS Receive timing

Audio port data in InS is sampled on the negative edge of the clock used in generating bit clock for the slaves connected to the InS bus, thus insuring proper reception of the data inside the chip.

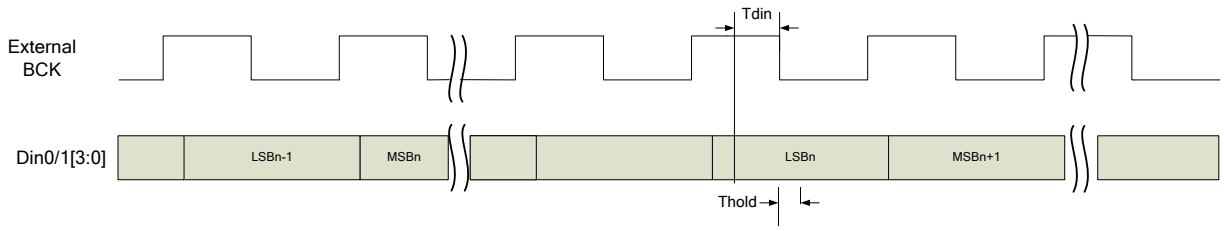


Figure 15: InS Receive Constants

Tdin	BCK0	BCK1
Di0[0] In setup before negative edge of Bck	6.01ns	8.73ns
Di0[1] In setup before negative edge of Bck	6.22ns	8.58ns
Di0[2] In setup before negative edge of Bck	6.78ns	9.14ns
Di0[3] In setup before negative edge of Bck	6.7ns	9.06ns
Di1[0] In setup before negative edge of Bck	6.17ns	8.53ns
Di1[1] In setup before negative edge of Bck	6.02ns	8.38ns
Di1[2] In setup before negative edge of Bck	6.01ns	8.37ns
Di1[3] In setup before negative edge of Bck	6.03ns	8.39ns

Table 13: Audio In port timing when used as InS

The hold time requirement (Thold) is less than 0ns.

8.2 AES Interface

For configuring Audio Port for AES please refer to section 4.1.5 in the User Guide.

In this section all data lines when used as AES, are referred to FCK0 which is as close to internal representation of frame count (sys1fs) as possible. FCK0 can be programmed to have duty cycle of 1 BCK0 or 32 BCK0 (please refer to section 5.6 of User Guide for programming), if duty cycle of frame count is of no concern and only the positive edge is used.

Timing const	Min	Max
Fck0 to AES data out (Do0[3:0])		0.1ns
Fck0 to AES data out (Do1[3:0])		0.2ns

Table 14: AES output data lines timing

Timing const	Min	Max
AES data in through port0 (Di0[3:0])		0.1ns
AES data in through port1 (Do1[3:0])		0.2ns

Table 15: AES input data lines timing

8.3 ADAT Interface

The TCD22xx chips contain two identical Alesis ADAT compatible transmitter/receiver pairs. Each ADAT block can transmit 8 channels of audio at the base rates. The transmitter can also handle 4 channels of audio at medium rate (96KHz) and 2 channels at high system rate (S-Mux mode). ADAT uses Audio ports as external interface. Only Audio Port 0 can be connected to ADAT. For configuring Audio Port for ADAT refer to section 4.1.5 in the User Guide.

Timing const	Min	Max
ADAT data in (Di0[3:0])		3ns
ADAT data out (Do0[3:0])	4.12ns	4.3ns

Table 16: ADAT Timing constants

8.4 UART

The UART in the DICE JR is implemented in compliance with industry standard type 16550. The UART uses an internal baud generator clocked by APB clock 'pclk' (connected to ARM system clock – typically 49.152 MHz).

The TCD2210 and TCD2220 does not support the UART handshake pins, only the serial communication pins. In applications where the handshake pins are required GPIO signals can be used instead.

8.4.1 Signal Description

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
UART0_TX	130	115	O	4	Serial output; active-high
UART0_RX	131	116	I	-	Serial input; active-high (5V)
UART1_TX	134	119	O	4	Serial output; active-high
UART1_RX	135	120	I	-	Serial input; active-high (5V)

Table 17: UART Signal Description

8.4.2 Signal Timing

Timing const	Min	Max
U0tx		13.0ns
U0rx min setup		3.5ns
U1tx		13.5ns
U1rx min setup		3.8 ns

Table 18: UART timing constants

8.5 I2C

The I2C bus is a two-wire synchronous serial interface. The I2C Interface module can operate in both standard mode (with data rates up to 100 Kb/s), fast mode (with data rates up to 400 Kb/s), and high-speed mode (with data rates up to 3.4 Mb/s). The I2C Interface can communicate with devices only of these modes as long as they are attached to the bus. The I2C serial clock determines the transfer rate.

The data signal (i2cd) is a bidirectional signal and changes only while the serial clock signal (i2cc) is low. The output drivers are open-drain or open-collector to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400 pF. Data is transmitted in byte packages.
To support standard and fast mode pull up resistors need to be added externally to both data and clock lines. The recommended value of the resistor is 2.2K. To support a high-speed mode a constant current source need to be added on board.

8.5.1 Signal Description

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
I2C_CLK	104 (shared)	97 (shared)	I/O (S)	6	I2C Clock (OD[1], 5V)
I2C_DATA	105 (shared)	98 (shared)	I/O (S)	6	I2C Data (OD, 5V)

Table 19: I2C signal description

8.5.2 I2C Timing

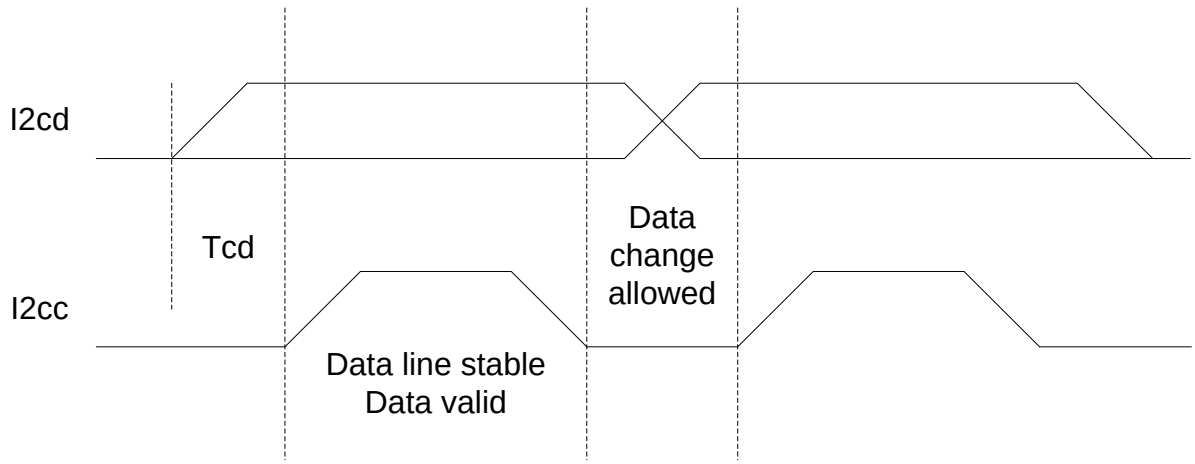


Figure 16: I2C Timing Diagramm

Timing const	Min	Max
I2C data out to I2C clock out (master out)		0.59ns
I2C data out after I2C clock in (slave out)	10.79ns	
I2C data in to I2C clock out (master in)		277ns
I2C clock in to I2C data in (slave in)		0.17ns

Table 20: I2C Timing constraints

8.6 GPIO

The General Purpose I/O (GPIO) module has 14 external pins on TCD2220 and 8 on TCD2210. The default direction of the GPIOs is input. This can be changed in firmware during boot. Generally there is no need for any external hardware to be connected to the GPIO. Only if there is a concern for the startup condition of the GPIO pin then external pull-up resistor should be added.

The GPIO module includes logic to support the debouncing of glitches. It also includes logic to support interrupt detection. The active level or edge for interrupt detection is active high. The GPIO also includes metastability registers to synchronize read back data.

The GPIO pins share functionality. Consult the GPCSR section in the User Guide for further details.

8.6.1 Signal Description

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
GPIO0	42 (shared)	N/A	I/O (S)	6	General Purpose I/O (5V)
GPIO1	138 (shared)	123 (shared)	I/O (S)	6	General Purpose I/O (5V)
GPIO2	139 (shared)	124 (shared)	I/O (S)	6	General Purpose I/O (5V)
GPIO3	137 (shared)	122 (shared)	I/O (S)	6	General Purpose I/O (5V)
GPIO4	85 (shared)	78 (shared)	I/O (S)	6	General Purpose I/O (5V)
GPIO5	86 (shared)	79 (shared)	I/O (S)	6	General Purpose I/O (5V)
GPIO6	117 (shared)	106 (shared)	I/O (S)	8	General Purpose I/O (5V)
GPIO7	118 (shared)	107 (shared)	I/O (S)	8	General Purpose I/O (5V)
GPIO8	119 (shared)	108 (shared)	I/O (S)	8	General Purpose I/O (5V)
GPIO9	55	N/A	I/O (S)	8	General Purpose I/O (5V)
GPIO10	56	N/A	I/O (S)	8	General Purpose I/O (5V)
GPIO11	57 (shared)	N/A	I/O (S)	8	General Purpose I/O (5V)
GPIO12	65 (shared)	N/A	I/O (S)	6	General Purpose I/O (5V)
GPIO13	66 (shared)	N/A	I/O (S)	6	General Purpose I/O (5V)
GPIO14	67 (shared)	N/A	I/O (S)	6	General Purpose I/O (5V)

Table 21: GPIO Signal Description

Note that all pins used by the GPIO module are multi-purpose or shared. The function and direction of these pins is software configurable via the GPCSR module.

Refer to the GPCSR module description in the User Guide for more information regarding possible configurations.

8.6.2 GPIO Timing

When used as GPIOs, the following timing is observed inside the chip:

Signal	Maximum input setup	Maximum output delay
GPIO0	2.35073ns	14.339437ns
GPIO1	2.29445ns	17.261551ns
GPIO2	2.41984ns	17.487366ns
GPIO3	2.526379ns	16.225338ns
GPIO4	2.615209ns	15.068150ns
GPIO5	2.38146ns	15.641041ns
GPIO6	2.160249ns	14.893370ns
GPIO7	2.5068ns	17.401211ns
GPIO8	2.31525ns	14.709011ns
GPIO9	2.68ns	15.302578ns
GPIO10	2.79938ns	15.434248ns
GPIO11	2.528501ns	15.618498ns
GPIO12	2.00081ns	18.142921ns
GPIO13	2.47561ns	16.453640ns
GPIO14	2.51485ns	16.537189ns

Table 22: GPIO signal Timing

8.7 1394 Link

The IP on board the chip implements the LINK layer functionality specified by IEEE1394-2000a standard. PHY is implemented on the board. Any PHY supporting the same standard can be used. No additional hardware is necessary to connect PHY to the TCD22xx chip. Traditionally, TI TSB41AB2 PHY is used.

8.7.1 Signal Description

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
SCLK	54	53	I (S)	-	49.152MHz PHY Clock
PHD0	58	54	I/O (S)	8	PHY tristatable data line bit 0
PHD1	59	55	I/O (S)	8	PHY tristatable data line bit 1
PHD2	60	56	I/O (S)	8	PHY tristatable data line bit 2
PHD3	63	59	I/O (S)	8	PHY tristatable data line bit 3
PHD4	64	60	I/O (S)	8	PHY tristatable data line bit 4
PHD5	68	61	I/O (S)	8	PHY tristatable data line bit 5
PHD6	69	62	I/O (S)	8	PHY tristatable data line bit 6
PHD7	70	63	I/O (S)	8	PHY tristatable data line bit 7
PHCT0	71	64	I/O (S)	8	PHY tristatable control line bit 0
PHCT1	72	65	I/O (S)	8	PHY tristatable control line bit 1
PHDI	73	66	I (S)	-	A high indicates isolation barrier is not present (PU, 5V)
PHLR	74	67	O	8	Serial request output from S-LINK (Z)
PHLP	75	68	O	4	Link power status. Pulsing if isol. barrier present
PHLO	76	69	I (S)	-	Link on indication from PHY. Pulsing when asserted (PU, 5V)

Table 23: Signal Description

8.7.2 Link Timing specification

Timing const	Min	Max
Delay time, SClk input high to initial instance of PHDn, PHCT0, PHCT1, and PHLR outputs valid	1ns	10ns
Delay time, SClk input high to PHDn, PHCT0, PHCT1, and PHLR invalid (high-impedance)	1ns	10ns
Setup time, PHDn, PHCT0 and PHCT1 inputs before SClk	6ns	

Hold time, PHDn, PHCT0 and PHCT1 inputs after SClk	0ns	

Table 24: Link Interface timing

8.8 SPI Interface

8.8.1 SPI features

The SPI interface implemented in TCD22xx can be programmed to be master or slave and supports four different combinations of clock phases and polarity, several Data Lengths (8-bit, 16-bit, 24-bit & 32 bit), MSB can be transferred first or last, depending on the configuration. The SPI bit rate also can be controlled in master mode. All transfer parameters should be identical for the master device and slave device involved in the current transaction and can be changed on the master side between transfers to accommodate various requirements of the slave devices.

8.8.2 Signal Description

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
SPIA_SS	138 (shared)	123 (shared)	I/O (S)	6	SPI Slave Select
SPIA_MISO	139 (shared)	124 (shared)	I/O (S)	6	SPI Master. In, Slave Out
SPIA_MOSI	104 (shared)	97 (shared)	I/O (S)	6	SPI Master. Out, Slave In
SPIA_CK	105 (shared)	98 (shared)	I/O (S)	6	SPI Clock
SPIB_SS	57 (shared)	N/A	I/O (S)	6	Alt. SPI Slave Select
SPIB_MISO	65 (shared)	N/A	I/O (S)	6	Alt. SPI Master. In, Slave Out
SPIB_MOSI	66 (shared)	N/A	I/O (S)	6	Alt. SPI Master. Out, Slave In
SPIB_CK	67 (shared)	N/A	I/O (S)	6	Alt. SPI Clock

Table 25: SPI Signal description

The SPI clock is generated by the master, and the SPI_SS signal represents the slave device select from the SPI master. The SPI clock, MISO & MOSI pins are directly connected between master and slave. The MISO signal is the output from the slave (slave transmission) and the MOSI signal is the output from the master (master transmission). On the chip interface SPI signals can be mapped to two locations depending on GPCSR register configuration (see User Guide **Error! Reference source not found.**). Location B is not available in TCD2210.

8.8.3 SPI timing

Timing const	Min	Max
Master Mode		
SPIA Slave Select to SPIA clock out		0.83ns
SPIA Master out to SPIA clock out		1.04ns
SPIA Master In to SPIA clock out		SPI clock period/2 – 7.7ns
SPIB Slave Select to SPIB clock out		-0.08ns
SPIB Master out to SPIB clock out		0.36ns

Timing const	Min	Max
SPIB Master In to SPIB clock out		SPI clock period/2 – 8.39ns
Slave Mode		
SPIA Slave Select in after SPIA clock in		0.83ns
SPIA Slave out after SPIA clock in	13.15ns	
SPIA Slave In after SPIA clock in		1.28ns
SPIB Slave Select in after SPIB clock in		-0.005ns
SPIB Slave out after SPIB clock in	13.14ns	
SPIB Slave In after SPIB clock in		1.02ns

Table 26: SPI Timing constraints

8.9 Clock controller

The clock controller contains the logic to handle selection of clock sources, clock domain memberships, block sync selection for the 60958 and AES receivers and transmitters, as well as setup for receiver clock regeneration (onboard VCO's), sample rate/phase detection and other clock related functions of the TCD22XX.

The Clock controller receives clock frequency from external oscillator circuit whose inputs are pins xtal 1 and xtal2 (typically 25.000MHz). Other external sources provide Clock controller with reference events for Jet™ PLL . Jet™ PLL takes any reference input and generates a base rate (1fsBase) and 512 times the base (512fs) rate clocks for the internal blocks.

The clocks coming out of the JET PLL are qualified such that the 1fsBase is driven on the negative edge of the 512fs so it is guaranteed to be valid on the rising edge of 512fs. 1fsBase can be monitored on the WCO output of the chip.

For all other outputs such as InS transmitters and ADAT the internal logic is sampling this 1fsBase on the rising edge of 512fs, so all operations of those modules will be aligned to that event. This means that all communication from these modules will be observed on the outside ½ 512fs later than 1fsbase event on the WCO output, which is ~20ns.

8.9.1 Signal Description

Signal	TCD2220	TCD2210	I/O	Drive (mA)	Description
EXT_FBR WCLK_IN0	85	78	B	6	External 1fs base rate clock (5V)
EXT_512BR WCLK_OUT0	86	79	B	6	External 512 x base rate clock (5V)/ Word clock out
XTAL2	102	95	O	-	XTAL - clock doubler/power manager/LLC
XTAL1	103	96	I	-	XTAL - clock doubler/power manager/LLC
WCLK_IN1	65	N/A	B	6	Word Clock In (5V)
WCLK_OUT1	66	N/A	B	6	Word Clock Out

Table 27: Clock Controller Signal Description

8.9.2 External Circuit (Jet™ PLL, AES and CLK_DBL).

DICE 22xx has 3 analog PLL's requiring 3 external components each to set the analog PLL loop filter values. COG / NPO types are recommended for the two capacitors. X7R types and 10% may do well in certain cases. A concern here is that pronounced mechanical capacitance changes have been observed on several non COG/NPO capacitor types.

The actual analog PLL loop filter circuit for each PLL is C2//(C1+R1), a series circuit between the chip filter pin and GND. See below figure. Minimum wiring length as well as allowing no other current to be drawn in the filter GND loops is highly recommended.

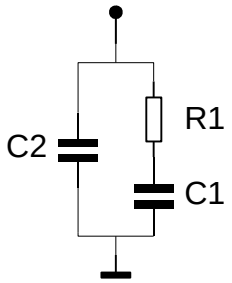


Figure 17: External filter diagram for Jet™ PLL & Clock Doubler PLL.

	Jet™ PLL's	Clock doubler
C1	10nF	470pF
C2	100pF	10pF
R1	1kohm	4.7kohm

Table 28: Recommended values for the Jet™ PLL & Clock Doubler PLL loop filters on TCD22xx.

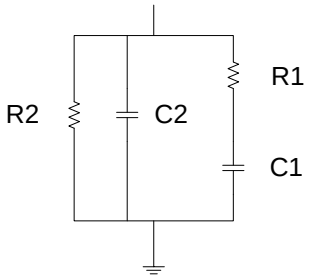


Figure 18: External filter diagram for AES PLL

	AES
C1	10nF
C2	10pF
R1	1kohm
R2	1mohm

Table 29: Recommended values for the AES PLL loop filter

Chapter 9 Electrical Characteristics

9.1 DC Characteristics

1.8v Core supply measured at 1.8v and ambient temperature of 20 deg.

Condition	min	typ	Max	Comment
nReset = 0v		20 mA		System Reset
Power Down		2 mA		Prepared to wake on LinkOn
ARM, no audio		97 mA		Audio subsystem not started
Normal Operation		100 mA	180mA	96KHz AES and 1394 Audio

3.3v Core supply measured at 3.3v and ambient temperature of 20 deg.

Condition	Min	typ	Max	Comment
nReset = 0v		-		System Reset
Power Down		-		Prepared to wake on LinkOn
ARM, no audio		-		Audio subsystem not started
Normal Operation		115 mA	200 mA	96KHz AES and 1394 Audio

The 3.3v supply consumption will depend on the actual loading of the outputs of the chip, these numbers are for a typical application such as the evaluation board with code executing from SDRAM.

9.1.1 3.3V DC Characteristics

Symbol	Parameter		Condition	Min	Typ.	Max	Unit
V_{IH}	High level input voltage LVCMOS interface			2.0			V
V_{IL}	Low level input voltage LVCMOS interface					0.8	
V_T	Switching threshold				1.4		
V_{T+}	Schmitt trigger, positive-going threshold		CMOS			2.0	
V_{T-}	Schmitt trigger, negative-going threshold		CMOS	0.8			
I_{IH}	High level input current	Input buffer	$V_{IN} = V_{DD}$	-10		10	µA
		Input buffer with pull-down		10	33	60	
I_{IL}	Low level input current	Input buffer	$V_{IN} = V_{SS}$	-10		10	
		Input buffer with pull-down		-60	-33	-10	
V_{OH}	High level output voltage	Type B1 to B24	I_{OH} = -1µA	V_{DD} – 0.05			V
		Type B1	I_{OH} = -1mA	2.4			
		Type B2	I_{OH} = -2mA				
		Type B4	I_{OH} = -4mA				
		Type B8	I_{OH} = -8mA				
		Type B12	I_{OH} = -12mA				
		Type B16	I_{OH} = -16mA				
		Type B20	I_{OH} = -20mA				
		Type B24	I_{OH} = -24mA				
V_{OL}	Low level output voltage	Type B1 to B24	I_{OH} = 1µA			0.05	
		Type B1	I_{OH} = 1mA			0.4	
		Type B2	I_{OH} = 2mA				
		Type B4	I_{OH} = 4mA				
		Type B8	I_{OH} = 8mA				

Symbol	Parameter		Condition	Min	Typ.	Max	Unit
		Type B12	I_{OH} = 12mA				
		Type B16	I_{OH} = 16mA				
		Type B20	I_{OH} = 20mA				
		Type B24	I_{OH} = 24mA				
I_{OZ}	Tri-state output leakage current		V_{OUT} = V_{DD} or V_{SS}	-10		10	μA
I_{DD}	Quiescent supply current					100	
C_{IN}	Input capacitance		Any input and bi-directional buffers			4	pF
C_{OUT}	Output capacitance		Any output buffer				

9.1.2 Absolute Maximum Ratings

Symbol	Parameter	Rating			Unit
			Min	Max	
V_{DD}	DC supply voltage	1.8V V_{DD}	-0.5	2.7	V
		3.3V V_{DD}	-0.5	4.8	
V_{IN}	DC input voltage	3.3V input buffer	-0.5	4.8	
		3.3V interface/ 5V tolerant input buffer	-0.5	6.5	
V_{OUT}	DC output voltage	3.3V output buffer	-0.5	4.8	
		3.3V interface/ 5V tolerant output buffer	-0.5	6.5	
I_{IO}	Input/Output current	± 20			mA
T_A	Storage temperature	-65 to 150			°C

9.1.3 Recommended Operating Conditions

Symbol	Parameter	Rating			Unit
			Min	Max	
V_{DD}	DC supply voltage for internal (=V_{DDIN})	1.8V V_{DD}	1.65	1.95	V
	DC supply voltage for I/O block (=V_{DDIO})	3.3V V_{DD}	3.0	3.6	
	DC supply voltage for analog core (=V_{DDA})	1.8V V_{DD}	1.8 – 5%	1.8 + 5%	
V_{IN}	DC input voltage	3.3V input buffer	-0.3	V_{DCIO} + 0.3	
		3.3V interface/ 5V tolerant input buffer	-0.3	5.5	
V_{OUT}	DC output voltage	3.3V output buffer	-0.3	V_{DCIO} + 0.3	
		3.3V interface/ 5V tolerant output buffer	-0.3	5.5	
T_A	Commercial temperature range			0 to 70	°C
	Industrial temperature range			-40 to 85	

9.2 PLL Characteristics

9.2.1 Recommended Operating Conditions

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage differential	AVDD18D/ AVDD18A	−0.1	–	0.1 V	V
Operating temperature	Topr	−40	–	85	°C

9.2.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Operating voltage	AVDD18D/ AVDD18A	1.65	1.8	1.95	V
Digital input voltage high	IIH	0.7VDD	–	–	V
Digital input voltage low	IIL	–	–	0.3VDD	V
Dynamic current	IDD	–	–	3	mA
Power down current	IPD	–	–	220	uA

9.2.3 AC Electrical Characteristics

Characteristics		Symbol	Min	Typ	Max	Unit
Input frequency		FIN	4	–	50	MHz
Output clock frequency		FOUT	20	–	300	MHz
VCO output frequency		FVCO	160	–	400	MHz
Input clock duty cycle		TID	40	–	60	%
Output clock duty cycle		TOD	45	–	55	%
Locking time		TLT	–	–	150	us
Cycle to cycle jitter	20M ~100MHz	TJCC	–300	–	300	ps
	100M ~ 200MHz	TJCC	–200	–	200	ps
	200M ~ 300MHz	TJCC	–120	–	120	ps

Chapter 10 Thermal Ratings

Operating Temperature

	MIN	TYP	MAX	UNIT
Operating ambient temperature, TCD22xx	0		70	**°C**
Operating ambient temperature, TCD22xx-E	-40		85	**°C**

Thermal Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
128 QFP	Board mounted, no air flow		46.4		**°C** /W
144 LQFP	Board mounted, no air flow		45.3		**°C** /W

Absolute Maximum Ratings over Operating Temperature Ranges

Supply voltage range AV_{dd} (1.8V)	-0.5 V to 2.7 V
V_{dd} (3.3V)	-0.5 V to 4.8 V
PLL_V_{dd} (1.8V)	-0.5 V to 2.7 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free–air temperature T_A – (TCD22xx)	0 **°C** to 70 **°C**
Operating free–air temperature T_A – (TCD22xx-E)	-40 **°C** to 85 **°C**
Storage temperature range T_{stg} -	-65 **°C** to 150 **°C**

Exposure to absolute–maximum–rated conditions for extended periods affects device reliability. Stresses beyond those listed under absolute maximum ratings cause permanent damage to the device.

Appendix 1. Revision history

Revision	Made By	Notes
0.01	L. Sherbak	Created based on User Guide
1.00	ML	Small format changes to InS section and table headers
1.01	ML	Added hold time comment for InS Receivers
1.02	ML	Changed internal RAM size to 16kb Added Electrical Specifications and Thermal Ratings Updated WCLK documentation
1.03	BK	Added disclaimer Moved revision history to here TOC fixes