DICE Jr/Mini Evaluation Board Rev1.10 Hardware Guide Addendum

Draft

File: DICE_JR_MINI_Evaluation_Board_Rev110_Hardware_Guide_Addendum.doc
Printed: 02/06/2008
Updated: 02/21/2008
Version: 0.9

Revision history

When	Who	What
2008-02-06	GIANA	Document Started. – 0.1-0.6
2008-02-10	BRKAR	Edits, formatting 0.7
2008-02-20	GIANA	Add LCD Interface module
2008-02-21	BRKAR	Edits 0.9

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1. Introduction

The DICE JR/Mini Evaluation board provides an easy to use evaluation and development platform for DICE Jr, DICE Mini and DICE II. By using detachable modules or “Microboards” mounted DICE Jr, DICE Mini or DICE II, engineers can evaluate the performance of the entire DICE family of devices.
The DICE Jr/Mini evaluation board is equipped with the following interfaces: AES3, SPDIF, dual-ADAT, four channels of analog input and output ports for audio, Word-sync, MIDI, two RS232 ports, 8 bit preset, 8 LED’s and two data ports for controls. The board can be connected to an IEEE1394 (Firewire) network via two standard 6-pin connectors. The entire board is operated by a DC 12V 1A external power source. The I2S, DSAI and AES3 signals from a DICE family module can be routed to different inputs and/or outputs from the default setup by using audio signal router jumpers placed on the board. Two data ports can be used to connect to external hardware. A DSP module port is also available for additional audio signal processing.

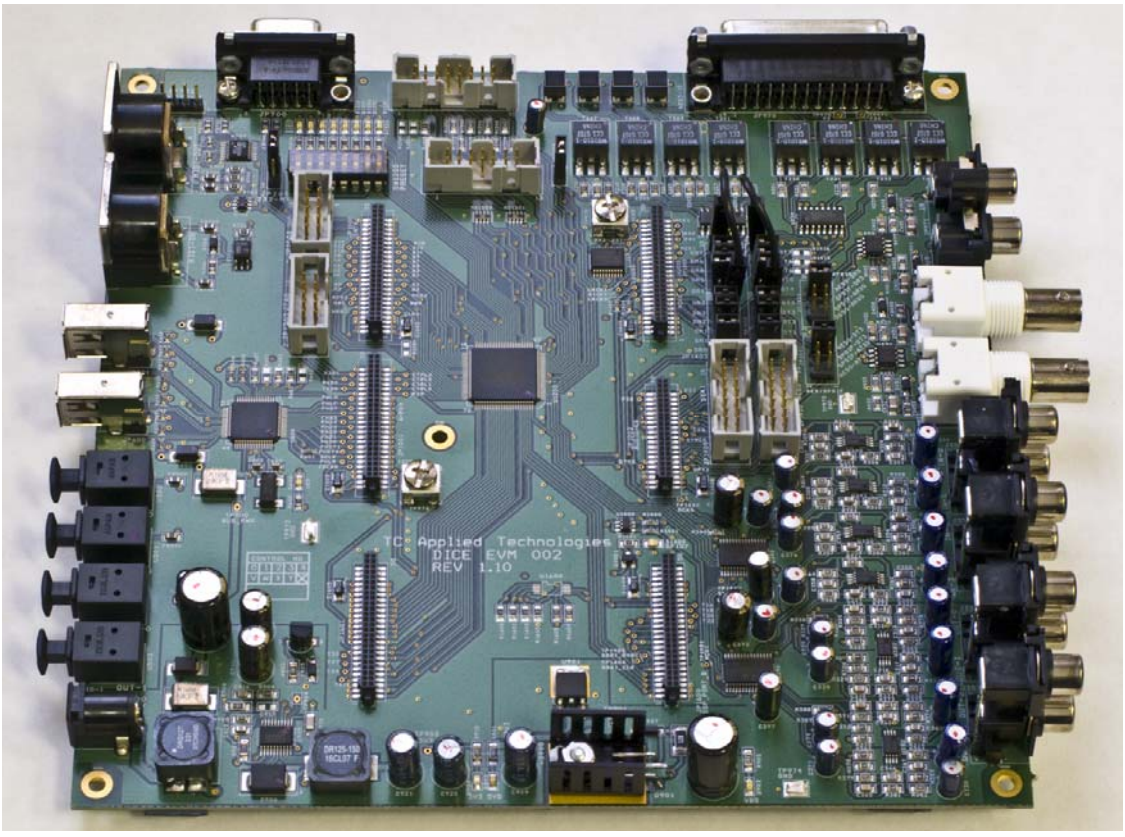

Figure 1: DICE EVM 002 Rev 1.10 Main Board

2. DICE™ Jr / Mini / II Evaluation Board Rev 1.10

What's new

GPIO4 & 5 Assignment Jumper

Byte-select pin BS0 and BS1, GPIO4 and GPIO5 of DICE are now connected to CPLD through signal switch U1000. Despite current CPLD firmware does not utilize both input signal BS0 and BS1, this switch allow rerouting GPIO4 and 5 to be connected to CPLD's BS0 and BS1 for future use.
With jumper placed at JP1005 (default), Both DICE's BS0 and BS1 are connected to CPLD's BS0 and BS1. GPIO4 and GPIO5 are connected to word sync input and output connector.
Without jumper placed at JP1005, DICE's BS0 and BS1 are disconnected. GPIO4 and GPIO5 are now connected to CPLD's BS0 and BS1.
In case of DICE II, GPIO14 pin is connected to either word sync input or BS0, and GPIO15 is connected to either word sync output or BS1.

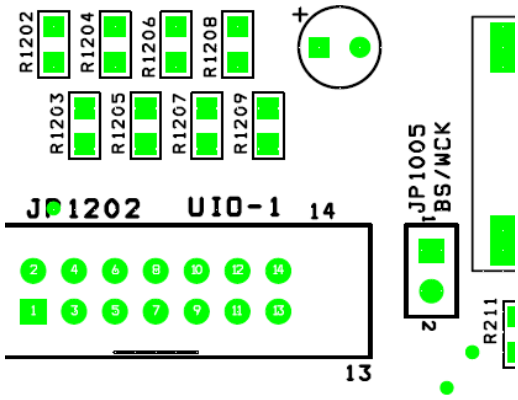

Figure 2: GPIO4 & 5 Assignment jumper

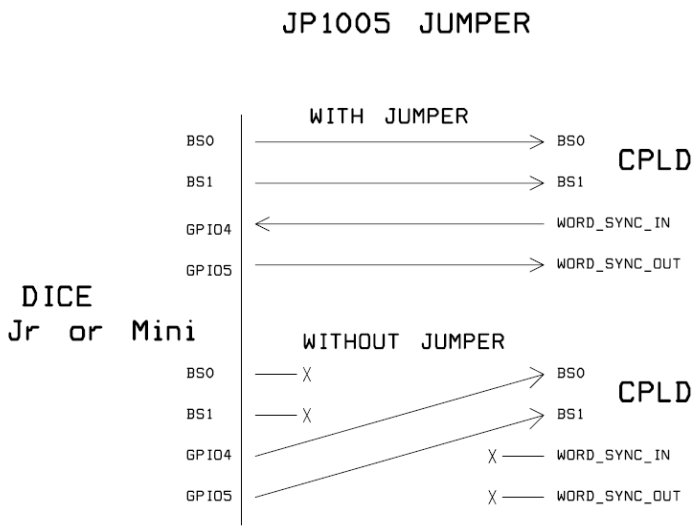

Figure 3: GPIO4 & 5 Signal paths

GPIO7 LED

DICE-Jr and Mini clock signal pin FCK1 can be configured as general purpose IO pin, GPIO7. New LED D1000 is connected to this signal path to provide simple method to monitor a state of signal.
In case of DICE II, this LED is connected to DICE II 's none configurable pin FCK1.

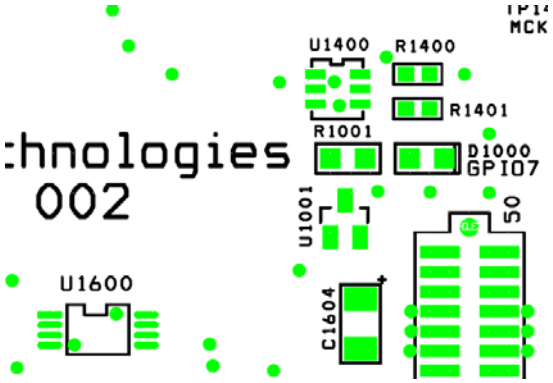

Figure 4: GPIO7 LED - D1000

DIP switch SW1200

All eight bits of this switch is now of available to user and bit mapped to CPLD's register.

DC Power requirement

The DICE-Jr/Mini Evaluation board operates with an AC-DC adapter min. 1A, operating range of DC 12V to 24V supplied by a centre positive 2.5mm DC plug. A 12V DC supply is recommended.

Parallel Bus and SPI port Pin Assignment

Parallel Bus - JP1201

Pin	Signal Name
1	Ground
2	VCC, 3.3V or 5V
3	UIA_D0 or Fix DC Voltage
4	UIA_D1
5	UIA_D2
6	UIA_D3
7	UIB_D0
8	UIB_D1
9	UIB_D2
10	UIB_D3
11	UIB_D4
12	UIB_D5
13	UIB_D6
14	UIB_D7
15	Ground
16	3.3V

Table 1: Parallel bus – JP1201

External SPI Port – JP1202

Pin	Signal Name
1	VCC, 3.3V
2	VCC, 3.3V
3	Ground
4	Ground
5	SPI_NCS, UIC_D0
6	Ground
7	SPI_CLK, UIC_D1
8	Ground
9	SPI_MOSI, UIC_D2
10	Ground
11	SPI_MISO, UIC_D3
12	Ground
13	NRST
14	Ground

Table 2: External SPI port – JP1202

3. CPLD and Register Map

Usage

The U1200, Altera CPLD EPM240-T100, is the main device used to interface with user provided hardware. All signals required for parallel data communication with the DICE embedded ARM processor, such as data D0 through D15, address A0 through A3, byte-select BS0 and BS1, chip select NCS2, control signals NRD, NWR and NRST, are connected to this CPLD.
For user interface, 8 LEDs – D1216 through D1223 and 8 bit preset switch - SW1200 are bit mapped to the CPLD register.
Parallel bus - JP1201 is connected to the CPLD with total of 16 data lines and a master reset signal, and with 4 data lines and master reset signal for External SPI Port - JP1202.

Register Map

Bit 2 of control register is now assigned for mode setting of External SPI port. All eight bits of DIP switch SW1200 are bit mapped to a register at address 0x4.

NC2	A[0..2]	BIT	Description	Default value	Access Mode
0	000		**Control register**		R/W
		7	DICE parallel bus access enable. 0: Disable, 1: Enable	0	
		6	Codec Enable. 0: Disable, 1: Enable	1	
		5	SPI Port-1 select. 0:Disable, 1:Enable	1	
		4	SPI Port-0 select. -//-	1	
		3	LED & DIP switch mode. 0:POST, 1:User	0	
		2	External SPI port mode. 0: Normal, 1: Exclusive	0	
		1	UIB_D port mode. 0: Normal, 1: LCD	0	
		0	UIB_D port mode. LCD RS mode register	0	
0	001		**Status register**		R
		7~2	Reserved	0	
		1	UIA & UIB port busy	0	
		0	SPI port busy	0	
0	010		**UIB_D port data**		R/W
		7_0	Data value	0	
0	011		**LED data register**		W
		7~0	Data for LED D1216 ~ D1223	0x00	
0	100		**DIP switch register**		R
		7~0	DIP switch setting of SW1200		
0	101	7~0	**Reserved**		
0	110	7~0	**Reserved**	0	-
0	111	7~0	**Firmware version**	0x13	R
1	XXX		Invalid		

Table 3: CPLD Register map

4. SPI Port

SPI Port Control Register Bit 2

1. Normal mode, Control register bit 2: 0

Any SPI command and data bit sent by DICE will be broadcasted to all SPI ports, CODEC, CPLD and External SPI port. SPI command and data must be conformed to 8 command bits followed by 8 data bits. The command data must include pre-defined port address, such as two MSB bit must be "10" for CODEC, “11" for CPLD and "01" for External port.
Reading External port data, first 8 bits of data read from the port will be stored then re-send the data to DICE SPI port (MISO) as data bit.

2. Exclusive mode, Control register bit 2: 1

External SPI port is exclusively assigned to DICE's SPI port.
This allows External SPI port accesses with any bit patterns and any bit length. Access to CODEC and CPLD by DICE’s SPI port is disabled. Using DICE's Parallel mode to CPLD does not affected by this setup.

Pre Defined Port Address

Address for CODEC, CPLD and External port (Optional User Interface board) are all pre defined as listed below.

1. CODEC address (AK4528 and AK4620)
   Read "1000_0000" ~ "1000_0111" (0x80 ~ 0x87)
   Write "1010_0000" ~ "1010_0111" (0xA0 ~ 0xA7)

2. CPLD register address
   Read "1100_0000" ~ "1100_0111" (0xC0 ~ 0xC7)
   Write "1110_0000" ~ "1110_0111" (0xE0 ~ 0xE7)

3. External address with Optional User IF board, Normal mode
   Read "0100_10xx" (0x48 ~ 0x4B)
   Write "0110_00xx" (0x60 ~ 0x63)

4. External address, Exclusive mode
   Read Any
   Write Any

For External SPI port, any bit length of command and data can be used when the port is defined as “Exclusive” by setting bit 2 of the control register.

SPI Format

SPI command and data must be conformed to 8 command bits followed by 8 data bits.
To write to SPI slave device, first send 8 bits command data and followed by 8 data bits. The command data must include pre-defined port address, such as two MSB bit must be "10" for CODEC, “11" for CPLD and "01" for External port.

To read data from the SPI port, first send 8 command bits. Then the slave device will return 8 data bits.

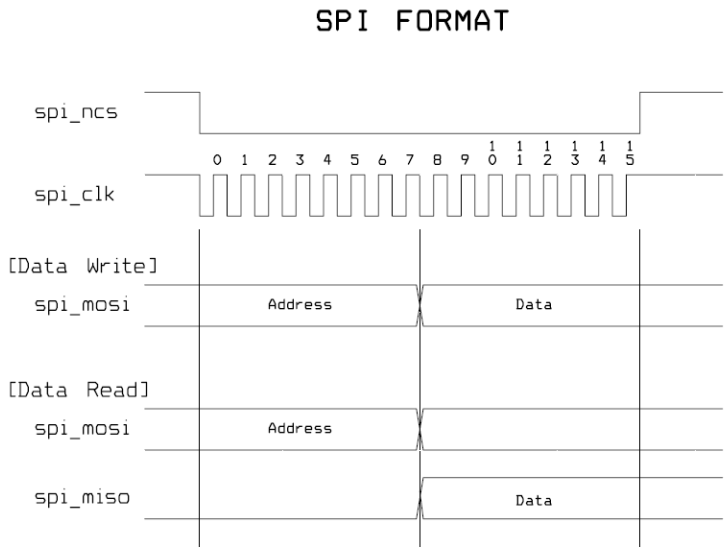

Figure 5: SPI format

5. Optional User Interface Board

The Optional User Interface board contains two 7-segment LED displays, 36 LED's, one rotary switch and four pushbutton switches. This board should be connected to connector JP1201 of the DICE EVM002 Rev 1.10 board using a 14-pin flat cable.

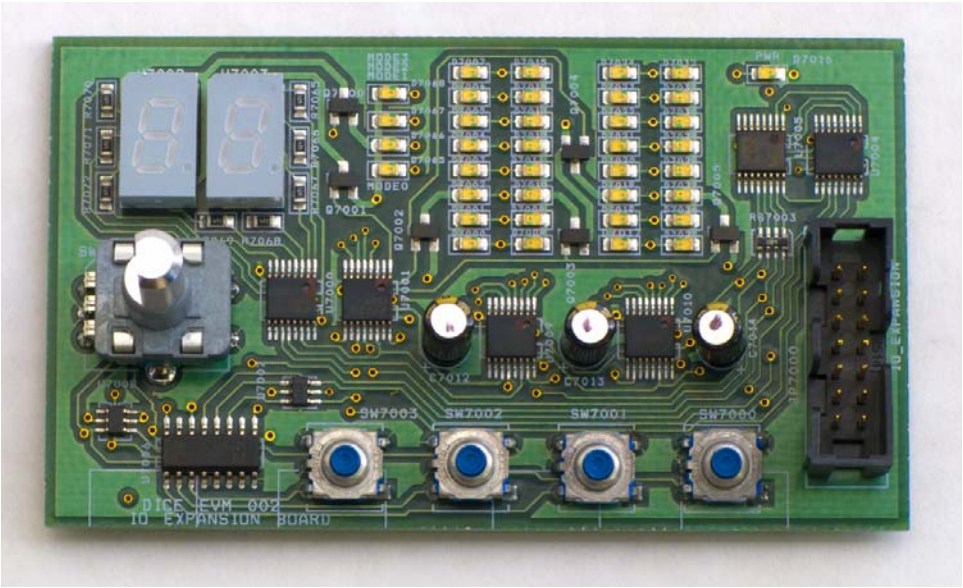

Figure 6: Optional User Interface board

6. Optional LCD Interface Board

The optional LCD interface board provides a simple solution to add industry standard DC-5V LCD modules to the DICE EVM002 board.

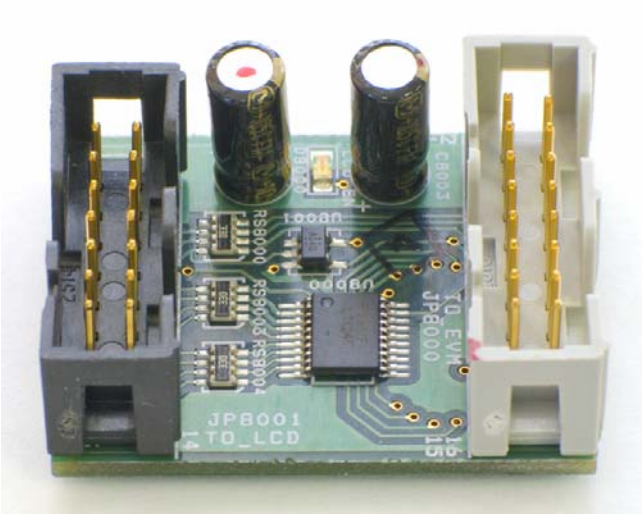

Figure 7: LCD Interface Module

Figure 8: LCD Module

DC5V for LCD module

The DICE EVM002 Parallel bus connector JP1201 provides either 3.3V to VCC pin #2 as default, or 5V instead. To use this port with a 5V LCD module, make sure to remove resistor R1227 and populate R1226 with 0R resistor. Both resistors are located at bottom side of the board near JP1201 connector.

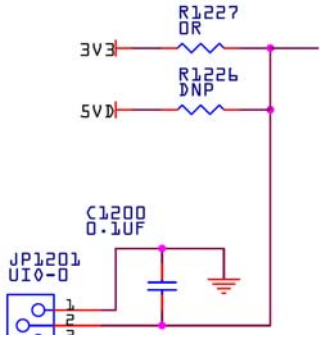

Figure 9: Parallel bus 3.3V/5V

The table below shows DICE EVM002 Parallel bus connector JP1201 pin assignments in LCD mode. These signal pins are not 5V tolerant.

Pin	Signal Name
1	Ground
2	5V
3	Not used by LCD module
4	RS (3.3V)
5	R/W (3.3V)
6	E (3.3V)
7	D0 (3.3V)
8	D1 (3.3V)
9	D2 (3.3V)
10	D3 (3.3V)
11	D4 (3.3V)
12	D5 (3.3V)
13	D6 (3.3V)
14	D7 (3.3V)
15	Ground
16	3.3V

Table 4: JP1201 LCD mode signal assignment

LCD Interface module

LCD Contrast adjustments can be made by changing the ratio of resistors R8000 and R8001 on the LCD Interface module. Both resistors are located on the bottom side of the board near the JP8001 connector.

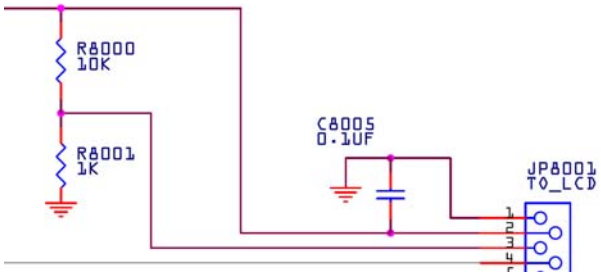

Figure 10: LCD Contrast control resistors

The table below shows signal assignments of JP8001 connector on the LCD Interface module. All bi-directional data pins, from pin 7 to 14, are 5V tolerant.

Pin	Signal Name
1	Ground
2	5V
3	Contrast Vss
4	RS
5	R/W
6	E
7	D0 (5V)
8	D1 (5V)
9	D2 (5V)
10	D3 (5V)
11	D4 (5V)
12	D5 (5V)
13	D6 (5V)
14	D7 (5V)

Table 5: JP8001 Signal assignment

Cable connection

Please note that some LCD modules have different pin connections from the LCD Interface Module provided, such as LUMEX LCD module S01602D/C. This module's pin assignment for 5V and GND are reversed from the LCD Interface Module. So make sure to reverse these two connections as shown in Figure 11. For safety, consult with LCD module manufacturer datasheet before using LCD Interface module.

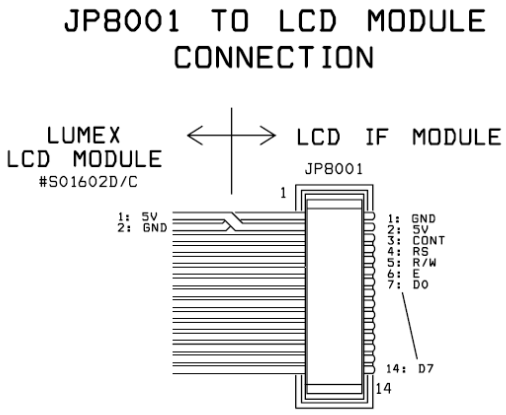

Figure 11: LCD module connection

CLI Commands for LCD

Sending characters to the LCD module can be done using CLI commands. The example below shows setting 1) LCD power-up initialization and mode, and 2) CPLD control register bits, using SPI commands. With a DICE-Jr module on the EVM board, the same can be achieved using parallel bus CLI commands.

```
evm.spi cpld 0xE0FA          // Set LCD mode bit of the CPLD Control register

evm.spi cpld 0xE230          // Send power up initialization commands to LCD
evm.spi cpld 0xE230
evm.spi cpld 0xE230
evm.spi cpld 0xC200          // Read BF flag

evm.spi cpld 0xE238          // LCD mode set, 8 bit, 5x7 dot and 2 lines
evm.spi cpld 0xE208
evm.spi cpld 0xE201
evm.spi cpld 0xE206
evm.spi cpld 0xE20E

evm.spi cpld 0xE0FB          // Set RS bit in the CPLD control register

evm.spi cpld 0xE22A          // Send character "*"
evm.spi cpld 0xE220          // "_"
evm.spi cpld 0xE244          // "D"
evm.spi cpld 0xE249          // "I"
evm.spi cpld 0xE243          // "C"
evm.spi cpld 0xE245          // "E"
evm.spi cpld 0xE220          // "_"
evm.spi cpld 0xE245          // "E"
evm.spi cpld 0xE256          // "V"
evm.spi cpld 0xE24D          // "M"
evm.spi cpld 0xE220          // "_"
evm.spi cpld 0xE230          // "0"
evm.spi cpld 0xE230          // "0"
```

```
evm.spi cpld 0xE232          // "2"
evm.spi cpld 0xE220          // "_"
evm.spi cpld 0xE22A          // "*"

evm.spi cpld 0xE0FA          // Clear RS bit
evm.spi cpld 0xE2C0          // Move to 2nd line
evm.spi cpld 0xE0FB          // Set RS bit again

evm.spi cpld 0xE246          // "F"
evm.spi cpld 0xE269          // "I"
evm.spi cpld 0xE272          // "r"
evm.spi cpld 0xE26D          // "m"
evm.spi cpld 0xE277          // "w"
evm.spi cpld 0xE261          // "a"
evm.spi cpld 0xE272          // "r"
evm.spi cpld 0xE265          // "e"
evm.spi cpld 0xE220          // "_"
evm.spi cpld 0xE252          // "R"
evm.spi cpld 0xE265          // "e"
evm.spi cpld 0xE276          // "v"
evm.spi cpld 0xE220          // "_"
evm.spi cpld 0xE231          // "1"
evm.spi cpld 0xE22E          // "."
evm.spi cpld 0xE232          // "2"
```

Note: Characters following "//" are comments and are not included in the CLI command.

7. Summary

The DICE EVM002 provides a flexible evaluation and development platform for the DICE II, DICE Jr and DICE Mini chip family. The EVM is part of a complete and easy to use solution for development of advanced, high-performance audio devices, including Firmware, Host computer Drivers, Utilities and User Interfaces. Contact TC Applied Technologies ™ for EVM and Microboard design files, chip User Guides, Firmware development kit, Host development kits and other software.