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Extended Application Protocol (EAP)
DICE

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Document History

Version	Date	Name	Comment
0.0.1.0	December 1, 2006	M Lave	Document started
0.0.7.0	February 19, 2007	M Lave	First external release
0.0.8.0	February 22, 2007	M Lave	Minor updates to capability and stand alone section.
0.0.9.0	May 30, 2007	M Lave	Added application specific space
0.1.0.0	June 25, 2007	M Lave	Added cap bits to specify if various sections are stored to flash.
0.1.0.1	July 25, 2007	M Lave	Fixed RO/RW typo in New Stream Config section and Current Config section
0.1.0.2	Sep. 10,2007	M Lave	Some more RO/RW corrections. Changed name to “Extended Application Protocol”

Table of Contents

1 Introduction

This specification specifies the Extended DICE Control protocol. This protocol in an optional addition to the DICE Driver Protocol and enables host applications to gain access to dynamic stream configuration and mixer, peak and router functionality for the chips supporting this feature.
This specification works with version 1.0.7.0 of the DICE Driver Specification with the exception of the addition of a new notification directing the driver to resynchronize the stream configuration.

2 Features

- Dynamic configuration of streams enabling control panels to provide a bandwidth configuration page.
- Direct access to routing tables enabling dynamic routing changes.
- Access to Peak information for any routed channel (DICE JR/Mini)
- Access to Mixer coefficients (DICE JR/Mini)
- Optional flash storage/retrieval of configuration parameters for each of the three major rate modes.
- Support for ‘stand alone’ mode configuration.

3 Communication model

The communication model is based on a private memory space. This memory space contains locations to read peaks, set mixer coefficients, change routing etc.
As devices can support all or parts of the protocol and functionality could expand with future chips and information and capability area is specified indicating the feature set of an actual device.
The private space used for the Extended Control Interface is split into sections. The offset to those sections are defined in the beginning of the space. This would allow for future extensions without jeopardizing backward compatibility. The following sections are defined in the EXT_CTRL_PRIVATE SPACE:

EXT_CTRL_SPC_CAPABILITY
EXT_CTRL_SPC_CMD
EXT_CTRL_SPC_MIXER
EXT_CTRL_SPC_PEAK
EXT_CTRL_SPC_NEW_ROUTING
EXT_CTRL_SPC_NEW_STREAM_CFG
EXT_CTRL_SPC_CURR_CFG
EXT_CTRL_SPC_STAND_ALONE_CFG
EXT_CTRL_SPC_APP

3.1 EXT_CTRL_PRIVATE_SPACE

Address	Parameter name	Size	Att
FFFF E020 0000_{16}	EXT_CTRL_SPC_CAPABILITY_OFS	32bit	RO
FFFF E020 0004_{16}	EXT_CTRL_SPC_CAPABILITY_SZ	32bit	RO
FFFF E020 0008_{16}	EXT_CTRL_SPC_CMD_OFS	32bit	RO
FFFF E020 $000C_{16}$	EXT_CTRL_SPC_CMD_SZ	32bit	RO
FFFF E020 0010_{16}	EXT_CTRL_SPC_MIXER_OFS	32bit	RO
FFFF E020 0014_{16}	EXT_CTRL_SPC_MIXER_SZ	32bit	RO
FFFF E020 0018_{16}	EXT_CTRL_SPC_PEAK_OFS	32bit	RO
FFFF E020 $001C_{16}$	EXT_CTRL_SPC_PEAK_SZ	32bit	RO
FFFF E020 0020_{16}	EXT_CTRL_SPC_NEW_ROUTING_OFS	32bit	RO
FFFF E020 0024_{16}	EXT_CTRL_SPC_NEW_ROUTING_SZ	32bit	RO
FFFF E020 0028_{16}	EXT_CTRL_SPC_NEW_STREAM_CFG_OFS	32bit	RO
FFFF E020 $002C_{16}$	EXT_CTRL_SPC_NEW_STREAM_CFG_SZ	32bit	RO
FFFF E020 0030_{16}	EXT_CTRL_SPC_CURR_CFG_OFS	32bit	RO
FFFF E020 0034_{16}	EXT_CTRL_SPC_CURR_CFG_SZ	32bit	RO
FFFF E020 0038_{16}	EXT_CTRL_SPC_STAND_ALONE_CFG_OFS	32bit	RO
FFFF E020 $003C_{16}$	EXT_CTRL_SPC_STAND_ALONE_CFG_SZ	32bit	RO
FFFF E020 0040_{16}	EXT_CTRL_SPC_APP_OFS	32bit	RO
FFFF E020 0044_{16}	EXT_CTRL_SPC_APP_SZ	32bit	RO
FFFF E020 0048_{16}	0x0000 0000	32bit	RO

This structure is read only and is used to specify the offset of the various configuration blocks. All values are 32 bit unsigned. The offsets are in quadlets from the start of this structure and the sizes are in number of quadlets.

3.2 CAPABILITY SPACE

The capability space enables the creation of generic control panel applications and/or generic drivers supporting the enhanced application functionality.

Offset	Parameter	Size	Attribute	Function
00_{16}	ROUTER_CAPS	32bit	RO	Indicates router capabilities
04_{16}	MIXER_CAPS	32bit	RO	Indicates mixer capabilities
08_{16}	GENERAL_CAPS	32bit	RO	Indicates general capabilities.
$0C_{16}$	RESERVED	32bit	RO	Reserved for future capability bits. Currently read as zero.

ROUTER_CAPS bit definitions

Bit	Name	Meaning
0	ROUTER_EXPOSED	If clear no router is exposed.
1	ROUTER_RO	If set router is read only and can not be configured through this interface.
2	ROUTER_FLS	Determines if router is stored to flash
16..31	MAX_ROUTES	This number is one less than the max number of router entries. A value of 0xff indicates 256 routes.

MIXER_CAPS bit definitions

Bit	Name	Meaning
0	MIXER_EXPOSED	If clear no mixer is exposed
1	MIXER_RO	Mixer coefficients are read only
2	MIXER_FLS	Determines if mixer is stored to flash
4..7	MIXER_IN_DEV	Routing input device ID for first 16 channels, if mixer has more than 16 input channels the consecutive ID's are expected.
8..11	MIXER_OUT_DEV	Routing output device ID for first 16 channels, if mixer has more than 16 output channels the consecutive ID's are expected.
16..23	MIXER_INPUTS	Number of mixer input channels.
24..31	MIXER_OUTPUTS	Number of mixer output channels.

GENERAL_CAPS bit definitions

Bit	Name	Meaning
0	STRM_CFG_EN	Dynamic stream configuration is enabled.
1	FLASH_EN	Flash store and load supported.
2	PEAK_EN	Peak enabled
4..7	MAX_TX_STREAMS	The maximum number of transmit streams which are supported by this device.
8..11	MAX_RX_STREAMS	The maximum number of receive streams which are supported by this device.
12	STRM_CFG_FLS	Determines if the stream config is stored to flash
16..23	Chip	ID of the chip used for the implementation: 0: DICE II (including router bug) 1: TCD2210 (DICE Mini) 2: TCD2220 (DICE JR) 3-255: Reserved

The capability section will be expanded in the future with ASCII descriptions of physical IO on the device enabling generic control panels to create drop down lists for routing entries and mixer channels.

3.3 COMMAND SPACE

Offset	Parameter	Size	Attribute	Function
00_{16}	OPCODE	32bit	RW	Writing op-code with execute bit set initiates execution.
04_{16}	RET_VAL	32bit	RO	Return value from previous operation. A value of zero indicates successful execution.

Definition of OPCODE bitfield

Bit	Name	Meaning
0..15	OPCODE_ID	The op-code identifier, see table below for a complete list of op-codes.
16	LD_LOW	Some commands perform operations relating to the rate mode. This bit indicates that the op-code should be performed on the LOW rate mode configuration.
17	LD_MID	Some commands perform operations relating to the rate mode. This bit indicates that the op-code should be performed on the MID rate mode configuration.
18	LD_HIGH	Some commands perform operations relating to the rate mode. This bit indicates that the op-code should be performed on the HIGH rate mode configuration.
19-30	Reserved	Should always be zero
31	EXECUTE	The host writes an op-code with this bit set. This will initiate execution and the bit will be cleared by the device when execution is completed.

Definition of OPCODE_IS's

Val	Name	Meaning
0000_{16}	NO_OP	Does nothing except for clearing the execute flag and indicate success.
0001_{16}	LD_ROUTER	Loads the router configuration written into the NEW_ROUTING space. The new routing will be loaded into the setting space for LOW/MID/HIGH depending on the corresponding op-code bits. If the space for the current rate mode is loaded this will have immediate effect on the routing otherwise it will have effect when the rate mode is changed.

Val	Name	Meaning
0002_{16}	LD_STRM_CFG	Loads the stream configuration written into the NEW_STREAM_CFG space. The new stream configuration will be loaded into the setting space for LOW/MID/HIGH depending on the corresponding op-code bits. If the space for the current rate mode is loaded this will have immediate effect on the DiceDriver information structure and a notification will be sent to the driver. The actual streaming however will not change until the driver disables streaming, reallocates isoc channels and bandwidth and restarts the streaming.
0003_{16}	LD_RTR_STRM_CFG	Equivalent to executing both of the above commands one after each other.
0004_{16}	LD_FLASH_CFG	Overwrite the current configuration with the last stored in flash. If the stored Flash setting is missing or damaged the factory default setting will be loaded. This is equivalent to what will happen at device boot time.
0005_{16}	ST_FLASH_CFG	Store current setting in Flash.

3.4 MIXER SPACE

The example below is for a 18x16 mixer as featured on TCD22xx

Offset	Parameter	Size	Attribute	Function
000_{16}	SAT_BITS	32bit	RO	Saturation bit for each of the 16 output channels. Bit 0 corresponds to channel 0 and so forth.
004_{16}	$Coeff_{0,0}$	32bit	RW	Coefficient for mixer input 0 to mixer output 0.
008_{16}	$Coeff_{1,0}$	32bit	RW	Coefficient for mixer input 1 to mixer output 0.
..	..	..	..	..
048_{16}	$Coeff_{17,0}$	32bit	RW	Coefficient for mixer input 17 to mixer output 0.
$04C_{16}$	$Coeff_{0,1}$	32bit	RW	Coefficient for mixer input 0 to mixer output 1.
..	..	..	..	..
630_{16}	$Coeff_{17,15}$	32bit	RW	Coefficient for mixer input 17 to mixer output 15.

The format of the coefficients is 16 bits unsigned placed in the 16 LSB of the 32bit entry. The coefficient is unsigned fix-point 2:14 meaning that the decimal point is between bit 13 and 14 giving a maximum gain of 4 (~12dB).

3.5 PEAK SPACE

The example below is for a 128 entry router as featured on TCD22xx. The peak detectors in the TCAT chips are part of the router. This result in each router entry having a 12 bit peak value. The interface returns the routing entry and the peak value to make it simpler to identify which channel the peak value belongs to.

Offset	Parameter	Size	Attribute	Function
000_{16}	$PEAK_0$	32bit	RO	Lower 16 bits contains the routing entry, bits 16..27 contains the 12 bit max absolute audio value since last read.
004_{16}	$PEAK_1$	32bit	RO	
..	..	..	..	
$4BC_{16}$	$PEAK_{127}$	32bit	RO	

3.6 NEW ROUTER SPACE

The example below is for a 128 entry router as featured on TCD22xx.

Offset	Parameter	Size	Attribute	Function
00_{16}	ROUTES	32bit	RW	Number of active routes in table.
04_{16}	$route_0$	32bit	RW	The 16 LSB contains a router word. For the format of router entries please refer to the TCD22xx User's Guide
08_{16}	$route_1$	32bit	RW	
..	..	..	..	
04_{16} + n	$route_n$	32bit	RW	

3.7 NEW STREAM CFG SPACE

Offset	Parameter	Size	Attribute	Function
00_{16}	NB_TX	32bit	RW	Number of Isoc Transmitters.
04_{16}	NB_RX	32bit	RW	Number of Isoc Receivers.
08_{16}	TX0_NB_AUDIO	32bit	RW	number of audio channels
$0C_{16}$	TX0_MIDI	32bit	RW	Number of MIDI channels (0-8)

Offset	Parameter	Size	Attribute	Function
10_{16}	TX0_NAMES	64 x 32bit	RW	Name string separated by '\', terminated with '\\'
110_{16}	TX0_AC3	32 bit	RW	A 1 in the bit field indicates that the corresponding channel pair is AC3 capable
114_{16}	TX1_NB_AUDIO	32bit	RW	number of audio channels
118_{16}	TX1_MIDI	32bit	RW	Number of MIDI channels (0-8)
$11C_{16}$	TX1_NAMES	64 x 32bit	RW	Name string separated by '\', terminated with '\\'
$21C_{16}$	TX1_AC3	32 bit	RW	A 1 in the bit field indicates that the corresponding channel pair is AC3 capable
..	..	..	..	..
08_{16} + NB_TX * 43_{16}	RX1_NB_AUDIO	32bit	RW	number of audio channels
$0C_{16}$ + NB_TX * 43_{16}	RX1_MIDI	32bit	RW	Number of MIDI channels (0-8)
10_{16} + NB_TX * 43_{16}	RX1_NAMES	32bit	RW	Name string separated by '\', terminated with '\\'
14_{16} + NB_TX * 43_{16}	RX1_AC3	32bit	RW	A 1 in the bit field indicates that the corresponding channel pair is AC3 capable
..	..	..	..	..

3.8 CURRENT CFG SPACE

Offset	Parameter	Size	Attribute	Function
0000_{16}	LOW_ROUTER	32bit	RO	Current routing for low rate mode. The format of this section is identical to the New Router Space above.
1000_{16}	LOW_STRM_CFG	32bit	RO	Current stream configuration for low rate mode. The format of this section is identical to the New Stream Cfg Space above.

Offset	Parameter	Size	Attribute	Function
2000_{16}	MID_ROUTER	32bit	RO	Current routing for mid rate mode. The format of this section is identical to the New Router Space above.
3000_{16}	MID_STRM_CFG	32bit	RO	Current stream configuration for mid rate mode. The format of this section is identical to the New Stream Cfg Space above.
4000_{16}	HIGH_ROUTER	32bit	RO	Current routing for high rate mode. The format of this section is identical to the New Router Space above.
5000_{16}	HIGH_STRM_CFG	32bit	RO	Current stream configuration for high rate mode. The format of this section is identical to the New Stream Cfg Space above.

3.9 STAND ALONE CFG SPACE

When the device is in stand alone mode there would typically not be any UI to rely on. For simple analog to analog connections this would be trivial, but with several digital interfaces involved more parameters are required.
A device in stand alone mode would use the routing and mixer setting stored in Flash.
Depending on how the device is clocked some extra parameters are needed. Each of the clock options are described below:

Source	Description	Extra settings	Extra settings
AES1	Specific AES Receiver	The device can automatically detect rates from 32kHz to 96kHz. A setting need to identify that the device is in HIGH mode.	AES_HIGH_RATE On Off
AES2			
AES3			
AES4			
AES_ANY	Auto-detect on any AES receiver		
ADAT	Clock from ADAT Receiver	ADAT uses the same carrier for all three ratemodes. An extra variable is needed to	ADAT_MODE Normal SMUX 2 SMUX 4

Source	Description	Extra settings	Extra settings
		select Normal, SMUX2 or SMUX 4 or auto-detect using user bits.	Auto
WC	Clock from WC BNC	If used for straight WC only no extra settings are required. In case of base-rate sync or Video sync a fractional number is needed.	WC_MUL 1-9999 WC_DIV 1-9999
Internal	Internally generated clock	An extra variable indicating the actual clock is needed.	INT_RATE 32 kHz 44.1 kHz 48 kHz 88.2 kHz 96 kHz 176.4 kHz 192 kHz

Offset	Parameter	Size	Attribute	Function
00_{16}	CLK_SRC	32bit	RW	Clock source used for stand alone mode. This field follows the DiceDriver clock source field.
04_{16}	AES_EXT	32bit	RW	Bit 0 indicates high rate mode. All other bits reserved for future use.
08_{16}	ADAT_EXT	32bit	RW	Bit 0..1 indicates mode. 00: Normal 01: SMUX II 10: SMUX Iv 11: Auto All other bits are reserved for future use.
$0C_{16}$	WC_EXT	32bit	RW	See below for bit definitions.
10_{16}	INT_EXT	32bit	RW	When internal mode is selected this field indicates actual rate. This field follows the DiceDriver nominal rate definition.

Offset	Parameter	Size	Attribute	Function
14_{16}-$3F_{16}$	Reserved	11x32bit	RO	Reserved for future options.

Definition of WC_EXT bitfield

Bit	Name	Meaning
0..1	MODE	The WC mode: 00: Normal WC 01: LOW 44.1k-48k use div/mul 10: MID 88.2k-96k use div/mul 11: HIGH 176.4k-192k use div/mul
4..15	WC_MUL	Numerator used to multiply the incoming clock to obtain the base rate.
16..31	WC_DIV	Denominator used to divide the incoming clock to obtain base rate.

The formula for the relation between the sample rate fs and the incoming clock is as follows:
$F_s = F_{wc}*(WC\_MUL+1)/(WC\_MUL+1)$

As an example:
NTSC, 48k (based on 29.97)
WC_MUL = 8008-1
WC_DIV = 5-1
And check:
$F_s = F_{wc}*8008/5 = 29.97*8008/5 = 48k$

3.10 APPLICATION SPACE

This space can be used for device specific control such as analog gains etc. It is entirely up to the manufacturer to define the content of this space. The firmware will be notified by changes and if Flash is enabled it will be stored with the other settings.

4 DICE Async. Capabilities

The DICE chips are able to handle payloads of 512 bytes (128 quadlets). Any write request with larger payload will result in multiple write transactions (Both Windows and OSX will split the transactions based on max receive size).
The DICE will not split large read transactions so no reads resulting in a response packet with a payload larger than 512 bytes should be issued.