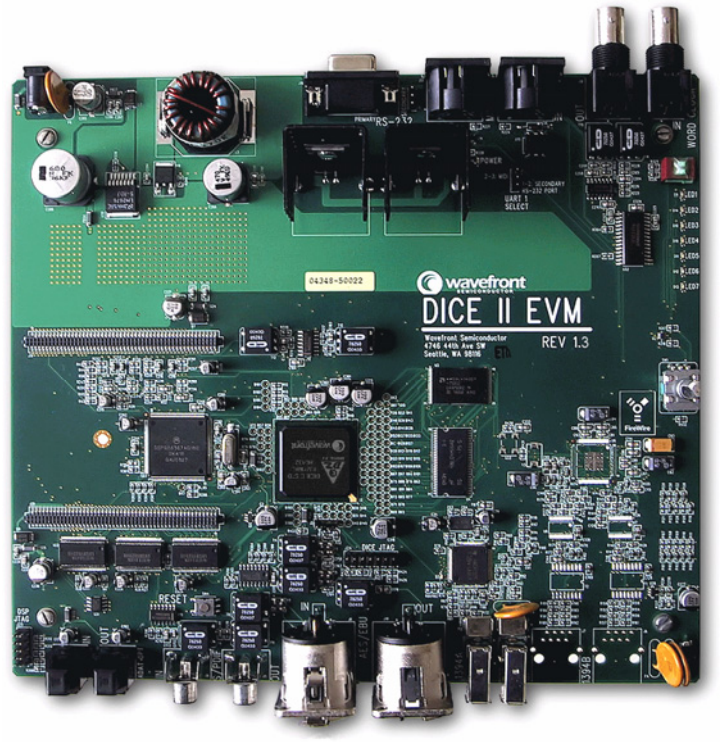
DICE II EVM
Manual



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Overview

EVM Features

FireWire
- IEEE 1394A via two 6-pin connectors
- IEEE 1394B via two CAT-5 connectors (not presently supported)

Audio Interfaces
- AES/EBU Input and Output
- SPDIF Input and Output
- ADAT Optical Input and Output
- Word Clock Input and Output
- MIDI Input and Output
- Optional expander card (AXM20) adds 20x20 analog and AES/EBU I/O channels, for total of 32x32 channels

Development Interfaces
- RS-232 Debug ports
- Expansion connectors
- Motorola DSP56367 to demonstrate typical DSP operation
- Headers and test points on all important signals

User Interface
- Eight LED's for indicating status
- Rotary grey-code encoder
- 2-bit DIP Switch

Power Supply
- Switching Power Supply accepts external power adapter or FireWire bus power

Connectors & User Controls

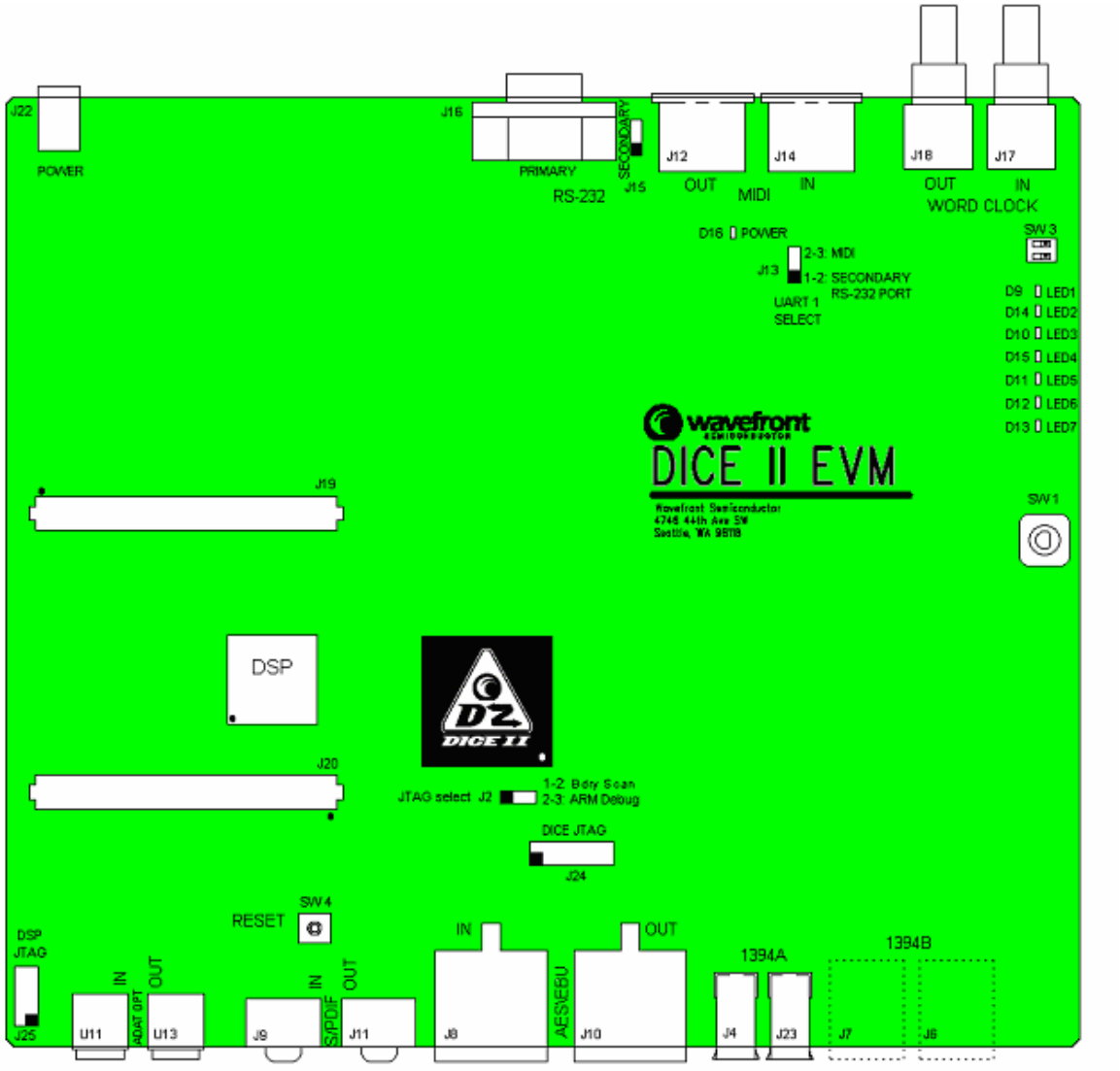

Figure 1 - ***DICE II EVM Top View***

Connector/Control	Component(s)	Description
Power Connector	J22	Plug your power adapter here. Since the EVM can be bus powered by FireWire, this power input is optional. D16 is the power indicator.
Primary RS-232 Connector	J16	Connect your PC COM port to this connector using the supplied serial cable. Run a terminal program (e.g. Hyper Terminal in Win XP) to access the DICE II Command Line Interpreter (CLI). The PC COM port must be set to: 115200 baud, N81 (no handshaking).
MIDI Interface	J12, J14	MIDI input and output connectors. MIDI input is dependent on the settings of header J13 and SW3.
Secondary RS-232 Connector	J15, J13	J15 is a three-terminal header that can be used to access the secondary UART on DICE II. RS-232 level shifting is provided on the EVM. Please use the supplied DB9/3-pin serial cable. This interface is used for debugging DICE II firmware via the GNU Debugger (GDB).
Word Clock Interface	J16, J17	These 75 ohm BNC connectors provide access to the Word Clock Input and Output on DICE II.
DIP Switch	SW3	Bit 1 of this DIP switch selects between MIDI or GDB debugging on the secondary UART. Bit 2 currently has no function.
LEDs	LED1 – LED7	These LED's indicated status of various functions on the EVM.
Rotary Encoder	SW1	This rotary encoder currently has no function. It is provided for future use, and serves as an example of how to properly connect grey code encoders to the DICE II.
IEEE1394b CAT-5 Interface	J6, J7	These connectors and the associated IEEE 1394B PHY are not mounted on this revision of the EVM.
FireWire Interface	J4, J23	Standard 6-pin IEEE 1394A connectors. Supports bus power (provides power to the FireWire bus if power adapter is plugged into J22; consumes bus power if no power adapter is plugged in). D16 is the power indicator.
AES3 (AES/EBU) Interface	J8, J10	AES3 input and output.
SPDIF (IEC 60958) Interface	J9, J11	SPDIF input and output.
ADAT Optical Interface	U11, U13	ADAT Optical input and output.
DSP JTAG	J25	JTAG port for the Motorola DSP56367 DSP.
DICE II JTAG	J24, J2	JTAG port for the DICE II. Primarily used for flashing a brand new unit. Not normally used for firmware development (serial debug via J15 using GNU GDB is favored over JTAG). J2 selects between Boundary Scan (shunt on pins 1-2) or debug (shunt on pins 2-3).
RESET Switch	SW4	Resets the EVM.
Expansion Connectors	J19, J20	These connectors carry important signals from DICE II to a "daughter card". Raw power from J22 or FireWire bus power is also present.

Table 1 – Connectors and User Controls

Theory of Operation

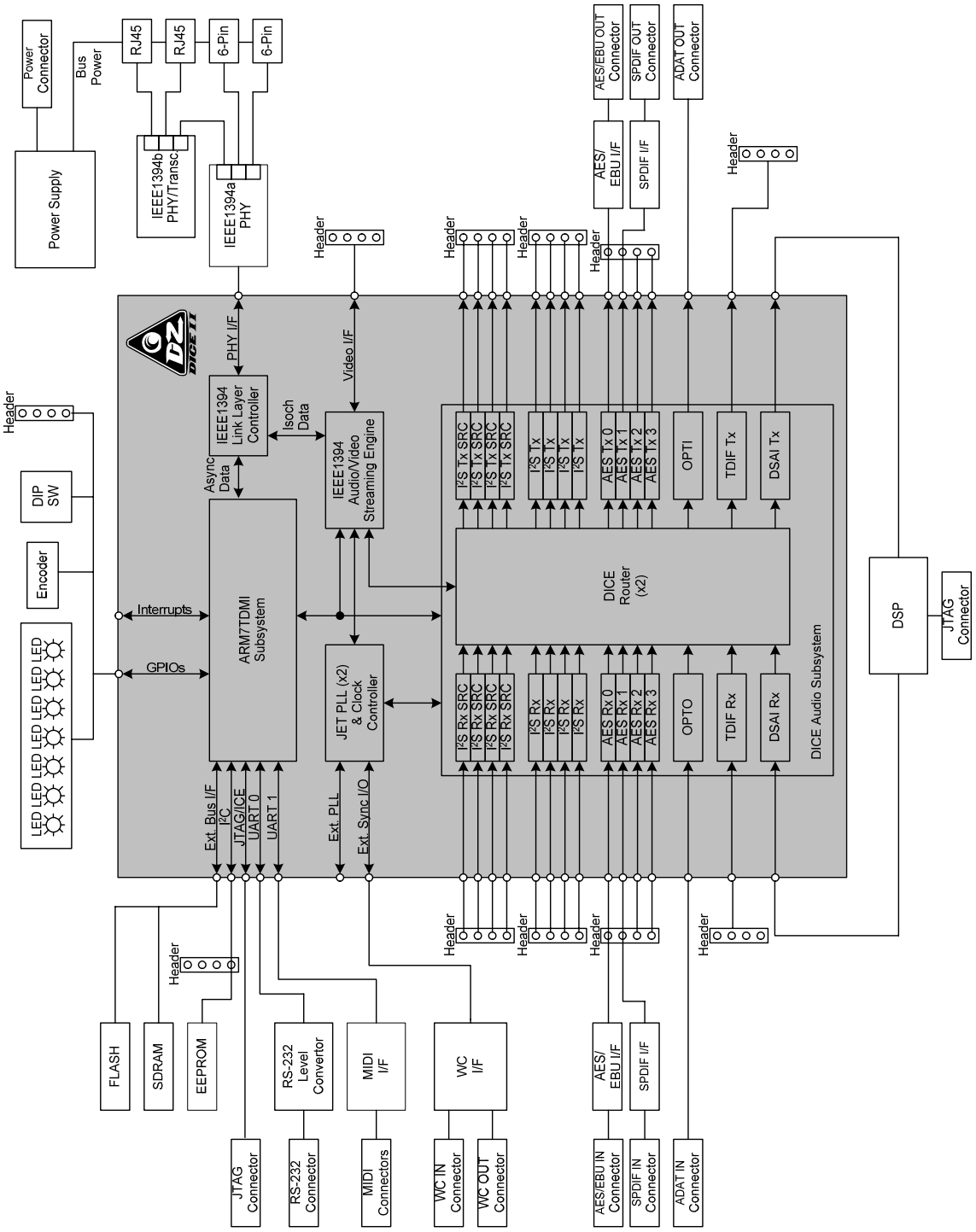

Figure 2 - *DICE II EVM Block Diagram*

Audio Interfaces

The DICE II EVM provides the following audio interfaces:

- SPDIF input and output via RCA connectors J9 & J11, connected to DICE II AES0 port.
- AES/EBU input and output via XLR connectors J8 & J10, connected to DICE II AES1 port.
- Two additional AES/EBU input and outputs are available via expansion connector J19. Note that XLR connectors must be interfaced to J19 by the user in order to access these extra AES/EBU signals.
- ADAT Optical input and output via optical transceivers U11 & U13, connected to the DICE II OPT I and OPTO ports.

MIDI Interface

The DICE II EVM has one MIDI interface, using DICE II UART1. This UART is also used for GDB debugging. Jumper J13 and DIP switch SW3 must be configured for MIDI operation or GDB as shown in Table 2 and Table 10:

J13	Shunt
MIDI	1-2
GDB Debug	2-3

Table 2 – J13 Settings for MIDI or GDB Debug

Note that the MIDI OUT connector will always carry data even if J13 is configured for GDB Debug mode, because J13 only selects the UART1 RX source.

Audio Expansion Connectors

Two high density expansion connectors (J19, J20) are provided for adding future daughter boards with additional features (e.g. I/O utilizing the 16-channel I2S ports). The mating connector for the daughter board is shown in Table 3:

Manufacturer	Model #
Samtec	TFM-150-32-S-D-LC

Table 3 - Mating Connector for J19/J20 Daughter Board Interface

The pin assignments of expansion connector J19 are shown in Table 4:

Pin #	Function	Pin #	Function *(DICE II Ball; type*; buffer)*
1	GND	2	n/c (factory testing only)
3	GND	4	n/c (factory testing only)
5	GND	6	n/c (factory testing only)
7	GND	8	n/c (factory testing only)
9	GND	10	n/c (factory testing only)
11	GND	12	n/c (factory testing only)
13	GND	14	n/c (factory testing only)
15	GND	16	n/c (factory testing only)
17	GND	18	n/c (factory testing only)
19	GND	20	n/c (factory testing only)
21	GND	22	n/c (factory testing only)
23	GND	24	n/c (factory testing only)
25	GND	26	n/c (factory testing only)
27	GND	28	n/c (factory testing only)
29	GND	30	n/c (factory testing only)
31	GND	32	n/c (factory testing only)
33	GND	34	VD7_TIEM_U1RI *(Ball W9; I/O; buffer U18A)*
35	GND	36	VD6_TIF1_U1DC_HFS2 *(Ball V9; I/O; buffer U18A)*
37	GND	38	VD5_TIF0_U1DS_HFS1 *(Ball U9; I/O; buffer U18-1)*
39	GND	40	VD4_TILR_U1CT *(Ball Y8; I/O; buffer U18-1)*
41	GND	41	VD3_TI3_U0RI *(Ball W8; I/O; buffer U18-1)*
43	GND	44	VD2_TI2_U0DC *(Ball V8; I/O; buffer U18-1)*
45	GND	46	VD1_TI1_U0DS *(Ball Y7; I/O; buffer U18-1)*
47	GND	48	VD0_TI0_U0CT *(Ball W7; I/O; buffer U18-1)*
49	GND	50	VFSY_TO0_U1DT *(Ball Y9; I/O; buffer U18-2)*
51	GND	52	VRDY_TO1_U1RT *(Ball W10; I/O; buffer U18-2)*

53	GND		54	VCLK_TO2_U1O1 *(Ball V10; I/O; buffer U18-2)*	
55	GND		56	VEDB_TO3_U1O2 *(Ball Y10; I/O; buffer U18-2)*	
57	GND		58	VVAL_TOLR_U0DT *(Ball Y11; I/O; buffer U18-2)*	
59	GND		60	GP15_TOEM_U0O2_WCKO *(Ball U11; I/O; buffer U18-2)*	
61	GND		62	GP14_TOF1_U0O1_WCKI *(Ball V11; I/O; buffer U18-2)*	
63	GND		64	GP13_TOF0_U0RT_BLKS *(Ball W11; I/O; buffer U18-2)*	
65	GND		66	AESR0 *(Ball W15; I; buffer U19-1)*	
67	GND		68	AESR1 *(Ball Y16; I; buffer U19-1)*	
69	GND		70	AESR2 *(Ball U14; I; buffer U19-1)*	
71	GND		72	AESR3 *(Ball V15; I; buffer U19-1)*	
73	GND		74	OPTI *(Ball W14; I; buffer U19-1)*	
75	GND		76	AEST0 *(Ball W16; O; buffer U19-2)*	
77	GND		78	AEST1 *(Ball Y17; O; buffer U19-2)*	
79	GND		80	AEST2 *(Ball V16; O; buffer U19-2)*	
81	GND		82	AEST3 *(Ball W17; O; buffer U19-2)*	
83	GND		84	OPTO *(Ball Y14; O; buffer U19-2)*	
85	POWER (8-40VDC) Raw input from external power supply or FireWire bus power.		86	AESR3_P	*(Ball V15; I; differential receiver U9)*
87			88	AESR3_N	
89			90	AESR2_P	*(Ball U14; I; differential receiver U9)*
91			92	AESR2_N	
93			94	AEST2_P	*(Ball V16; O; differential buffer U12)*
95			96	AEST2_N	
97			98	AEST3_P	*(Ball W17; O; differential buffer U12)*
99			100	AEST3_N	

Table 4 – J19 Pinout

(*I/O types are from perspective of DICE II chip)

J19 Notes

1) Unregulated power from the FireWire bus power / power input jack is available on pins 85, 87, 89, … 99. It should be regulated on a daughter board to ensure that widely varying FireWire bus power does not damage circuitry on the daughter board.
2) Pins 2, 4, 6, … 32 are for factory testing only and should be left unconnected.
3) Pins 34, 36, 38, … 58 provide access to the DICE II video and TDIF interfaces, and UART handshaking signals. Dual bank buffer U18 controls the direction of the signals. Bank 1 (U18-1) can be configured to input or output some of these signals to/from the daughter board, or to disable the signals, by installing 0-ohm resistors for R251 & R252 as shown in
4) Table 5. Bank 1 (U18-2) can be configured to input or output the remainder of these signals via R249 & R250 as shown in
5) Table 6. Attention should be paid to the entire set of signals assigned to each bank of U18 when configuring the buffer for a particular signal to ensure that the other signals assigned to the same bank do not contend with other signals on the EVM. If the group of signals in a bank must be configured for different directions, then U18 should be removed from the PCB and resistors R362-R377 should be installed (22 ohms recommended) as required to connect signals to J19 (see DICE II EVM Schematic Diagram).
6) Pins 60, 62 provide access to DICE II multifunction pins with GPIO, WORD CLOCK, TDIF, and UART signals. The EVM is configured for WORD CLOCK operation, buffered by U17. Therefore, if the signals on pins 60 & 62 are required by a daughter board, the WORD CLOCK functions on the EVM PCB should be disabled by removing U17.
7) Pins 66, 68, 70, … 84 provide access to the DICE II AES receive/transmit and ADAT Optical ports. The EVM PCB is configured for SPDIF I/O on AESR0/AEST0 and AES/EBU I/O on AESR1/AEST1, respectively. Additional circuitry is present on the EVM for interfacing AES/EBU balanced signals to AESR2/AEST2 and AESR3/AEST3 via J19 pins 86, 88, 90, … 100. Dual bank buffer U19 allows a daughter board to send/receive AES/EBU to the DICE II chip. Bank 1 (U19-1) controls the direction of the AESRx and OPTI signals. Bank 2 (U19-2) controls the direction of AESTx and OPTO signals. U19-1 and U19-2 is configured by installing resistors R260-R263 as shown in
8) Table 7 and
9) Table 8. Attention should be paid to the entire set of signals assigned to each bank of U19 when configuring the buffer for a particular signal to ensure that the other signals assigned to the same bank do not contend with other signals on the EVM. If the group of signals in a bank must be configured for different directions, then U19 should be removed from the PCB and resistors R378-R387 should be installed (22 ohms recommended) as required to connect signals to J19 (see DICE II EVM Schematic Diagram).
10) All signals on J19 are 3.3V LVCMOS.

U18-1	Input from J19	Output to J19	Disable Signals
Add 0-ohm resistors to:	R251, R252	R251	
Leave open:		R252	R251, R252 (default)

Table 5 – Buffer U18-1 configuration

U18-2	Input from J19	Output to J19	Disable Signals
Add 0-ohm resistors to:	R249, R250	R249	
Leave open:		R250	R249, R250 (default)

Table 6 – Buffer U18-2 configuration

U19-1	Input from J19	Output to J19	Disable Signals
Add 0-ohm resistors to:	R262, R263	R262	
Leave open:		R263	R262, R263 (default)

Table 7 – Buffer U19-1 configuration

U19-2	Input from J19	Output to J19	Disable Signals
Add 0-ohm resistors to:	R260, R261	R260	
Leave open:		R261	R260, R261 (default)

Table 8 – Buffer U19-2 configuration

The pin assignments of expansion connector J20 are shown in Table 9:

Pin #	Function *(DICE II Ball; type*; buffer)*	Pin #	Function
1	I2S_RX0_D0 *(Ball B17; I; buffer U20-1)*	2	GND
3	I2S_RX0_D1 *(Ball C17; I; buffer U20-1)*	4	GND
5	I2S_RX0_D2 *(Ball D16; I; buffer U20-1)*	6	GND
7	I2S_RX0_D3 *(Ball A18; I; buffer U20-1)*	8	GND
9	I2S_RX1_D0 *(Ball E19; I; buffer U20-1)*	10	GND
11	I2S_RX1_D1 *(Ball D20; I; buffer U20-1)*	12	GND
13	I2S_RX2_D0 *(Ball H19; I; buffer U20-1)*	14	GND
15	I2S_RX2_D1 *(Ball H18; I; buffer U20-1)*	16	GND
17	I2S_RX0_MCK *(Ball A20; O; buffer U20-2)*	18	GND
19	I2S_RX0_BCK *(Ball A19; O; buffer U20-2)*	20	GND

21	I2S_RX0_LRCK *(Ball B18; O; buffer U20-2)*	22	GND
23	I2S_TX0_D0 *(Ball C19; O; buffer U20-2)*	24	GND
25	I2S_TX0_D1 *(Ball B20; O; buffer U20-2)*	26	GND
27	I2S_TX0_D2 *(Ball C18; O; buffer U20-2)*	28	GND
29	I2S_TX0_D3 *(Ball B19; O; buffer U20-2)*	30	GND
31	I2S_RX1_MCK *(Ball E20; O; buffer U20-2)*	32	GND
33	I2S_RX1_BCK *(Ball G17; O; buffer U21-1)*	34	GND
35	I2S_RX1_LRCK *(Ball F18; O; buffer U21-1)*	36	GND
37	I2S_TX1_D0 *(Ball G18; O; buffer U21-1)*	38	GND
39	I2S_TX1_D1 *(Ball F19; O; buffer U21-1)*	40	GND
41	I2S_TX1_MCK *(Ball G20; O; buffer U21-1)*	41	GND
43	I2S_TX1_BCK *(Ball G19; O; buffer U21-1)*	44	GND
45	I2S_TX1_LRCK *(Ball F20; O; buffer U21-1)*	46	GND
47	I2S_RX2_MCK *(Ball J18; O; buffer U21-1)*	48	GND
49	I2S_RX2_BCK *(Ball J17; O; buffer U21-2)*	50	GND
51	I2S_RX2_LRCK *(Ball H20; O; buffer U21-2)*	52	GND
53	I2S_TX2_D1 *(Ball J19; O; buffer U21-2)*	54	GND
55	I2S_TX2_D0 *(Ball J20; O; buffer U21-2)*	56	GND
57	I2S_TX0_MCK *(Ball C20; O; buffer U22-1)*	58	GND
59	I2S_TX0_BCK *(Ball E17; O; buffer U22-1)*	60	GND
61	I2S_TX0_LRCK *(Ball D18; O; buffer U22-1)*	62	GND
63	I2S_TX2_MCK *(Ball K19; O; buffer U22-2)*	64	GND
65	I2S_TX2_BCK *(Ball K18; O; buffer U22-2)*	66	GND
67	I2S_TX2_LRCK *(Ball K17; O; buffer U22-2)*	68	GND
69	EFBR *(Ball Y15; I/O; unbuffered)*	70	GND
71	EHBR *(Ball V14; I/O; unbuffered)*	72	GND
73	NLIG *(Ball C9; I; unbuffered)*	74	GND
75	PLLE *(Ball B9; I; unbuffered)*	76	GND

77	HPX3 *(Ball L18; I/O; unbuffered)*	78	GND
79	HPX2 *(Ball L20; O; unbuffered)*	80	GND
81	HPX1 *(Ball K20; O; unbuffered)*	82	GND
83	I2CD *(Ball C5; I/O; unbuffered)*	84	POWER (8-40VDC) Raw input from external power supply or FireWire bus power.
85	I2CC *(Ball A4; I/O; unbuffered)*	86	
87	BNK3_GP3_EN3B *(Ball V3; I/O; unbuffered)*	88	
89	RESET *(Ball A9; I; unbuffered)*	90	
91	*reserved*	92	
93	*reserved*	94	
95	*reserved*	96	
97	*reserved*	98	
99	*reserved*	100	

Table 9 – J20 Pinout

(*I/O types are from perspective of DICE II chip)

J20 Notes

1) Unregulated power from the FireWire bus power / power input jack is available on pins 84, 86, 88, … 100. It should be regulated on a daughter board to ensure that widely varying FireWire bus power does not damage circuitry on the daughter board.
2) Pins 1, 3, 5, ..15 are buffered by bank 1 of U20 (U20-1). The output enable of U20-1 is controlled by resistor R269. By installing a 0-ohm resistor (or short circuit) for R269 the buffer will be enabled. It is shipped from the factory uninstalled (R269 is not installed, buffer is disabled).
3) Pins 17, 19, 21, … 31 are buffered by bank 2 of U20 (U20-2). The output enable of U20-2 is controlled by resistor R271. By installing a 0-ohm resistor (or short circuit) for R271 the buffer will be enabled. It is shipped from the factory uninstalled (R271 is not installed, buffer is disabled).
4) Pins 33, 35, 37, … 47 are buffered by bank 1 of U21 (U21-1). The output enable of U21-1 is controlled by resistor R277. By installing a 0-ohm resistor (or short circuit) for R277 the buffer will be enabled. It is shipped from the factory uninstalled (R277 is not installed, buffer is disabled).
5) Pins 49, 51, 53, 55 are buffered by bank 2 of U21 (U21-2). The output enable of U22-2 is controlled by resistor R279. By installing a 0-ohm resistor (or short circuit) for R279 the buffer will be enabled. It is shipped from the factory uninstalled (R279 is not installed, buffer is disabled).
6) Pins 57, 59, 61 are buffered by bank 1 of U22 (U22-1). The output enable of U22-1 is controlled by resistor R290. By installing a 0-ohm resistor (or short

circuit) for R290 the buffer will be enabled. It is shipped from the factory uninstalled (R20 is not installed, buffer is disabled).

7) Pins 63, 65, 67 are buffered by bank 2 of U22 (U22-2). The output enable of U22-2 is controlled by resistor R292. By installing a 0-ohm resistor (or short circuit) for R292 the buffer will be enabled. It is shipped from the factory uninstalled (R22 is not installed, buffer is disabled).
8) All signals on J20 are 3.3V LVCMOS.

1394a Interface

The EVM provides 2 standard 6-pin IEEE1394a connectors (J4, J23). A Texas Instruments TSB41AB3 PHY chip is used for bus arbitration. This PHY chip is connected to the DICE II PHY/LINK interface pins without galvanic isolation. The 6-pin connectors support IEEE 1394 bus power in "alternate power provider" mode.

1394b CAT 5 Interface

The EVM was designed to support IEEE1394B CAT 5 using the new Texas Instruments TSB41BA3 "1394B PHY" and TSB17BA1 UTP transceivers. However, testing has revealed some problems with this early TI CAT5 transceiver silicon and consequently, the 1394B silicon and RJ45 connectors were not mounted on this version of the DICE II EVM. Please contact us if you wish to experiment with this exciting technology and we will guide you through the known problems with the TI silicon.

DSP

The DICE II EVM has a Motorola DSP56367 to demonstrate typical interfacing between a host processor and the DICE II. Currently the DSP is not being utilized, but future upgrades to the EVM will include DSP software for processing audio via the DICE II DSAI interface.

User Interface Controls

LED's

The DICE II EVM has seven LED's (labeled LED1 – LED7) for indicating board status. The LED functions are listed in Table 10.

LED	Function
LED1	Lit when clock domain 0 is locked
LED2	Toggles whenever there is a 1394 cycle timer second interrupt
LED3	Lit when a PC driver has enabled isochronous streaming
LED4	Lit when a PC driver has attached to the EVM
LED5	Lit whenever the AES receiver is locked
LED6	Lit whenever the ADAT receiver is locked
LED7	Lit whenever the TDIF receiver is locked

Table 10 – LED Functions

DIP Switch

The DICE II EVM has a 2-bit DIP switch (SW3) that demonstrates how to connect switches to GPIO on the DICE II. Bit #1 of SW3 (SW3-1) selects whether the secondary UART on the DICE II chip is configured for MIDI or GDB debugging, as specified in Table 11. Bit #2 of SW3 (SW3-2) is not currently used.

SW3-1	Function
OFF	Secondary UART is configured for MIDI
ON	Secondary UART is configured for GDB

Table 11 – SW3-1 Functions

Rotary Encoder

The DICE II EVM has a rotary grey code encoder (with integrated push switch) to demonstrate how to connect to the encoder inputs on the DICE II. The push switch is connected to GPIO GP3. Currently the encoder has no function.

Memory

The DICE II EVM has the following types of memory connected to the DICE II:

- 1Mbit x 16 FLASH (AMD AM29LV160DT-70; U3)
- 4Mbit x 16 SDRAM (Samsung K4S641632F-TC75; U4)
- 16Kbit serial EEPROM (Atmel T24C16A; U31)

FLASH and SDRAM are used by the DICE II ARM for firmware. In the future, DSP firmware images will also reside in FLASH and be booted into the DSP by the ARM.

The DICE II firmware image currently occupies approximately 750KB of FLASH. The firmware is not yet optimized for minimal code size, and the sector size in the FLASH file system is relatively large, so the firmware could realistically be optimized to fit into about 500KB of FLASH space.

The serial EEPROM is not currently used, but may be employed in the future to store parameter settings. It is provided as an illustration of how to use the DICE II I2C interface.

Power Supply

The DICE II EVM power supply is designed to support FireWire bus power or power from an external “wall wart” power supply. The power supply is a multistage design. The first stage is a DC-DC converter (U30) designed for 8-40VDC input and 5VDC output. Low dropout linear regulators convert the 5V to 3.3VDC and 1.8VDC required by on-board logic.

The power input is limited to 1.6A by a self resetting fuse. The typical current draw from a 12VDC power input under normal operating conditions (DICE II streaming audio bidirectionally on the FireWire bus, AES/EBU, SPDIF, and ADAT ports active) is 280mA.

Software Development

The DICE II EVM serves as an excellent platform for developing DICE II firmware. The EVM provides several debug ports for software development:

GDB Debug Port

The preferred tool for debugging DICE II firmware is the GNU GDB debugger. This debugger interfaces to DICE II via J15, a three-pin header connected to the DICE II secondary UART (UART1). Please use the supplied DB9/3-pin serial cable for interfacing to this port. RS-232 level shifting is provided on-board the EVM. Note that this secondary UART is shared with the MIDI function. To enable RS-232 debug please place a shunt over pins 1-2 of J13, and set DIP SW SW3-1 to the ON position. For MIDI operation, please place the shunt over pins 2-3 of J13, and set DIP SW SW3-1 to the OFF position.

For more information on the GNU GDB debugger, and DICE II firmware development, please consult the DICE II Software Developer's Kit.

Command Line Interface

The Command Line Interpreter (CLI) allows you to access DICE II registers and to configure its basic functions (e.g. configure audio routing, clock settings, FireWire transmission, etc.) via a PC terminal program such as Hyper terminal. The CLI is provided via DB9 connector J16 and DICE II UART0. Communications settings are 11520 baud, N81 (no handshaking). Details about the CLI commands can be found in the *DICE II Command Line Interface Reference* which is file name **DICE_Firmware_CLI_Ref.pdf**.

The CLI provides context sensitive help. Simply type a question mark '?' in place of the parameters in a command and you will be given a list of options for that command (e.g. " **dice.clock ?** " will return a list of possible clock source arguments for the **dice.clock** command).

JTAG Port

The DICE II JTAG port is primarily used to load an empty FLASH with its first image on a new PCB. The JTAG port is not required for software development – the preferred method of debugging software during development is via the serial GDB debugger.
Please note that there are two standard pin-outs for ARM JTAG connectors: a 14-pin connector, and a 20-pin connector. The JTAG connector on the DICE II EVM (J24) is wired per the ARM 14-pin JTAG standard (see Table 12 below).

ARM 14-Pin JTAG Connector Specification 2x7 header, 0.10" spacing	
Pin #	**Signal**
1	VTRef
2	GND
3	nTRST
4	GND
5	TDI
6	GND
7	TMS
8	GND
9	TCK
10	GND
11	TDO
12	nSRST
13	VTRef
14	GND

Table 12 – DICE II ARM JTAG Connector Pin-out

(Note – Please see DICE II EVM schematic, or ARM JTAG reference, for pin numbering convention on JTAG connector J24)

JTAG Debug Probe

The EVM ships with firmware already loaded in FLASH. Firmware may be updated using the RedBoot file system via RS-232. Therefore, it is not necessary for users to purchase a JTAG probe to update firmware or to do development. However, if you wish to use a JTAG emulator with the DICE II EVM, we recommend the following device:

Vendor	Model #
Embedded Performance, Inc. 606 Valley Way Milpitas, CA 95035 408-719-5621	MAJIC-LT JTAG Debug Probe [ARM14-CK Cable option]

Boundary Scan versus ARM Debugging

The DICE II JTAG port supports IEEE1149.1 boundary-scan in addition to ARM debugging. Jumper J2 selects between boundary-scan and ARM debug (see Table 13).

J2 Shunt	JTAG Function
Pins 1-2	Boundary Scan
Pins 2-3	ARM Debug

Table 13 – J2 JTAG Configuration

Software Development Kit

TCAT offers a software development kit (SDK) for DICE II that includes source code, GNU development tools, and documentation of the DICE II firmware APIs and CLI. This SDK is free of charge, but requires a license agreement governing its use. Please contact TCAT to obtain the SDK.

Loading new Firmware

New firmware can be loaded onto the DICE II EVM using the J28 CLI serial port. For instructions, please refer to TCAT document "*DICE II EVM Procedure for Updating RedBoot and DICE Application Firmware*" which is file name **EVM_FW_Update.pdf**.