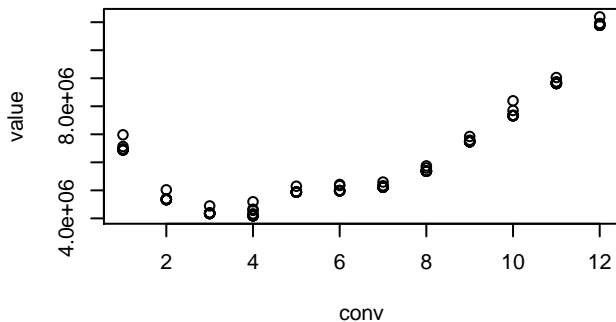
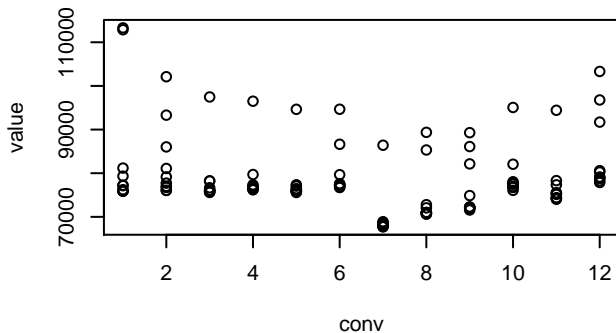


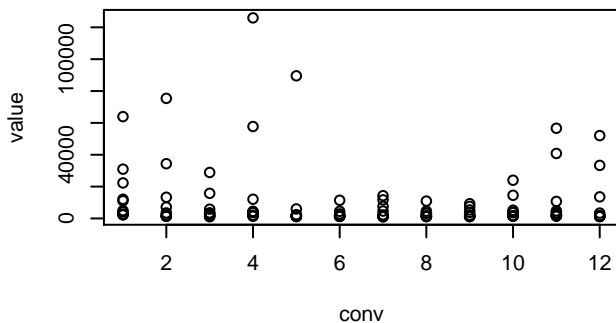
Cache access



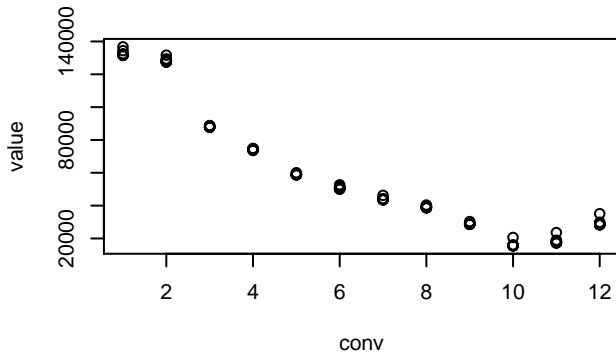
Cache misses



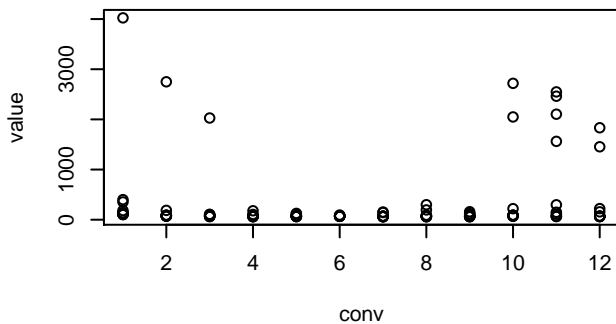
Instruction cache misses



TLB data misses



TLB instruction misses



Total cycles

