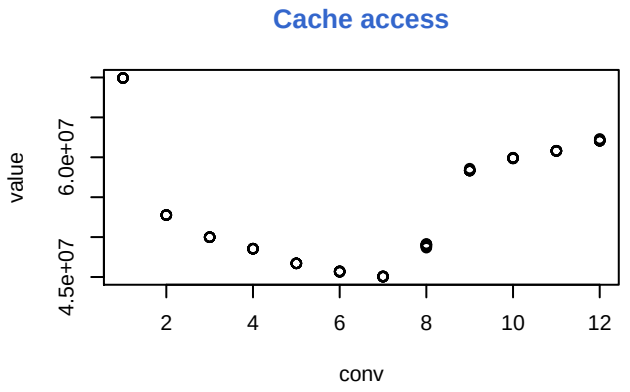
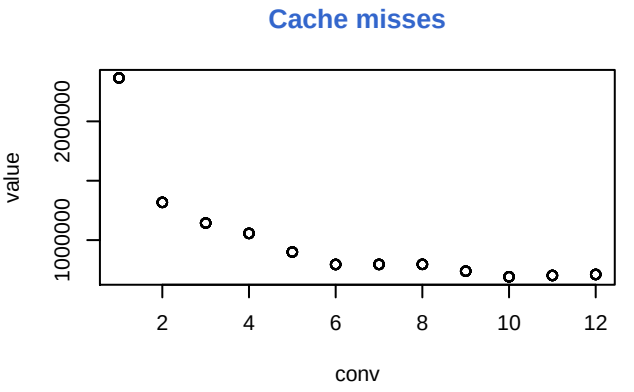
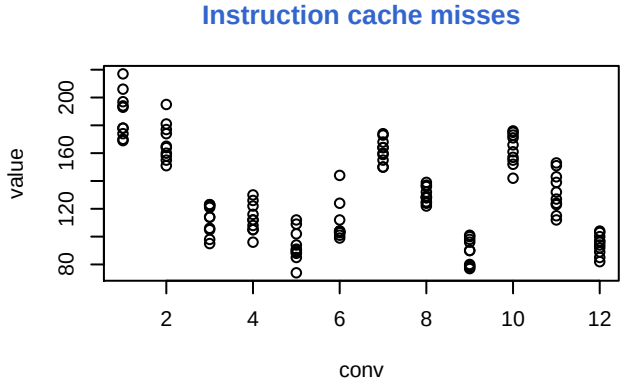
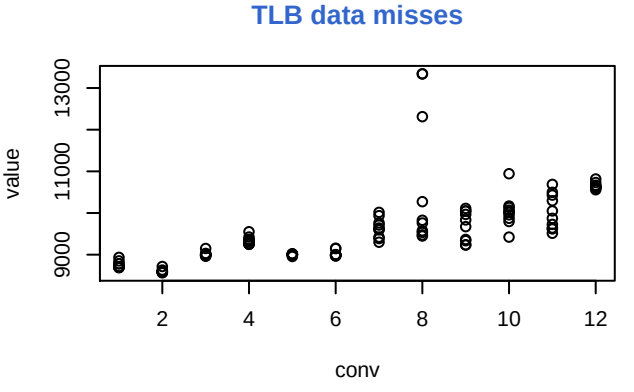
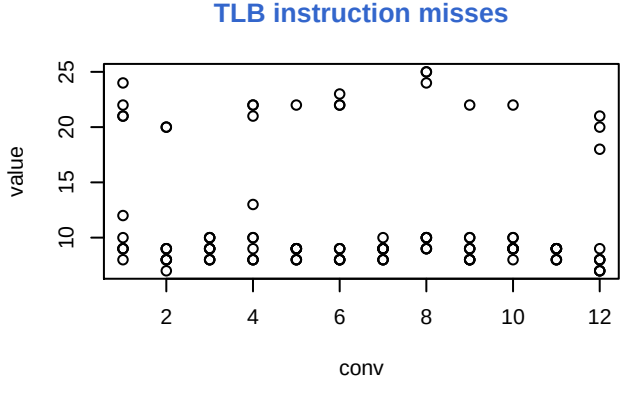
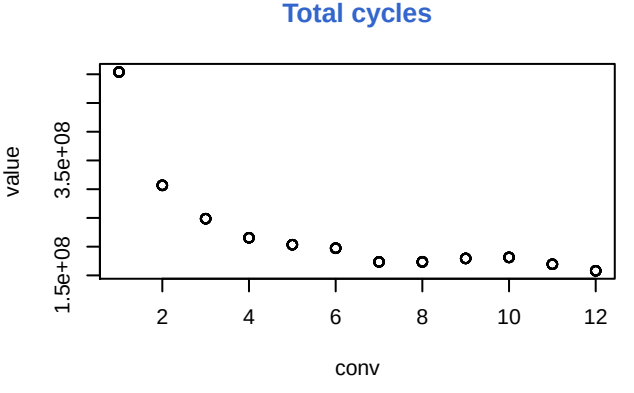

Cache access
value
4.5e+07
6.0e+07
2
4
6
8
10
12
conv


Cache misses
value
1000000
2000000
2
4
6
8
10
12
conv


Instruction cache misses
value
80
120
160
200
2
4
6
8
10
12
conv


TLB data misses
value
9000
11000
13000
2
4
6
8
10
12
conv


TLB instruction misses
value
10
15
20
25
2
4
6
8
10
12
conv


Total cycles
value
1.5e+08
3.5e+08
2
4
6
8
10
12
conv