# Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

*Bachelor of Technology*
*in*
*Electronics and Communication Engineering*

by

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# Chapter *1*

# Experiment - 8

## 1.1 Aim of the Experiment

Sequential system design using state Machines

A. Write a VHDL code of mod 4 up/down counter using state machines. The counter has a Reset signal to reset the current count to 0, another control signal count to decide the up or down count. If count =0, then it acts like up counter and as a down counter for count=1.Output of the counter is current state of the machine. Show at least 20 clock cycles in your testbench.
B. Write a VHDL code for a sequential system using state machine which recognizes the pattern 1101 in a sequence of 0's and 1's. The system has a input x and output z. z is 1 if x(t-3,t) = 1101, else 0. Show at least 4 detections of pattern 1101 in your testbench.

## 1.2 Theory

A finite-state machine (FSM), or simply a state machine, is a mathematical model of computation. It is an abstract machine that can be in exactly one of a finite number of states at any given time. The FSM can change from one state to another in response to some external inputs; the change from one state to another is called a transition. An FSM is defined by a list of its states, its initial state, and the conditions for each transition.

The behavior of state machines can be observed in many devices in modern society that perform a predetermined sequence of actions depending on a sequence of events with which they are presented. Examples are vending machines, which dispense products when the proper combination of coins is deposited, elevators, whose sequence of stops is determined by the floors requested by riders, traffic lights, which change sequence when cars are waiting, and combination locks, which require the input of combination numbers in the proper order. The largest use of finite state machines is as a mathematical model for designing digital logic circuits and computer programs.

## 1.3 Coding Techniques used

DATA FLOW method - It describes the flow of data, the circuit is described using concurrent statements, each of the concurrent statements is woken up by changes on its input and delivers its output.

BEHAVIORAL method - It describes circuit in its behaviour, it describes how the output is derived from the input using structured statements Circuit is described using an input output relationship using sequential statements inside a process.

STRUCTURAL method - It consists number of building blocks like gates, multiplexers etc. It describes how gates are interconnected similar to schematic approach.

## 1.4 Simulation and Results

### 1.4.1 4-bit Up and Down Counter

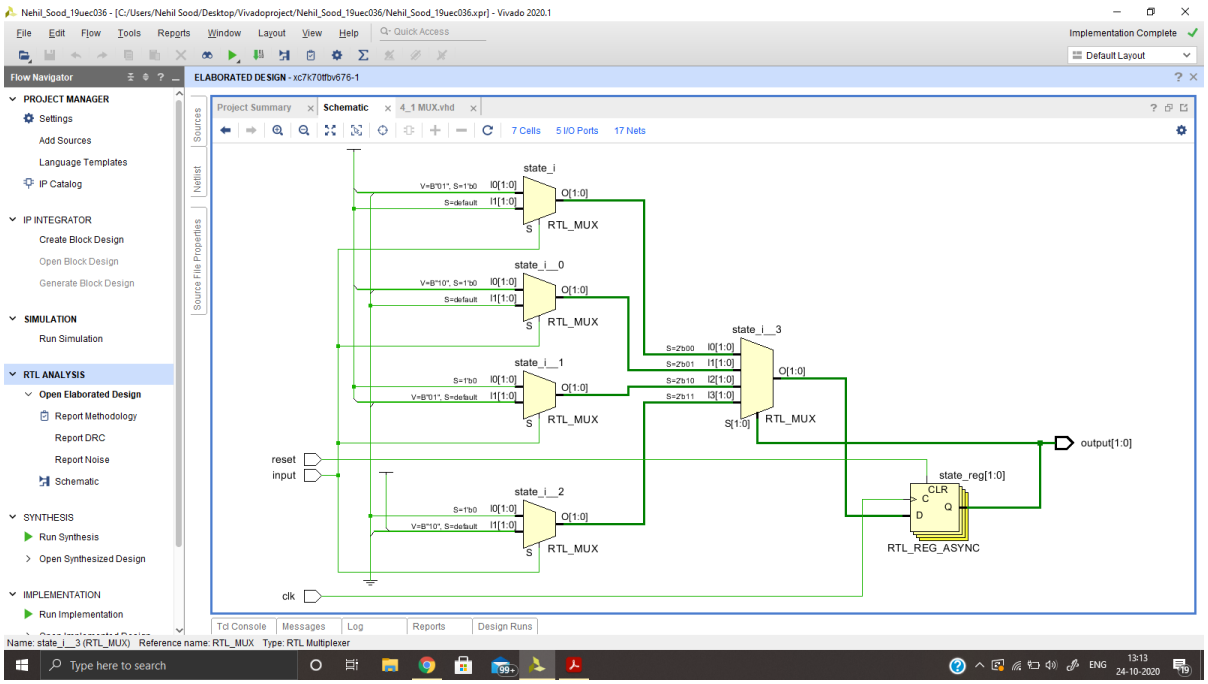


**Figure 1.1** Schematic of the 4-bit Up and Down Counter

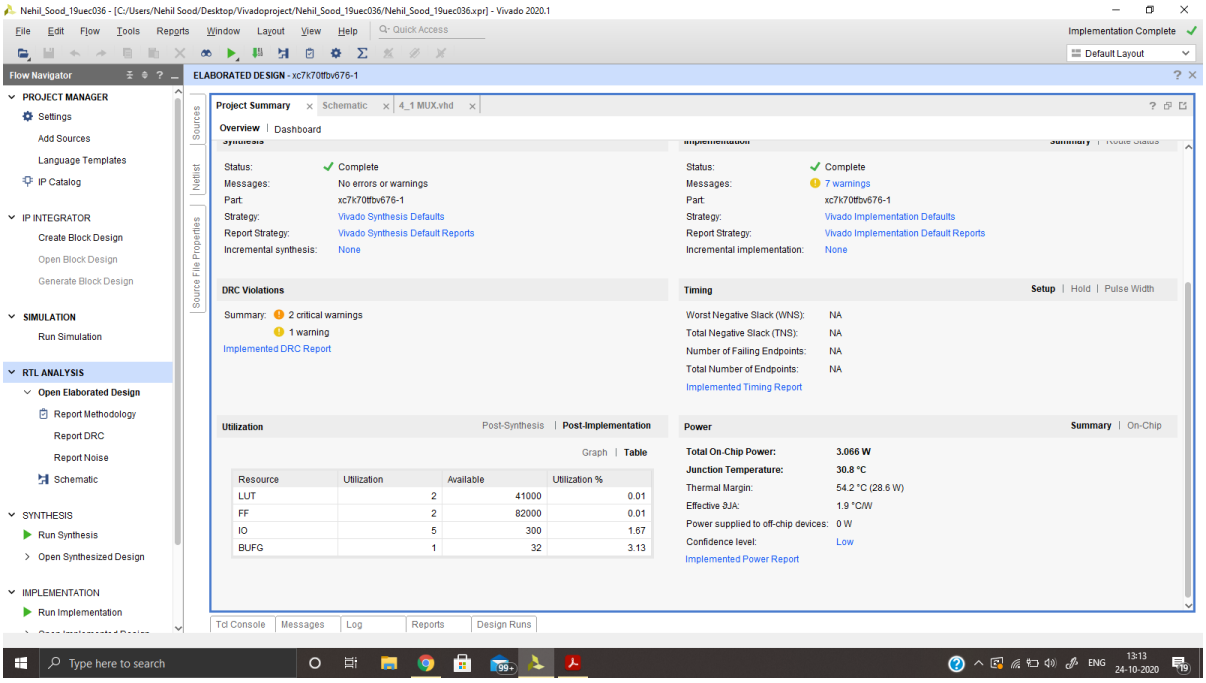


**Figure 1.2** Project Summary of the 4-bit Up and Down Counter

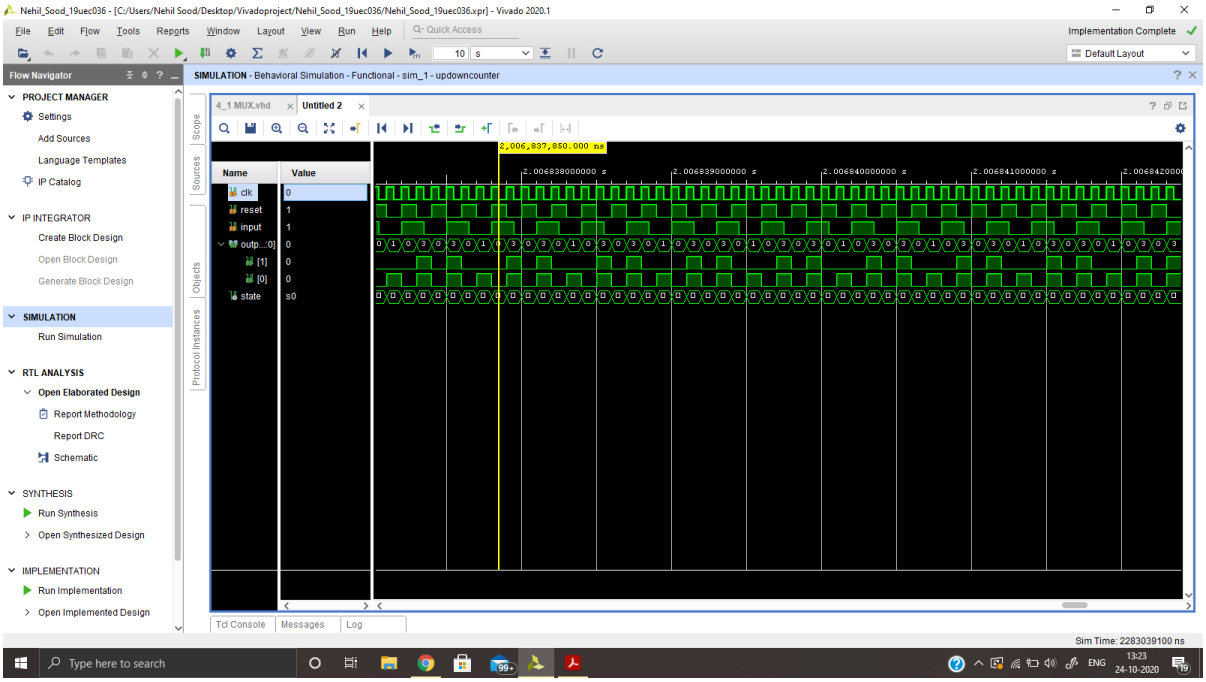


**Figure 1.3** Simulation of the 4-bit Up and Down Counter

### 1.4.2 Sequence Detector

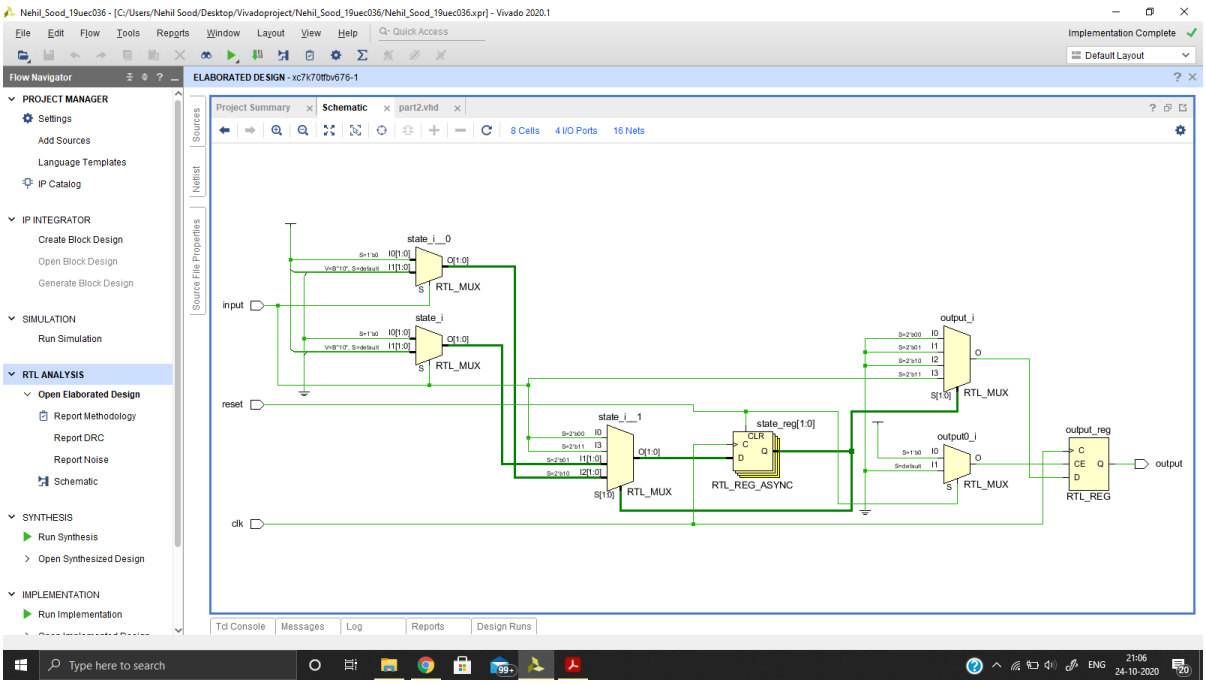


**Figure 1.4** Schematic of the Sequence Detector

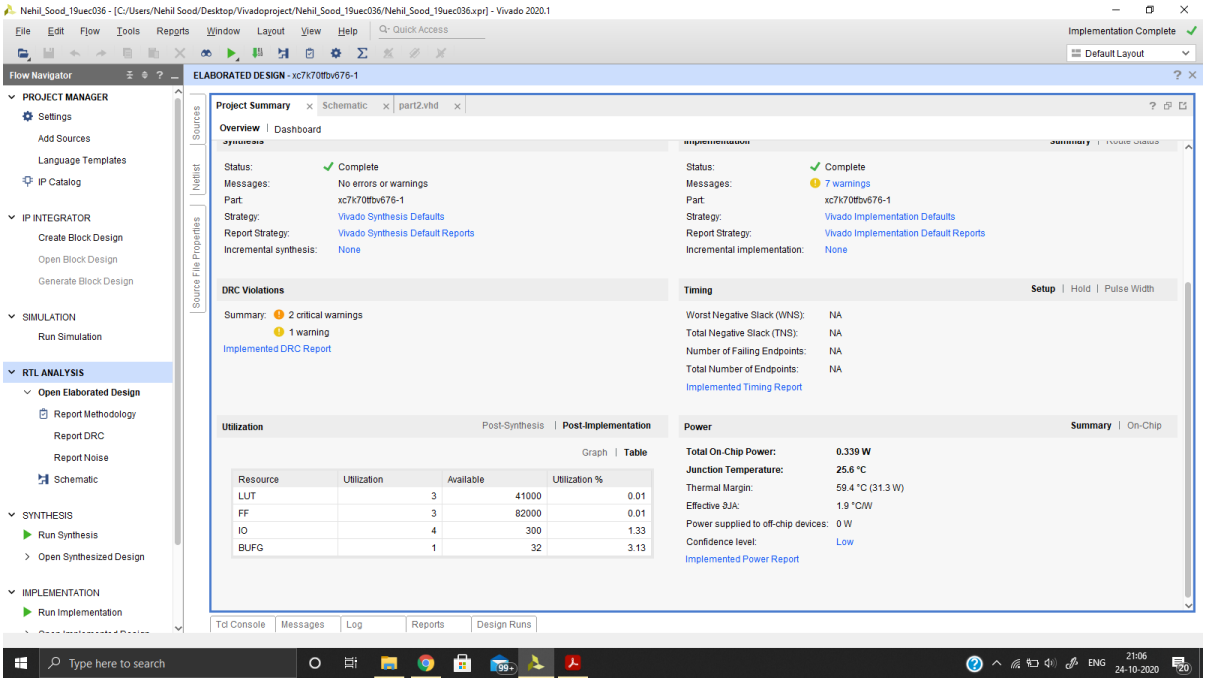


**Figure 1.5** Project Summary of the Sequence Detector

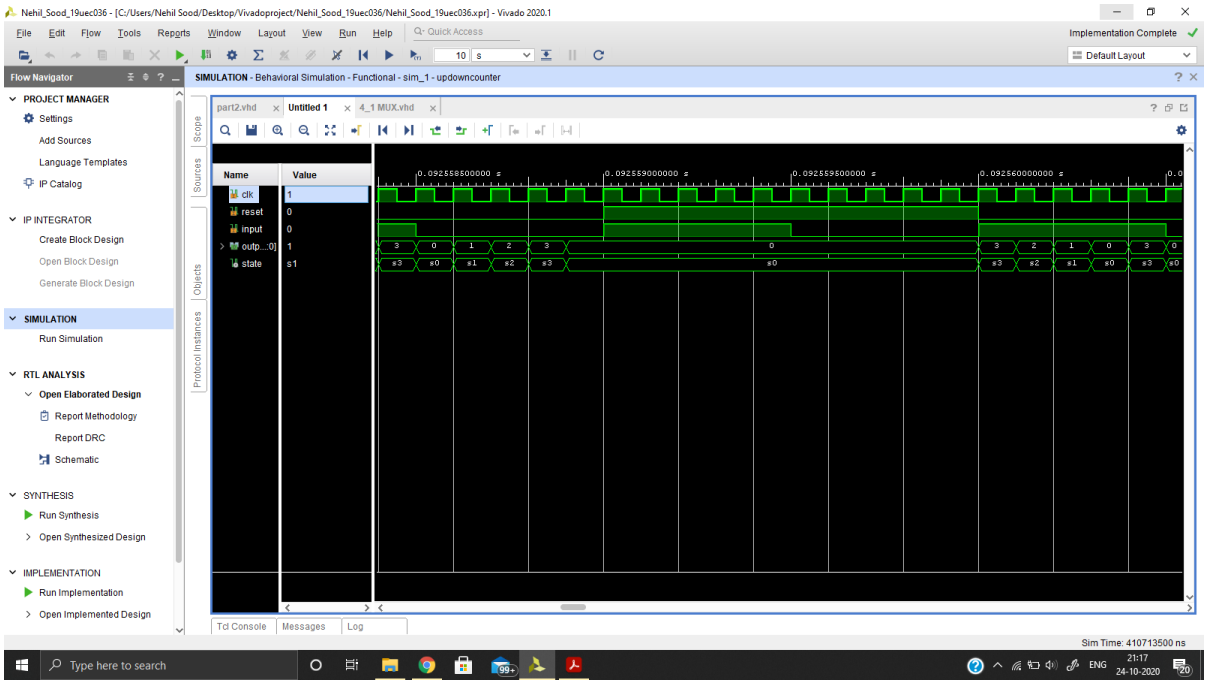


**Figure 1.6** Simulation of the Sequence Detector

## 1.5 Summary

| Name of the Entity | No. of LUT used | Total On Chip Power |
|---|---|---|
| Mod 4 up/down counter using state machines | 2 | 3.066W |
| Sequential system using state machine | 3 | 0.339W |

**Table 1.1** Comparison of Area and power requirements for different kinds of adders.