Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor of Technology
in
Electroincs and Communication Engineering

by

Nehil Sood 19UEC036

Course Coordinator
Dr. Kusum Lata
ECE Wednesday batch

Department of Electronics and Communication Engineering
The LNM Institute of Information Technology, Jaipur

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Chapter *1*

Experiment - 5

1.1 Aim

Implement 1 to 2, 2 to 4 and 3 to 8 line decoder using dataflow, behavioral and mixed modeling in VHDL. Implement Booleans functions using decoders.

1.2 Theory

The Binary Decoder is a combinational logic circuit constructed from individual logic gates and is the exact opposite to that of an Encoder. A decoder is a circuit that transforms a set of digital input signals into an equivalent decimal code at its output.
Binary Decoders is digital logic device that has inputs of 2-bit, 3-bit or 4-bit codes depending upon the number of data input lines, so a decoder that has a set of two or more bits will be defined as having an n-bit code, and therefore it will be possible to represent 2n possible values.
Thus, a decoder generally decodes a binary value into a non-binary one by setting exactly one of its n outputs to logic 1. Gray code, also known as reflected binary code (RBC), is a binary numeral system where two successive values differ in only one bit (binary digit).
Gray Code is a non-weighted code which belongs to a class of codes called minimum change codes. In this codes while traversing from one step to another step, only one bit in the code group changes. In case of Gray Code two adjacent code numbers differs from each other by only one bit.
This code is not applicable in any types of arithmetical operations but it has some applications in analog to digital converters and in some input/output devices.

1.3 Coding Techniques used

This experiment uses data flow and structural methods of Coding Techniques.
Using the behavioral technique, a 2 to 4 line decoder is designed with the help of nested if and elsif statements.
Data Flow: Describes how the data flows from the inputs to the output most often using NOT, AND and

OR operations.

Structural Modeling: COMPONENT and PORT MAP statements are used to implement structural modeling. Structural modeling is used to implement hierarchical design concept. That is the entities are already declared and then they can be used to implement a higher level entity.

1.4 Simulation and Results

1.4.1 2 to 4 decoder using behavioural modelling

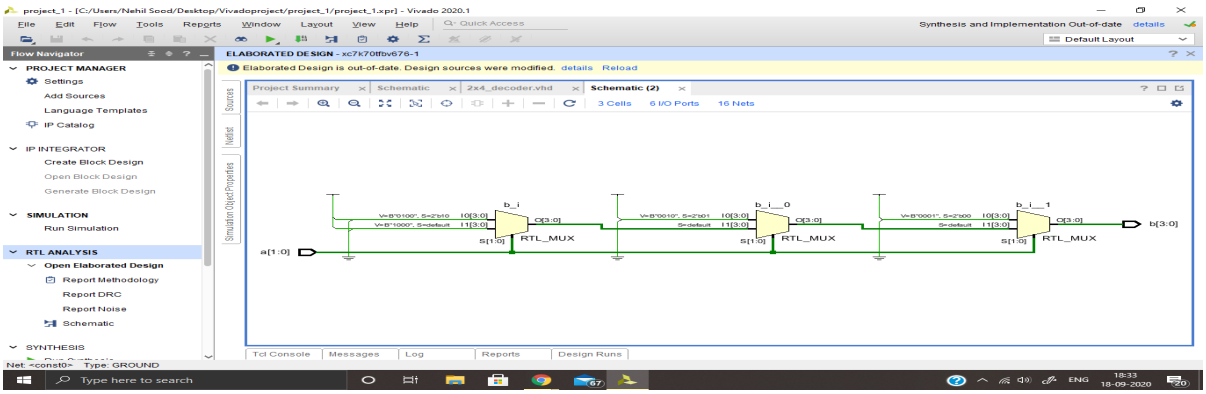

Figure 1.1 Schematic

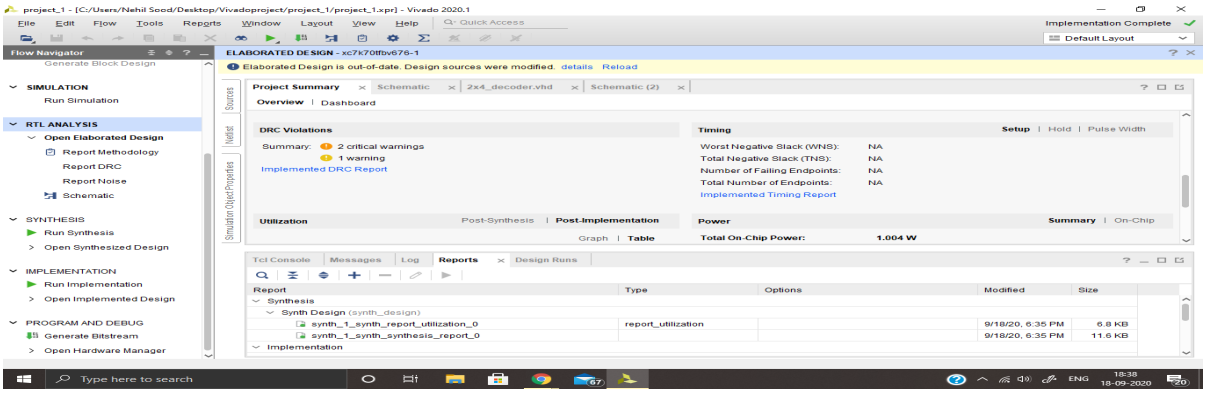

Figure 1.2 Project Summary

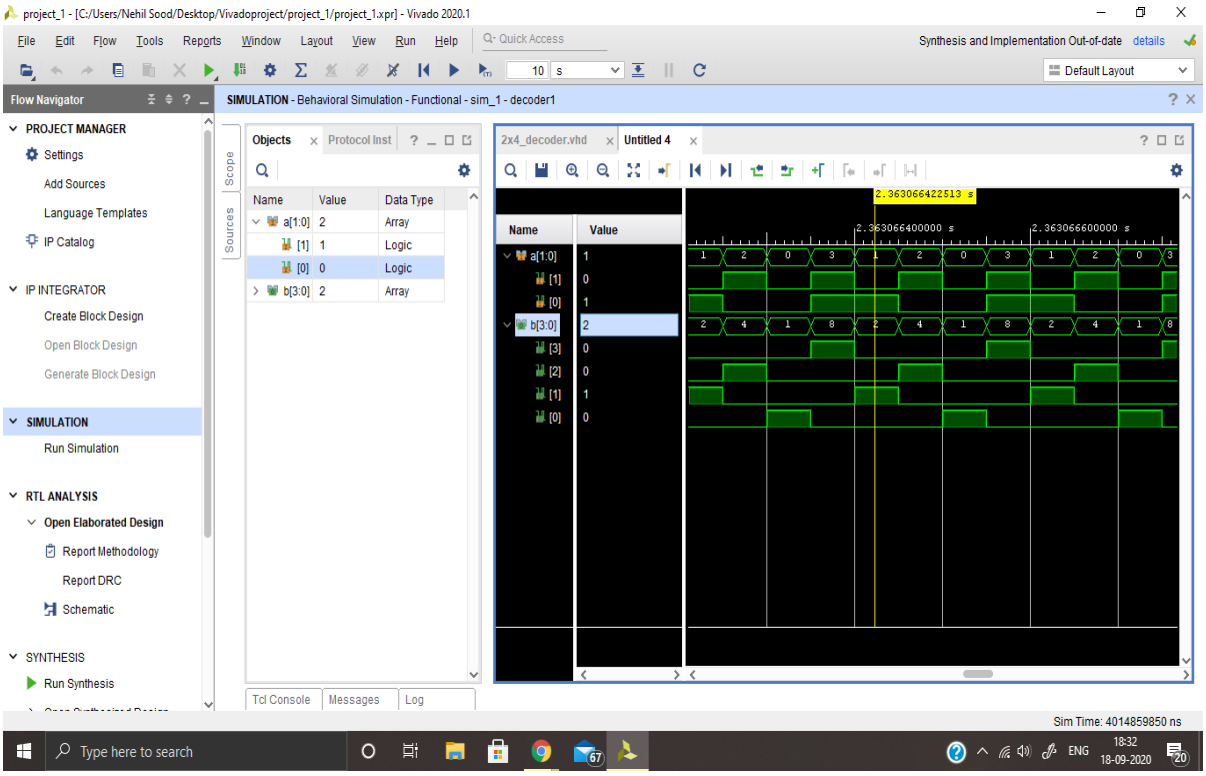

Figure 1.3 Simulation

1.4.2 3 to 8 line decoder Using dataflow

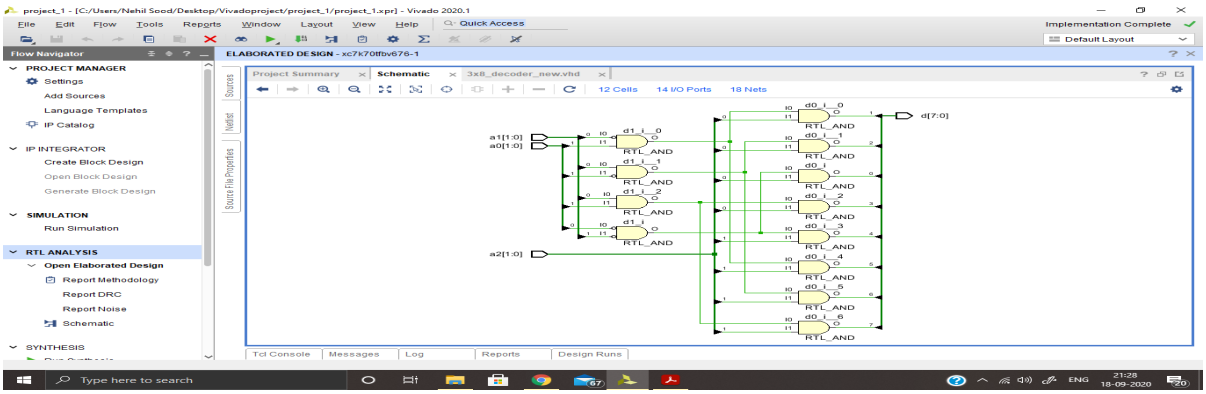

Figure 1.4 Schematic

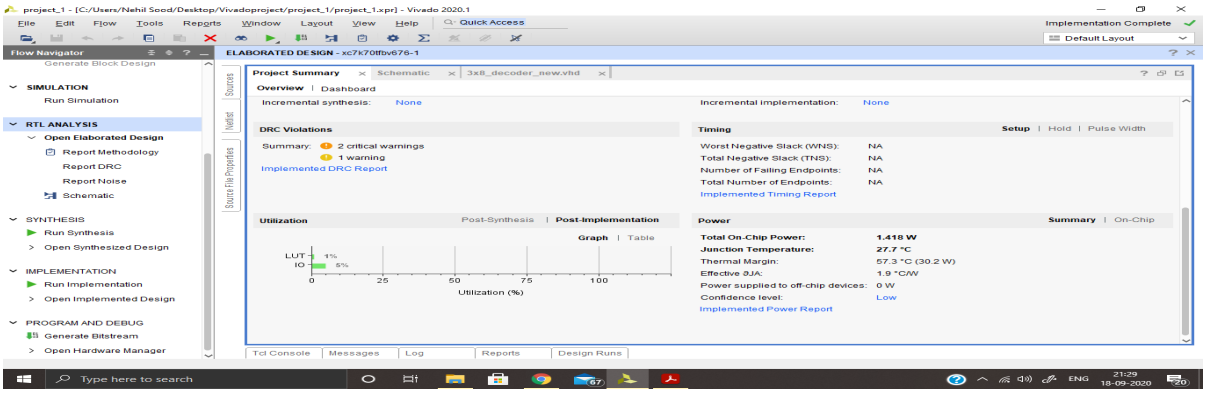

Figure 1.5 Project Summary

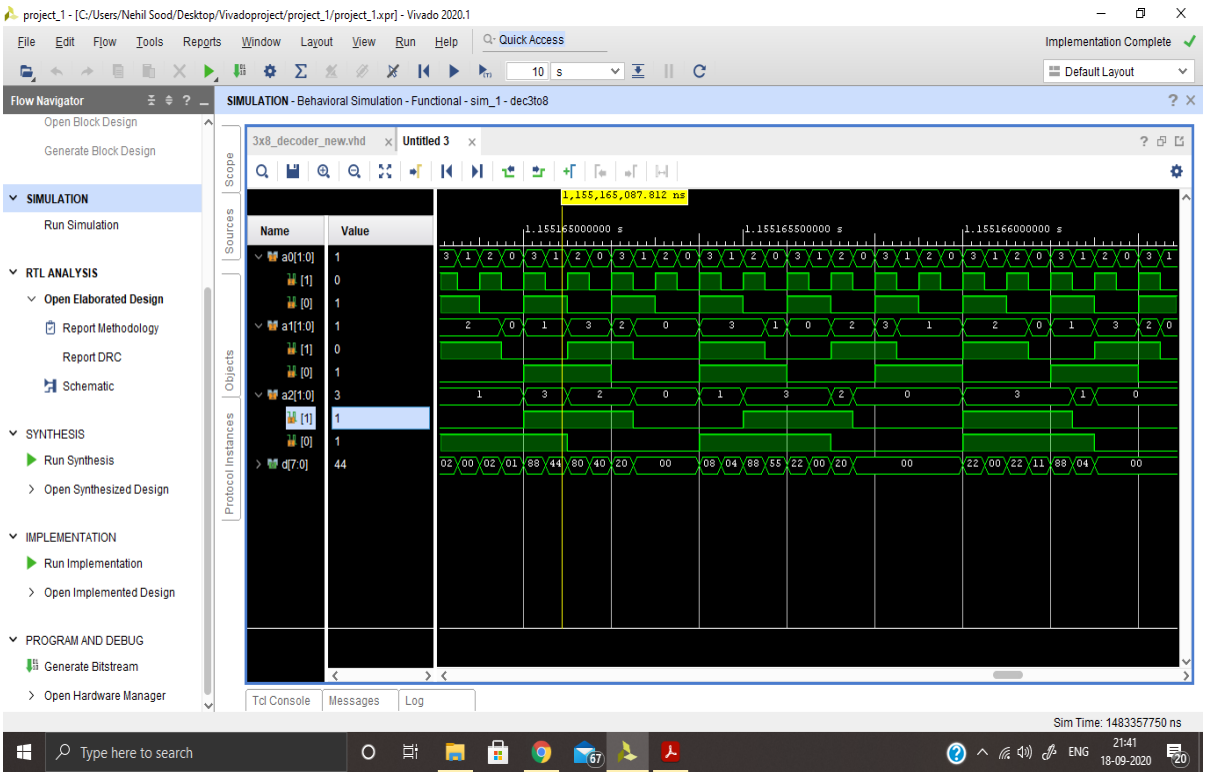

Figure 1.6 Simulation

1.4.3 3 to 8 line decoder by using structural architecture

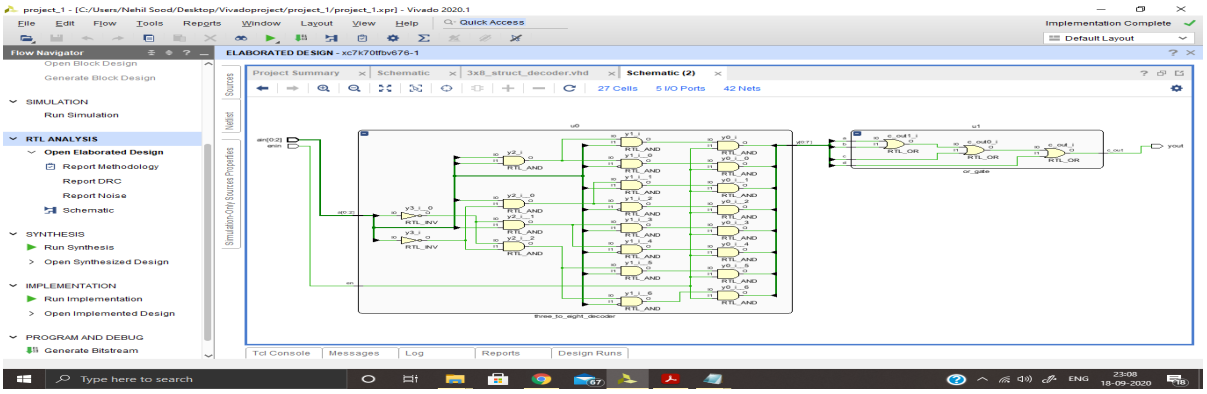

Figure 1.7 Schematic

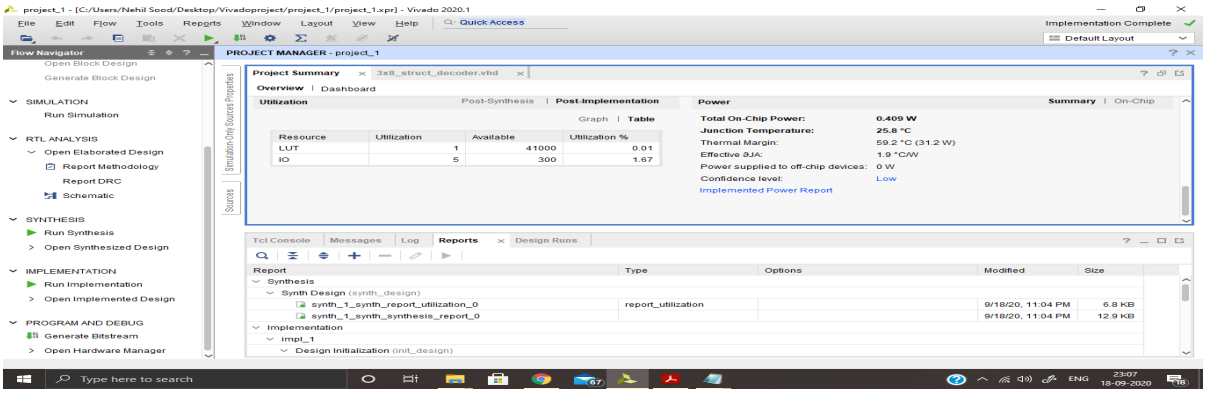

Figure 1.8 Project Summary

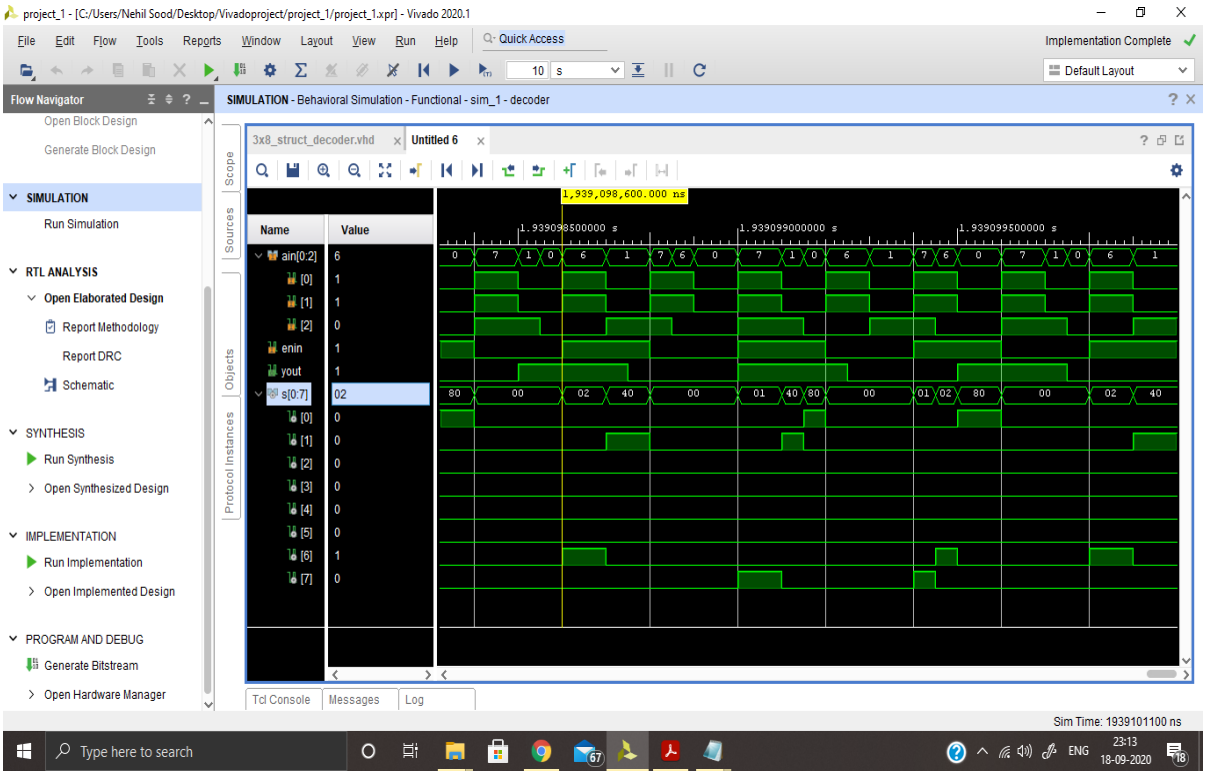

Figure 1.9 Simulation

1.4.4 4 bit array of binary number system to the corresponding 4 bit array of gray code.

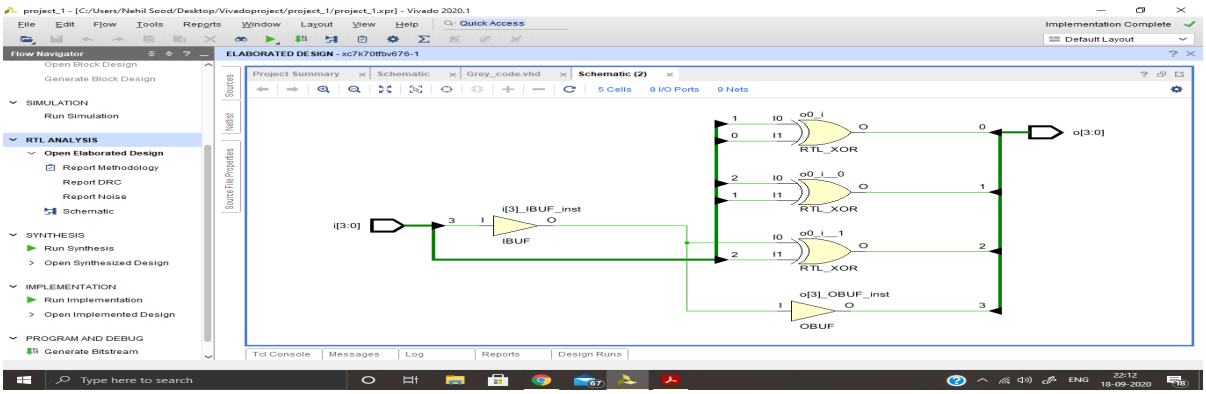

Figure 1.10 Schematic

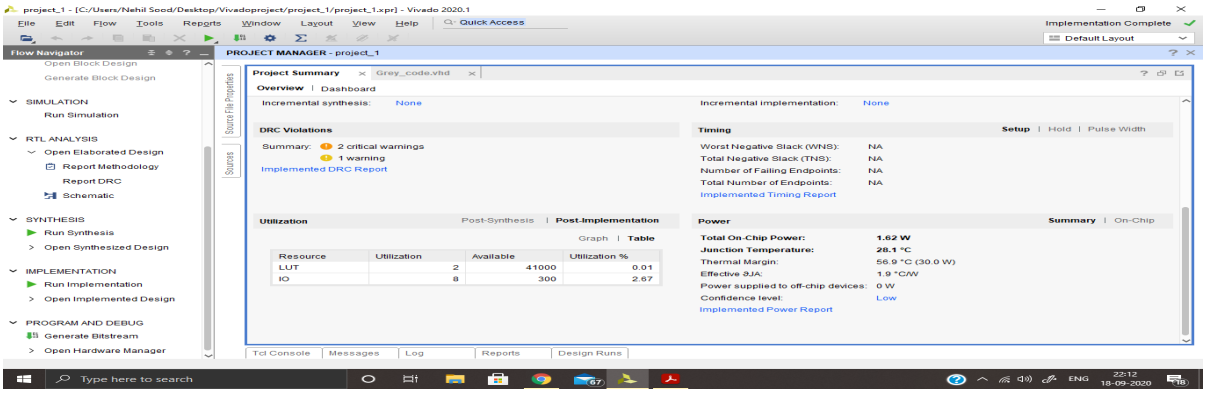

Figure 1.11 Project Summary

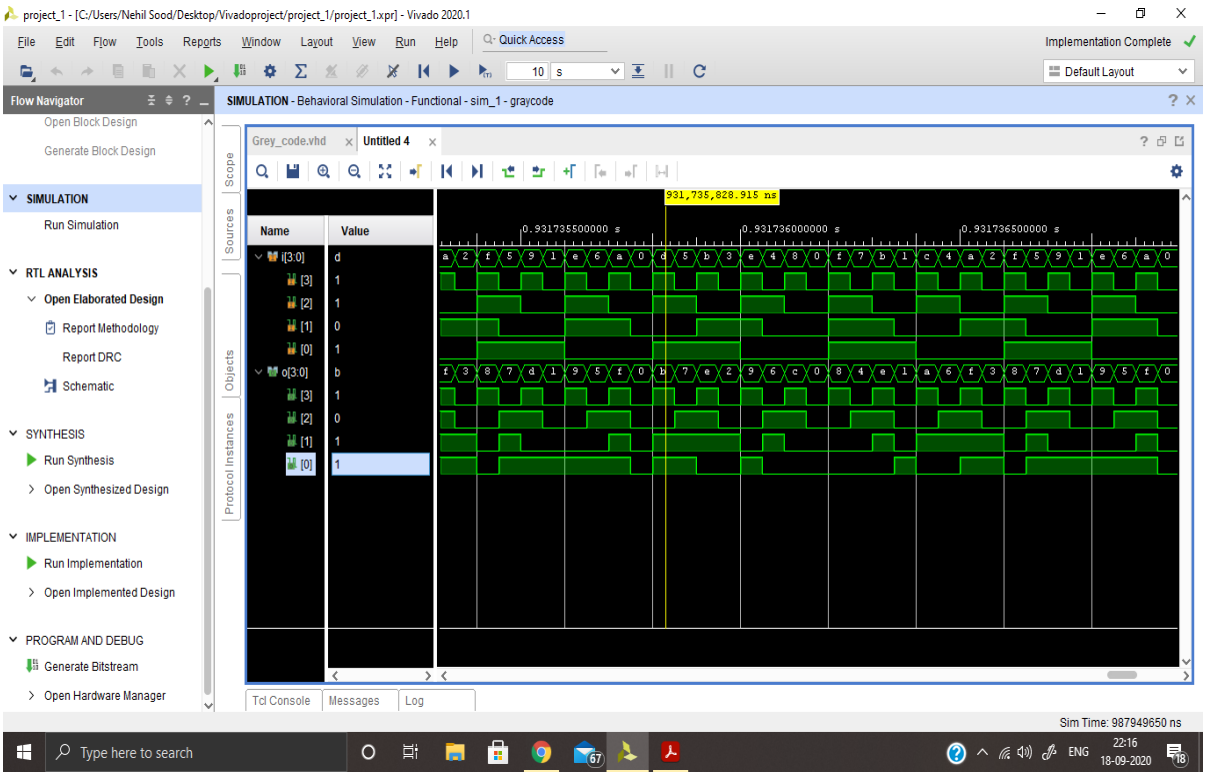

Figure 1.12 Simulation

1.4.5 4 to 16 line decoder using only 2 to 4 line decoders, using structural modeling

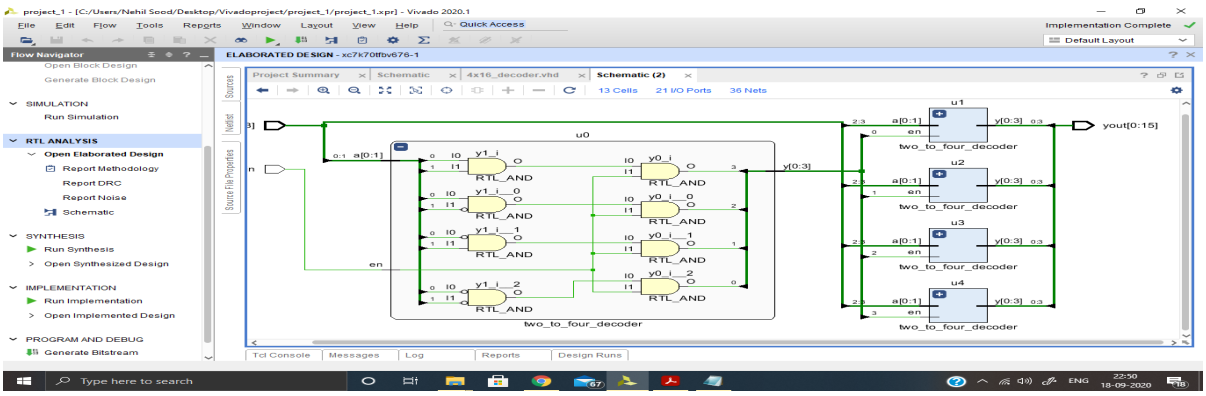

Figure 1.13 Schematic

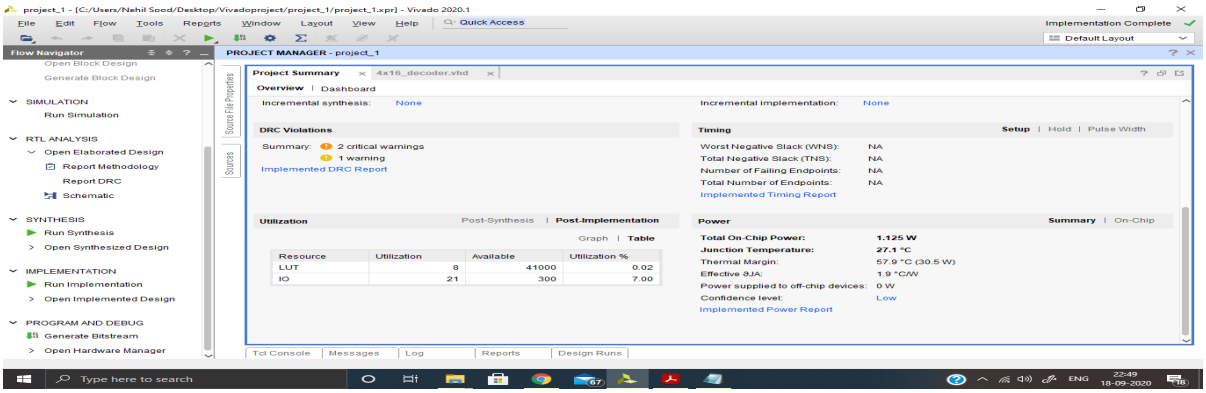

Figure 1.14 Project Summary

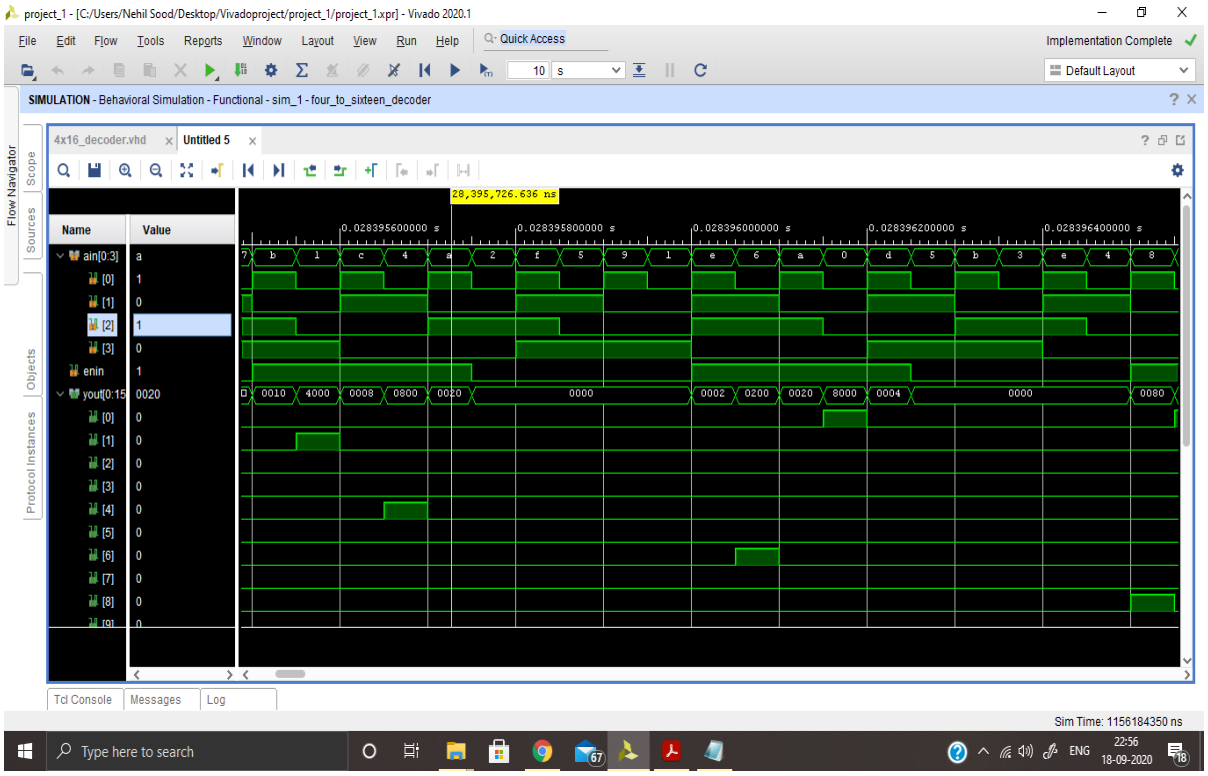

Figure 1.15 Simulation

1.5 Summary

Name of the Entity	No. of LUT used	Total On chip Power
2 to 4 decoder using behavioural modelling	1	1.004W
3 to 8 line decoder Using dataflow	2	1.418W
3 to 8 line decoder by using structural architecture	1	0.409W
4 bit array of binary number system 4 bit array of gray code	2	1.620W
4 to 16 line using only 2 to 4 line, using structural modeling	8	1.125W

Table 1.1 Comparison of Area and Power requirements for different kinds of adders.