Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor of Technology
in
Computer and Communication Engineering

by

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Contents

Chapter *1*

Experiment - 3

1.1 Aim

Implementation of 2x1, 4x1 and 8x1 multiplexers using Dataflow, Behavioral and Structural modeling in VHDL.

1.2 Description

A. The multiplexer, shortened to MUX, is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal. Multiplexers operate like very fast acting multiple position rotary switches connecting or controlling multiple input lines called channels one at a time to the output.

B. Multiplexers, or MUXs, can be either digital circuits made from high speed logic gates used to switch digital or binary data or they can be analogue types using transistors, MOSFETs or relays to switch one of the voltage or current inputs through to a single output.

C. So the three basic and bare minimum terms on any Multiplexer will be Input Pins, Output Pin and Control Signal:
i) Input Pins: These are the available signal pins from which one has to be selected. These signals can either be a digital signal or analog signal.
ii) Output Pin: A multiplexer will always have only one output pin.The selected input pin signal will be provided by the output pin.
iii) Control/Selection Pin: The Control Pins are used to select the input pin signal. The number of control pins on a Multiplexer depends on the number of input pins.

1.3 Simulation and Results

1.3.1 2x1 mux using Dataflow

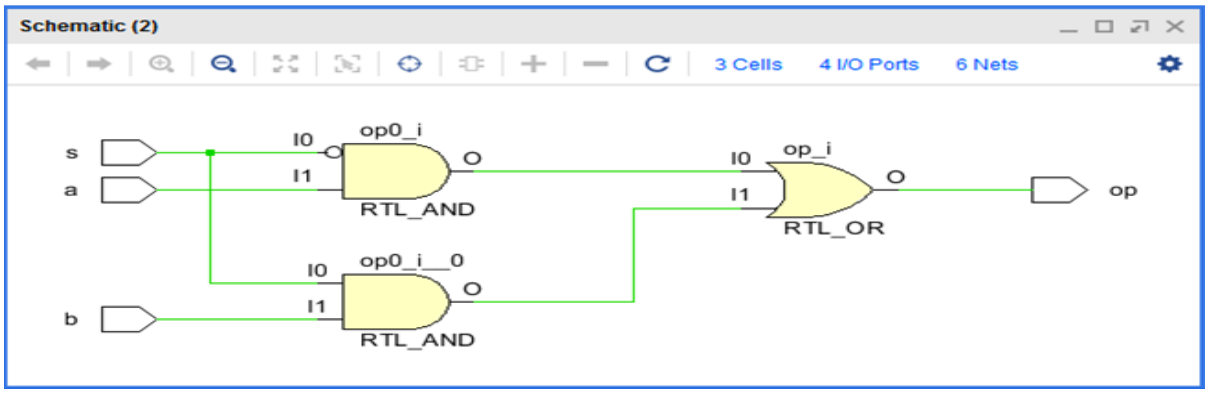

Figure 1.1: Schematic for problem (i)

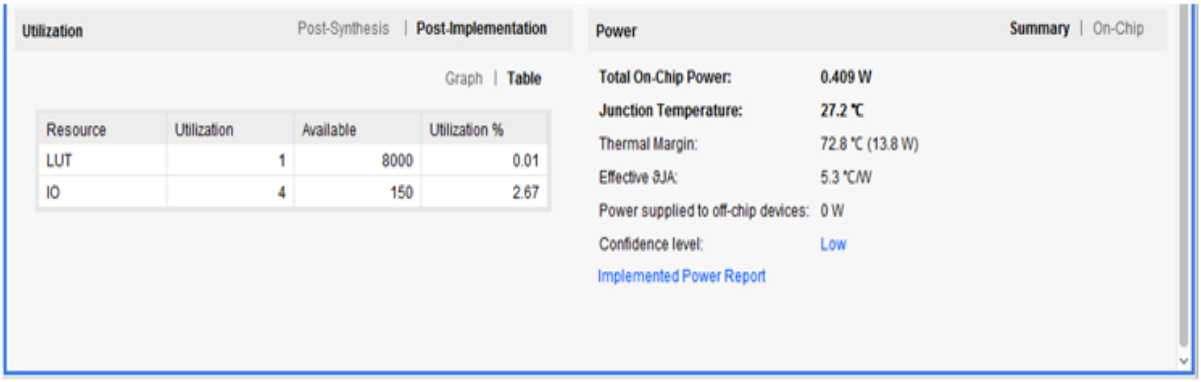

Figure 1.2: Project Summary for problem (i)

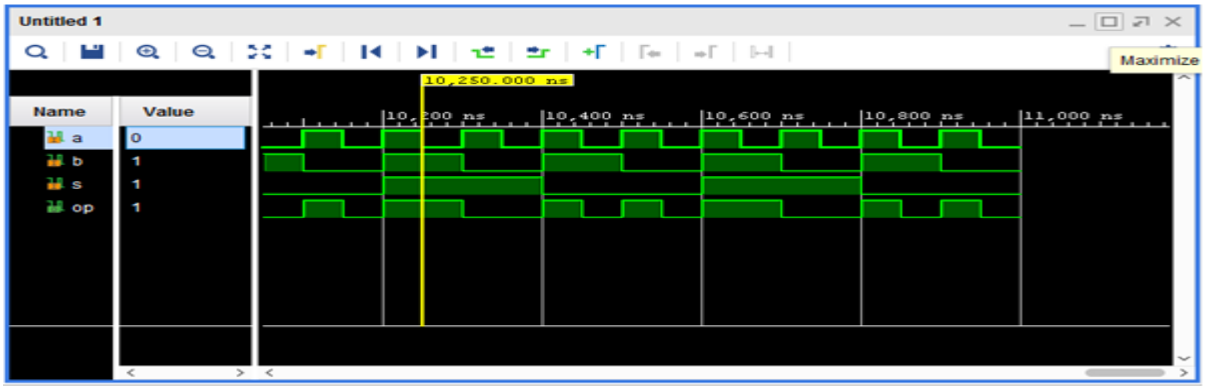

Figure 1.3: Simulation for problem (i)

1.3.2 2x1 mux using Behavioral

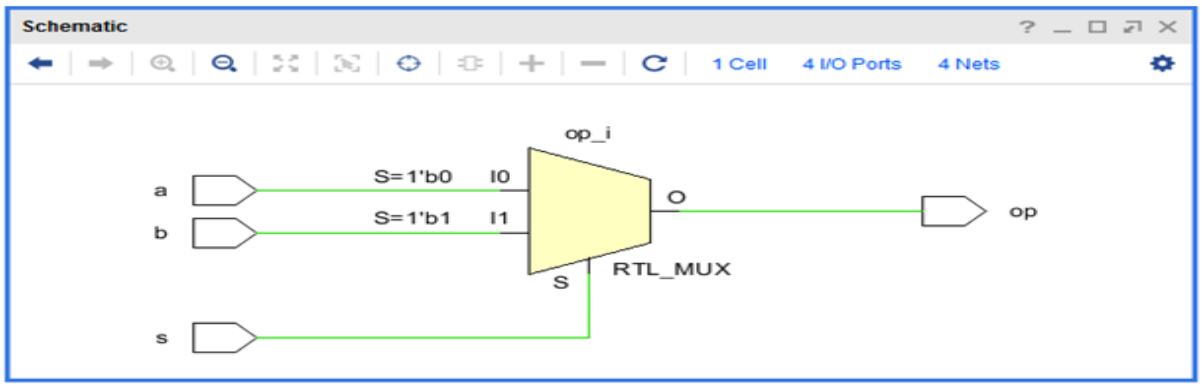

Figure 1.4: Schematic for problem (ii)

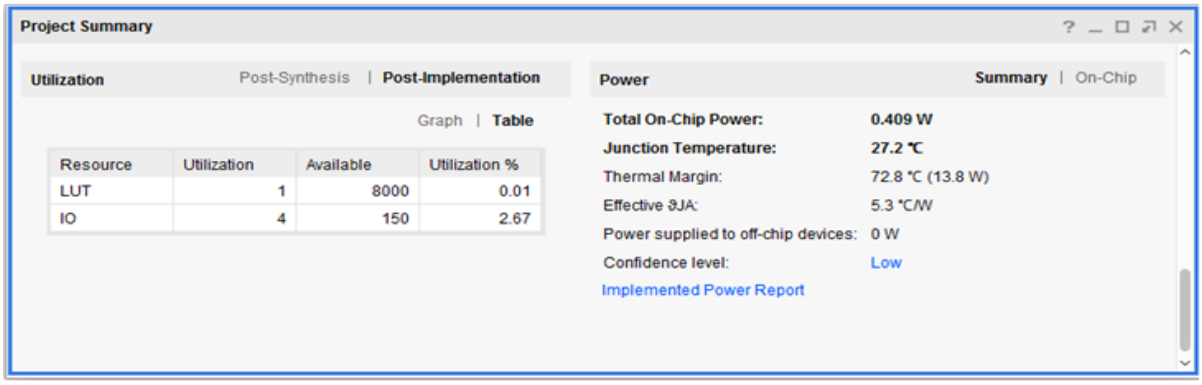

Figure 1.5: Project Summary for problem (ii)

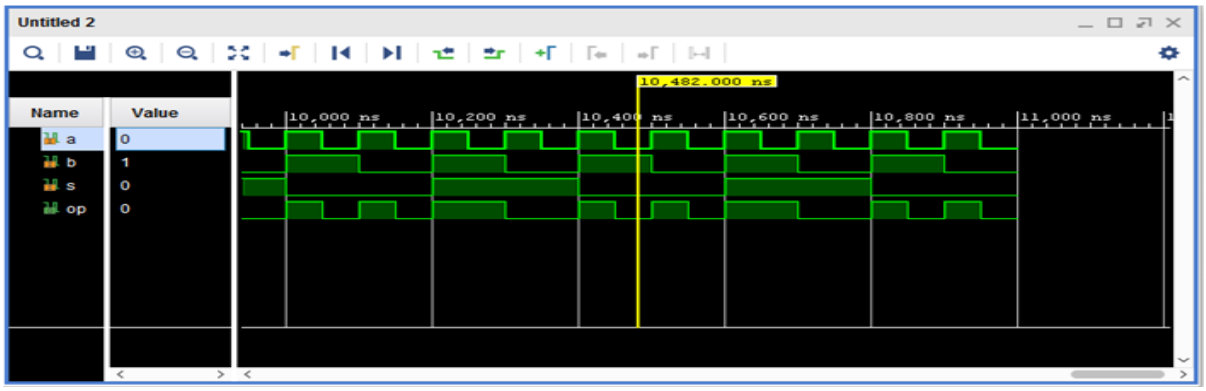

Figure 1.6: Simulation for problem (ii)

1.3.3 4x1 mux using dataflow

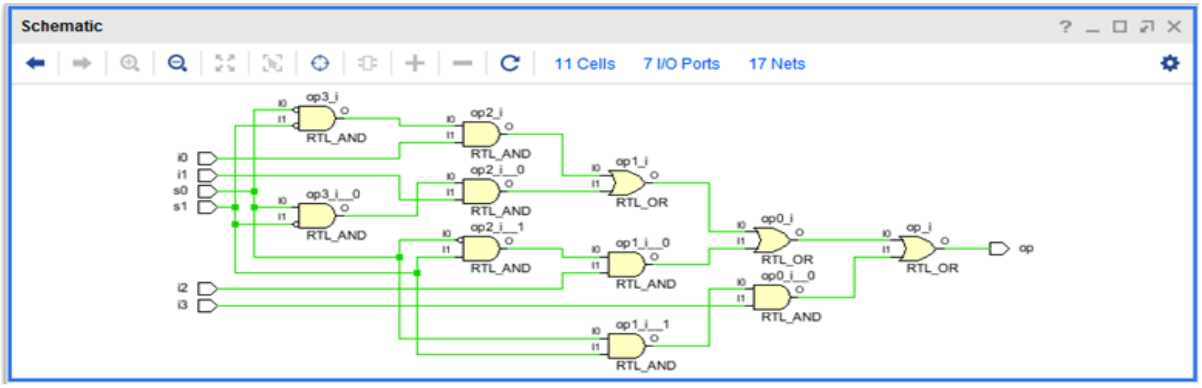

Figure 1.7: Schematic for problem (iii)

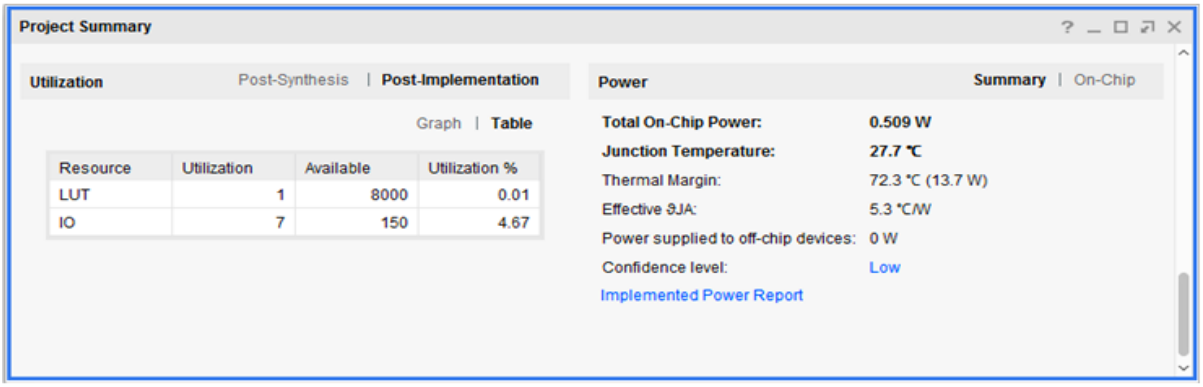

Figure 1.8: Project Summary for problem (iii)

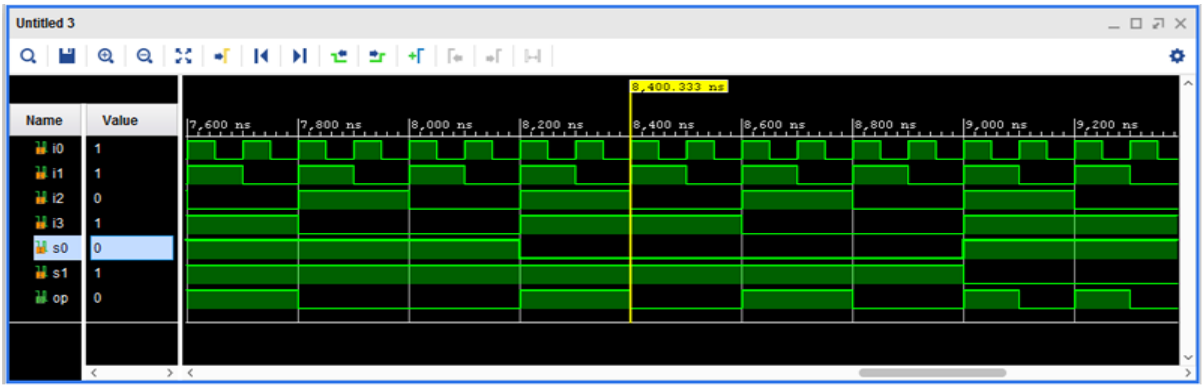

Figure 1.9: Simulation for problem (iii)

1.3.4 4x1 mux using structural

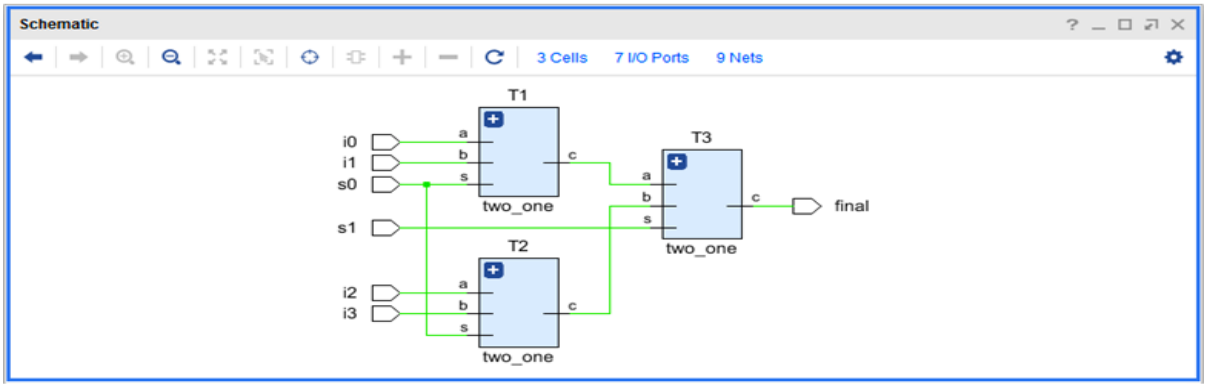

Figure 1.10: Schematic for problem (iv)

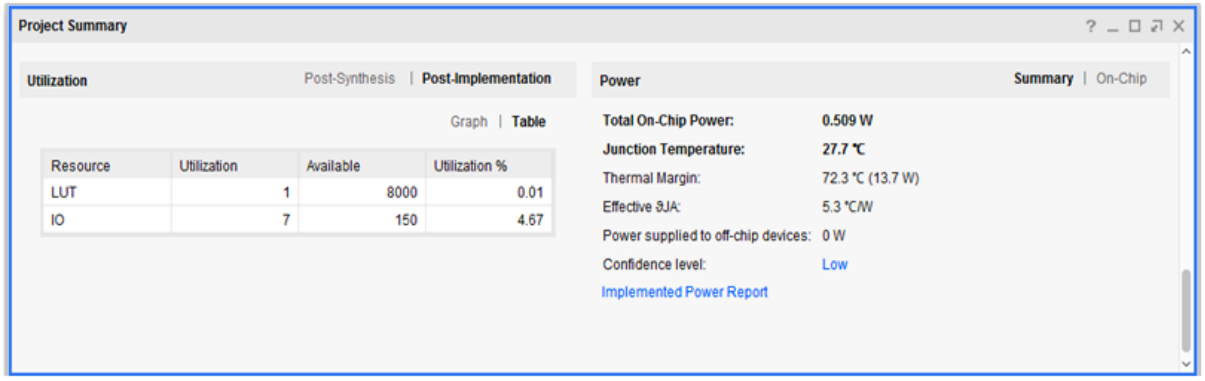

Figure 1.11: Project Summary for problem (iv)

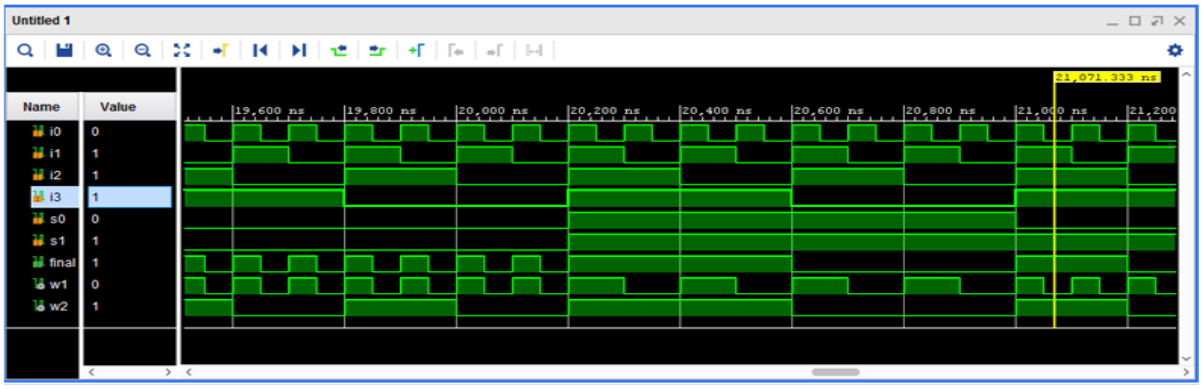

Figure 1.12: Simulation for problem (iv)

1.3.5 8x1 mux using structural

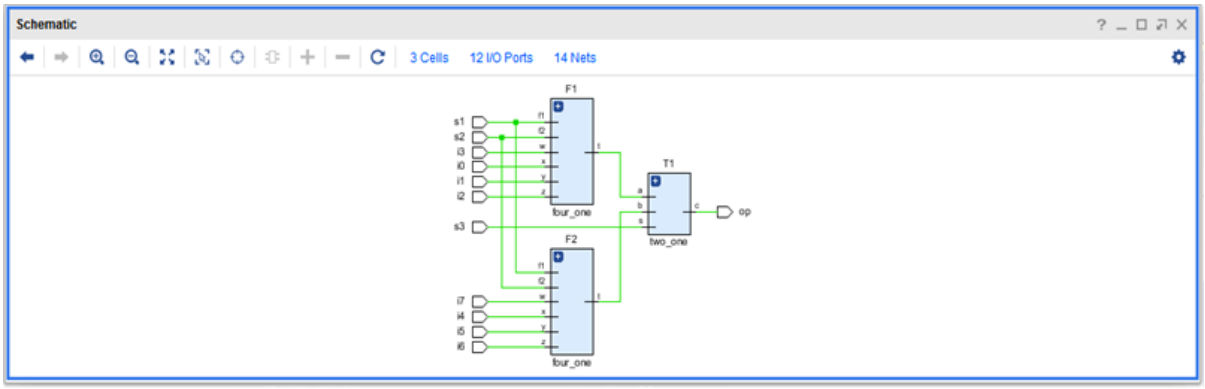

Figure 1.13: Schematic for problem (iv)

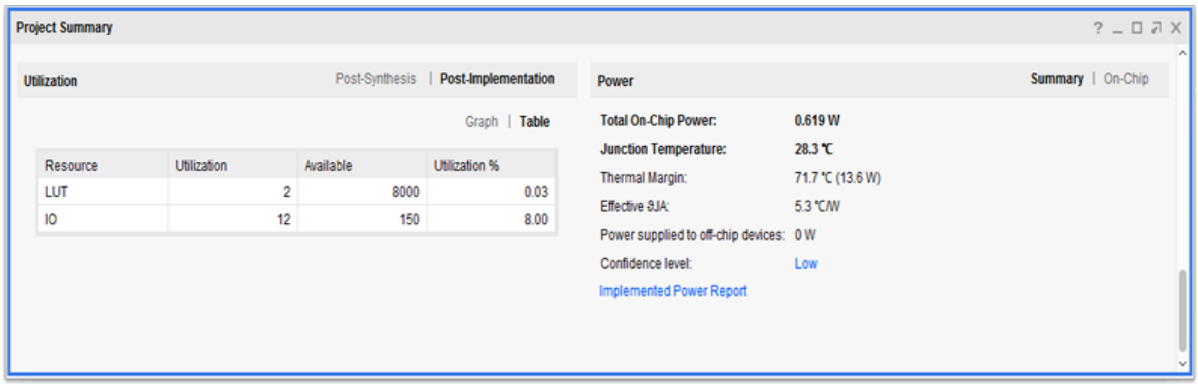

Figure 1.14: Project Summary for problem (iv)

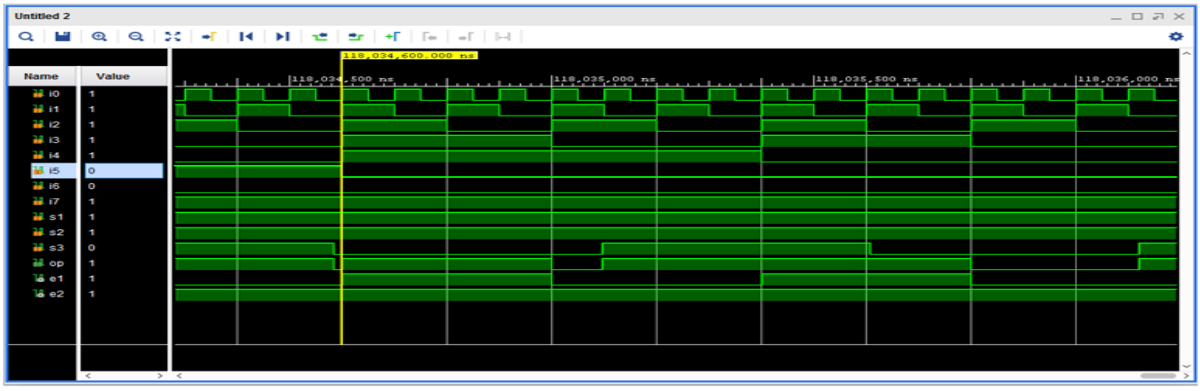

Figure 1.15: Simulation for problem (iv)

1.4 Summary

Name of the Entity	No. of LUT used	Total On chip Power
2x1 MUX using dataflow	1	0.409
2x1 MUX using behavioral	1	0.409
4x1 MUX using dataflow	1	0.509
4x1 MUX using structural	1	0.509
8x1 MUX using structural	2	0.619

Table 1.1: Comparison of the power and cell usage in all 4 different implementation.