Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor of Technology
in
Electronics And Communication Engineering

by

Nehil Sood – 19uec036

Course Coordinator
Dr. Kusum Lata

Department of Electronics and Communication Engineering
The LNM Institute of Information Technology, Jaipur

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Contents

Chapter *1*

Experiment - 9

1.1 Name of the Experiment

To study mod - 16 counter and 2 to 12 counter.

1.2 Theory

The counter have 4 bit parallel input I, control signals clock, clear, count enable and load. It has 4 bit output S and one bit output Terminal count.it have a relation between input and load.

Counter is a digital sequential circuit which is used for a counting pulses. Counter is the widest application of ip-ops. It is a group of ip-ops with a clock signal applied. Counters are of two types.

1. Asynchronous or ripple counters.
2. Synchronous counters.

Counters which advance their sequence of numbers or states when activated by a clock input are said to operate in a count-up mode. Likewise, counters which decrease their sequence of numbers or states when activated by a clock input are said to operate in a count-down mode. Counters that operate in both the UP and DOWN modes, are called bidirectional counters. The modulus (or just modulo) is the number of states the counter counts and is the dividing number of the counter. Modulus counters, or simply MOD counters, are dened base on the number of states that thecou nter will sequence through before returning back to its original value.

1.3 Coding Techniques used

mod- 16 counter behavioral coding has been used. mod 2 to 12 counter we have used structural coding.

1. The modulo 16 counter was implemented with 4 bit parallel input I, control signals clock, clear, count enable and load. It has 4 bit output S and one bit output Terminal count. Using Behavioral model for the vhdl code, we dene two separate processes, one for the output S and the other for Terminal Count.

2. The modulo 16 counter was used as a component to design a 2 to 12 counter using Structural model. The S(3) and S(2) bit of the 4 bit output vector are fed into the Load input via an AND gate. Whenever the counter gets an output of 12 (ie. 1100 in binary) the Load input gets an input 1. we specify that when Load input is 1, input wil be 2 (ie. 0010 in binary). Hence it will count from 2 to 12.

1.4 Simulation and Results

1.4.1 Mod 16 counter

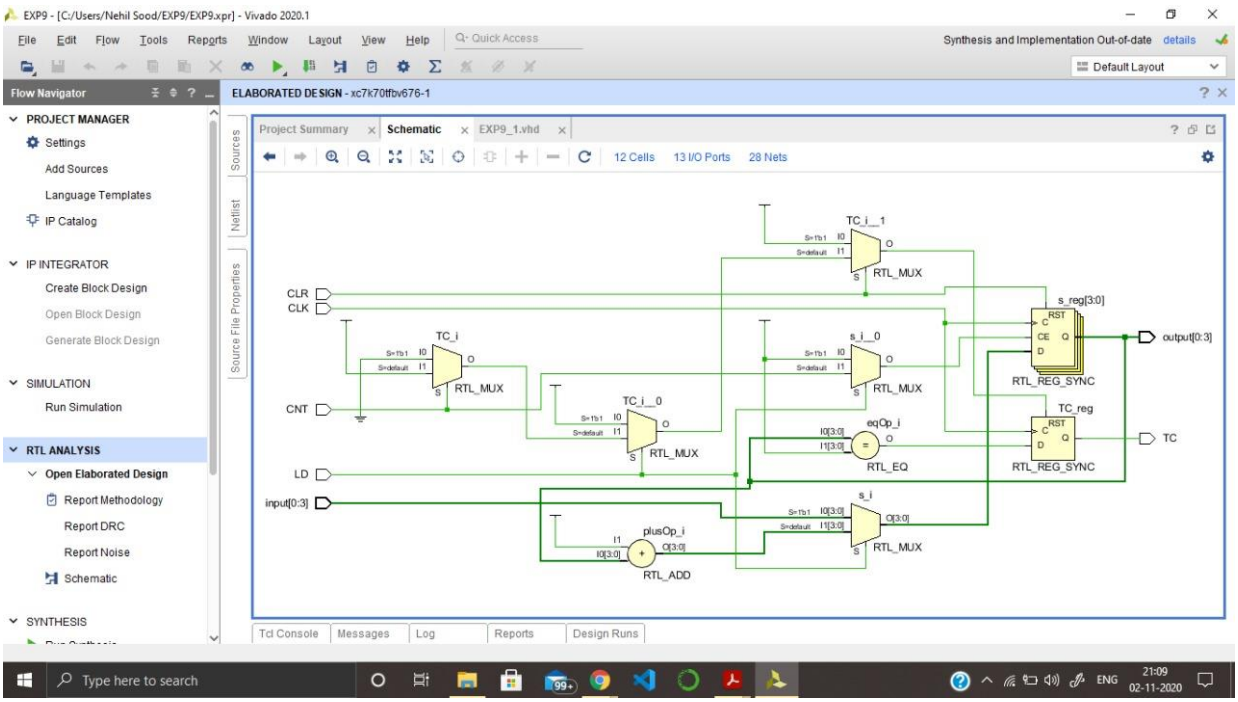

Figure 1.1 Schematic of the mod 16 counter

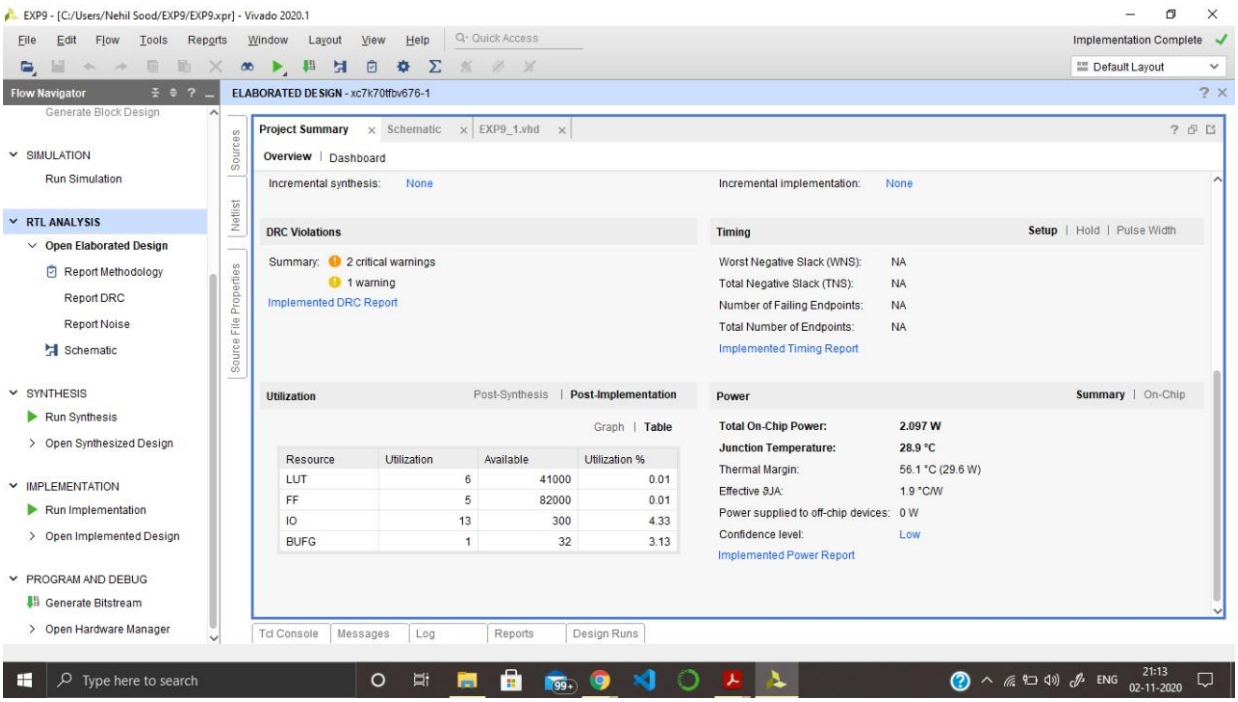

Figure 1.2 Project Summary of the mod 16 counter

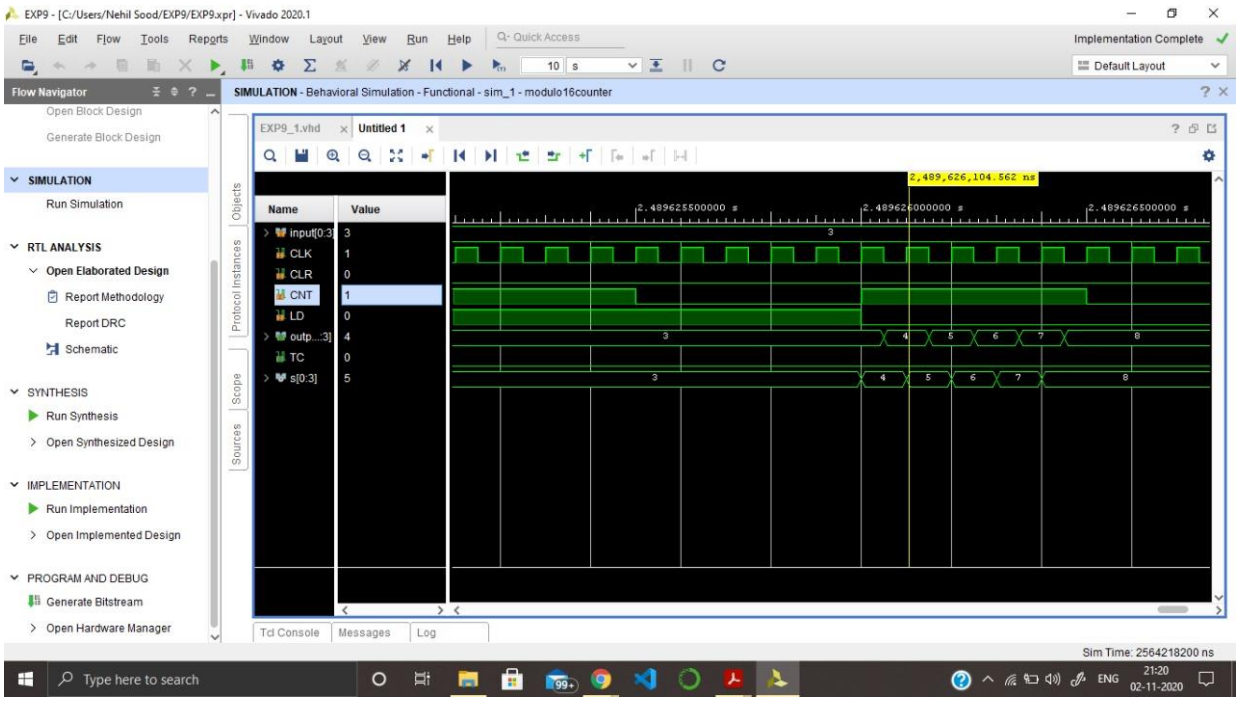

Figure 1.3 Simulation of the mod 16 counter

1.4.2 Mod 2 to 12 counter

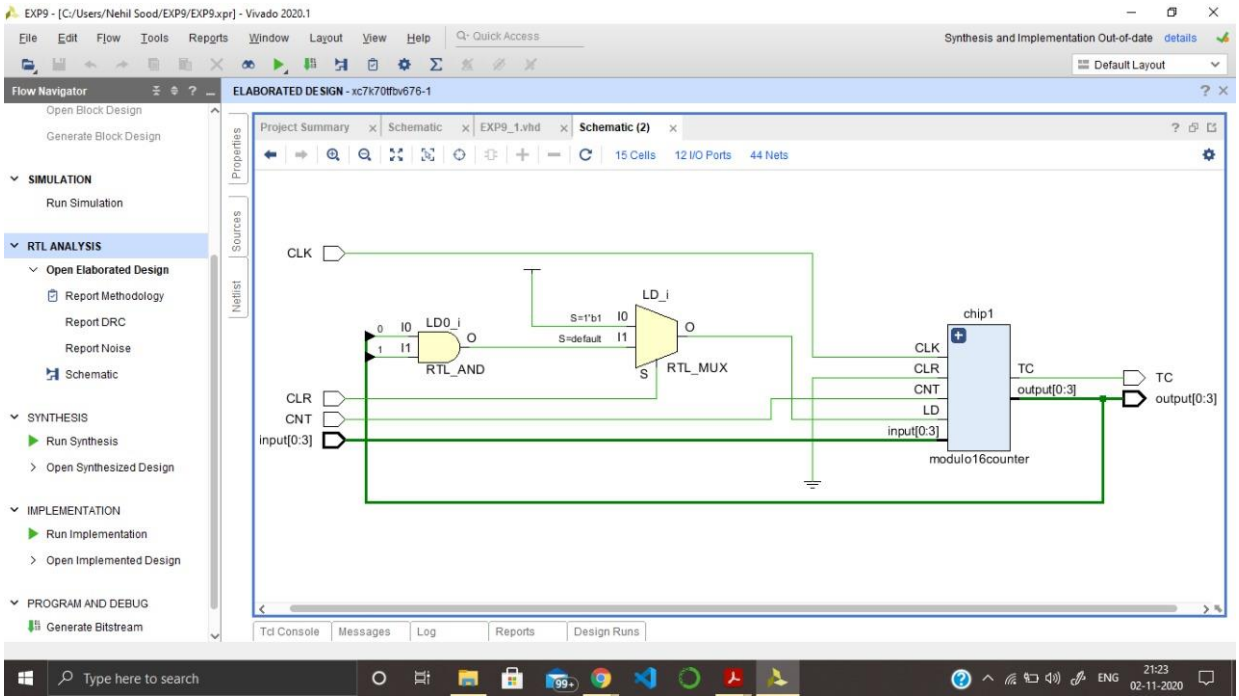

Figure 1.4 Schematic of the mod 2 to 12 counter

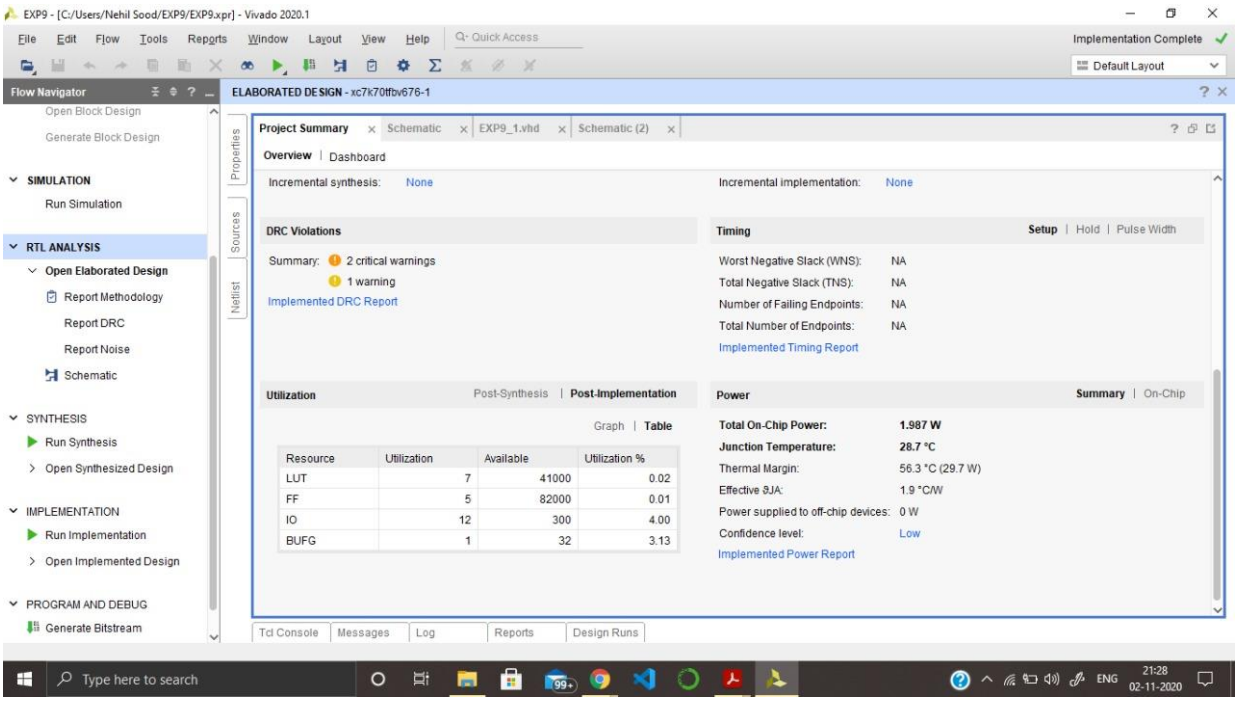

Figure 1.5 Project Summary of the mod 2 to 12 counte

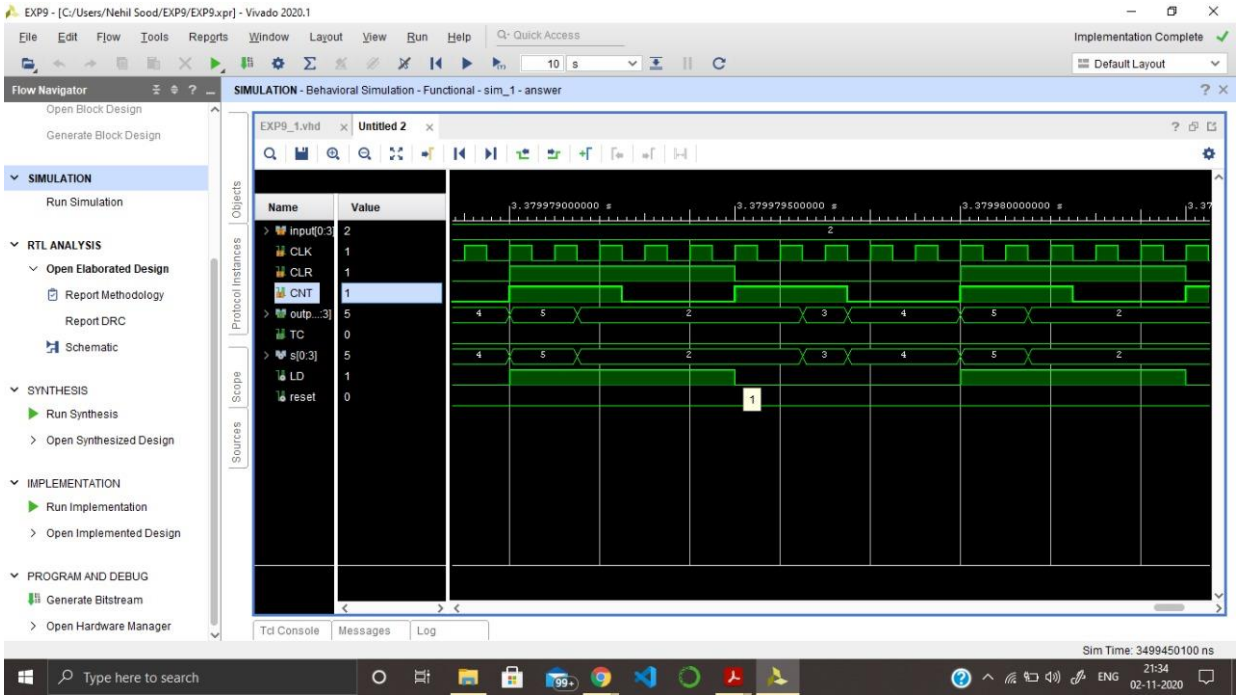

Figure 1.6 Simulation of the mod 2 to 12 counter

1.5 Summary

Name of the Entity	No. of LUT used	Total On chip Power
Mod 16 counter	8	2.032 W
Mod 2 to 12 counter	9	2.326 W

Table 1.1 comparison of Area and power requirements