Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor of Technology
in
Computer and Communication Engineering

by

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Contents

Chapter *1*

Experiment - 2

1.1 Aim

Realize the function,mentioned below in at least four different physical ways:
$F(x) = x0 + x1 + x2 + x3 + x4 + x5 + x6 + x7 + x8 + x9$

1.2 Description

A. Here we will give two inputs in the two input OR gate which results in the 1st stage of our network.Now its output and next input will be passed through another OR gate resulting in the second stage. Similarly, we can implement the function in eight stages.

B. In this implementation, we can give first four variable as inputs to the 1st 4-input OR gate and the other four variables to the 2nd 4-input OR gate. Now give the output of these both to another 4 input OR gate with rest of the inputs.

C. For implementing f(x) as a three stage network we can use series of three 4-input OR gate. In the first gate we will give four variables .Then its output to another 4 input OR gate with next 3 inputs and so on.

D. In this implementation also we can use our 4-input OR gate. we will use a series of four gates which will give us four stage network.

1.3 Coding Techniques used

First, we have to implement a 8 stages of 2 input or gates by creating a structural 2 input or gate.Second,we implement f(x) using 3 4-input or gates by creating a structural 4 input or gate.Third,we

implement f(x) using 3 stages by using structural 3 inputs and 2 inputs or gate.At last,we implement f(x) in four stages,done by 3 input or gates by creating structural 3 input or gate components.

1.4 Simulation and Results

1.4.1 8 Stages of 2 input-or gate

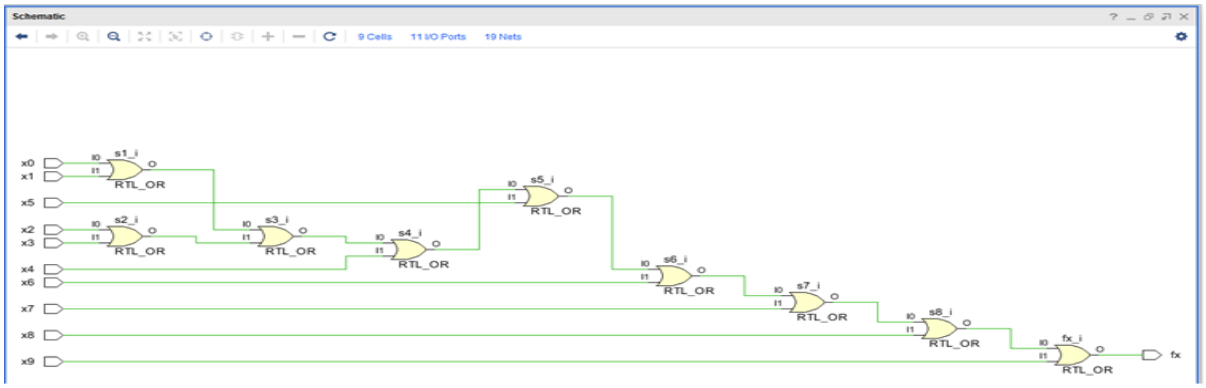

Figure 1.1: Schematic for problem (i)

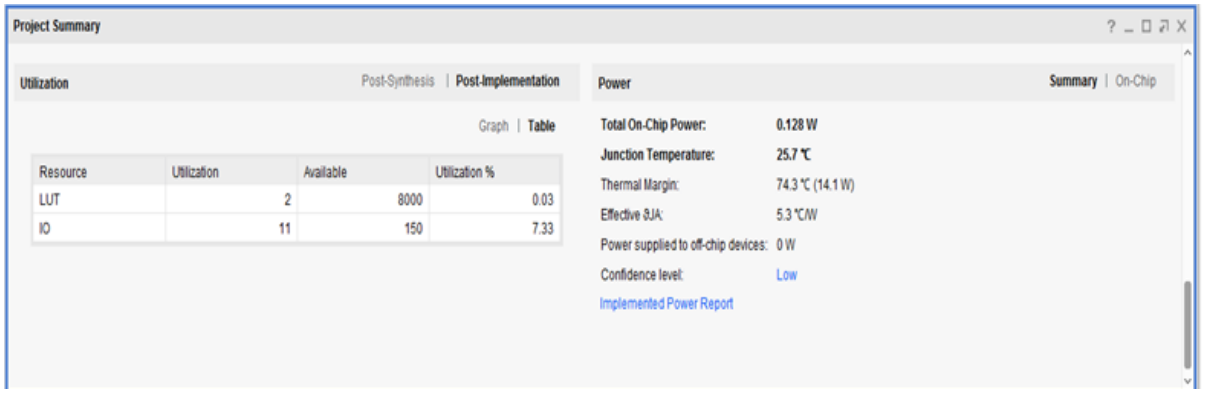

Figure 1.2: Project Summary for problem (i)

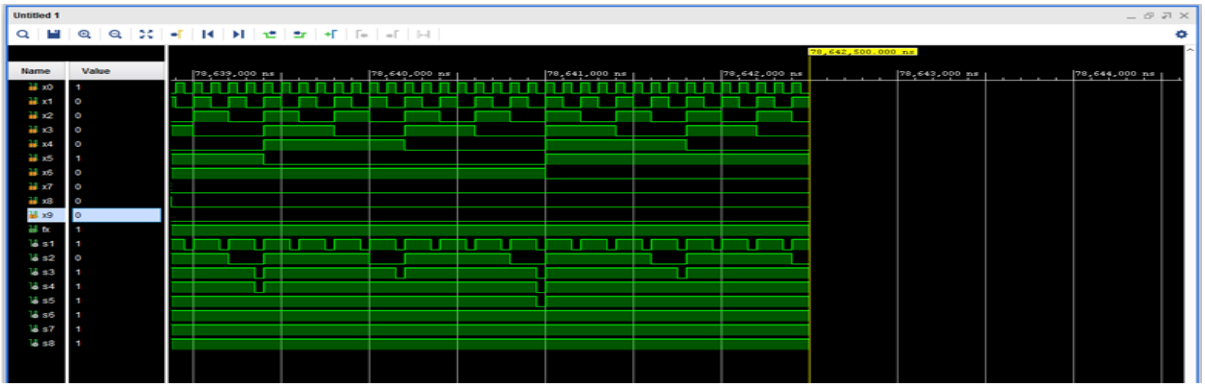

Figure 1.3: Simulation for problem (i)

1.4.2 3 or gates having 4 input

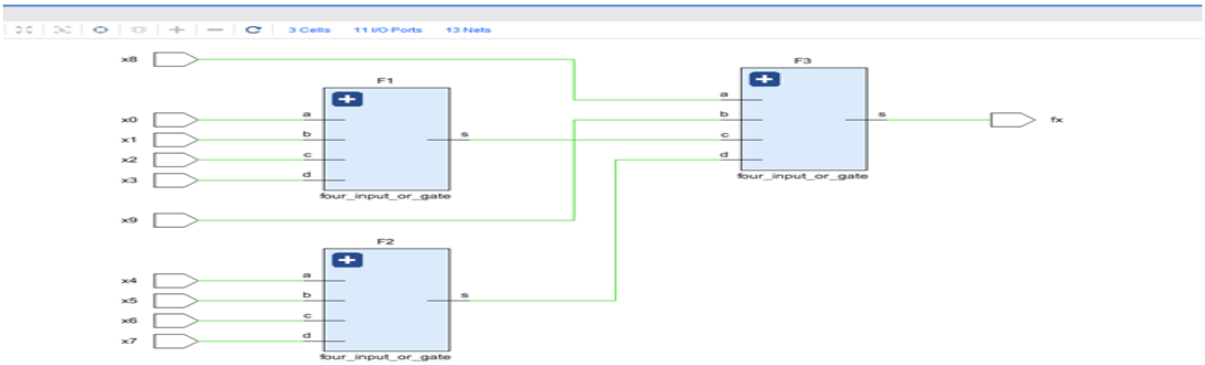

Figure 1.4: Schematic for problem (ii)

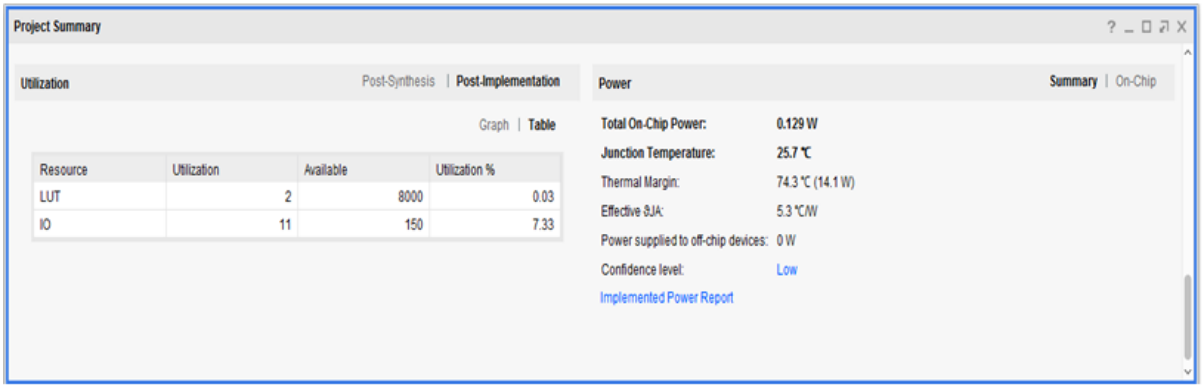

Figure 1.5: Project Summary for problem (ii)

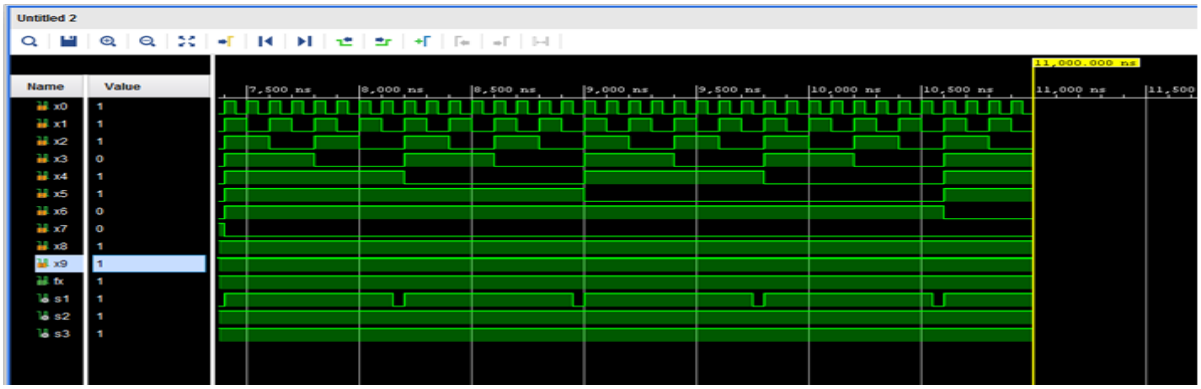

Figure 1.6: Simulation for problem (ii)

1.4.3 3-stage network

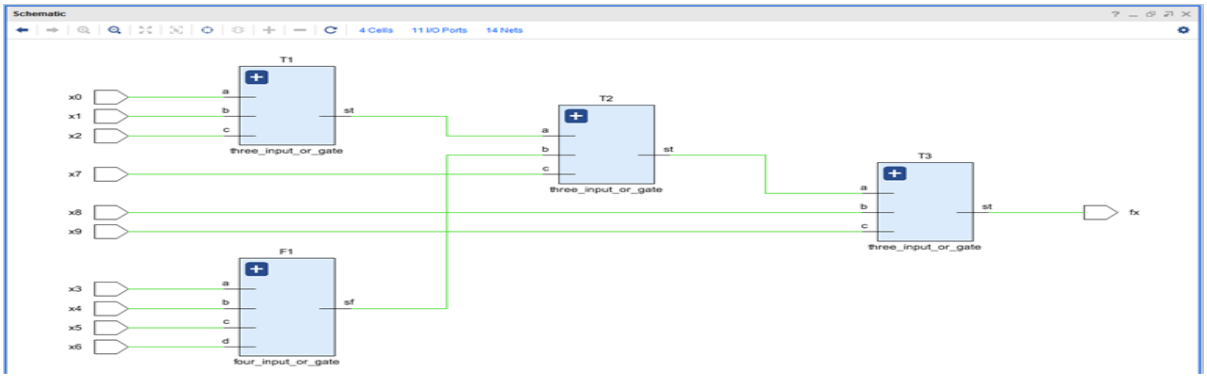

Figure 1.7: Schematic for problem (iii)

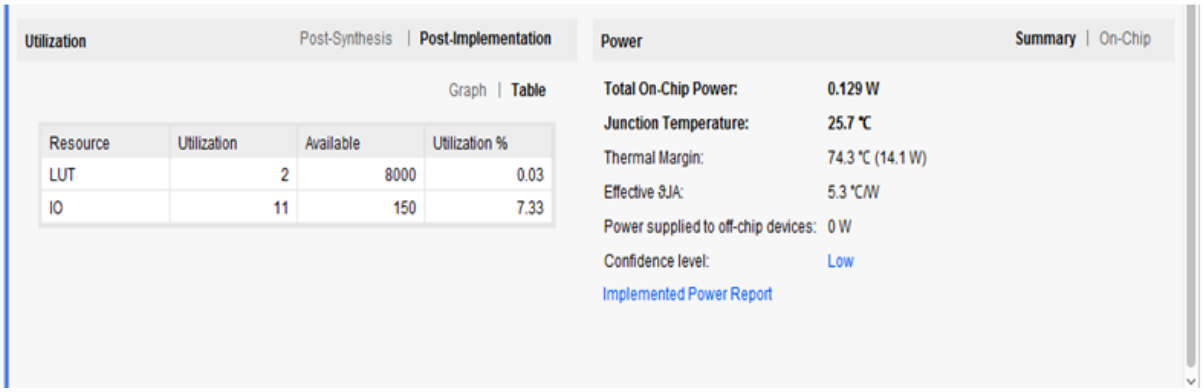

Figure 1.8: Project Summary for problem (iii)

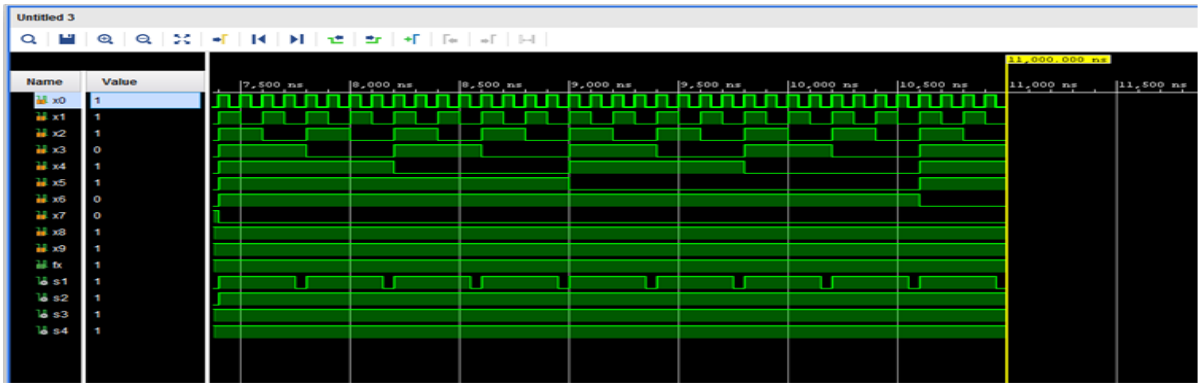

Figure 1.9: Simulation for problem (iii)

1.4.4 4-stage network

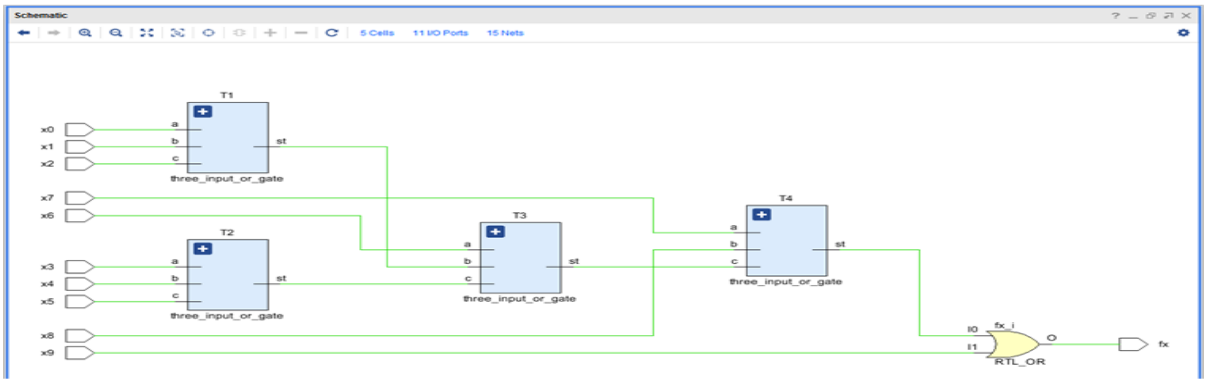

Figure 1.10: Schematic for problem (iv)

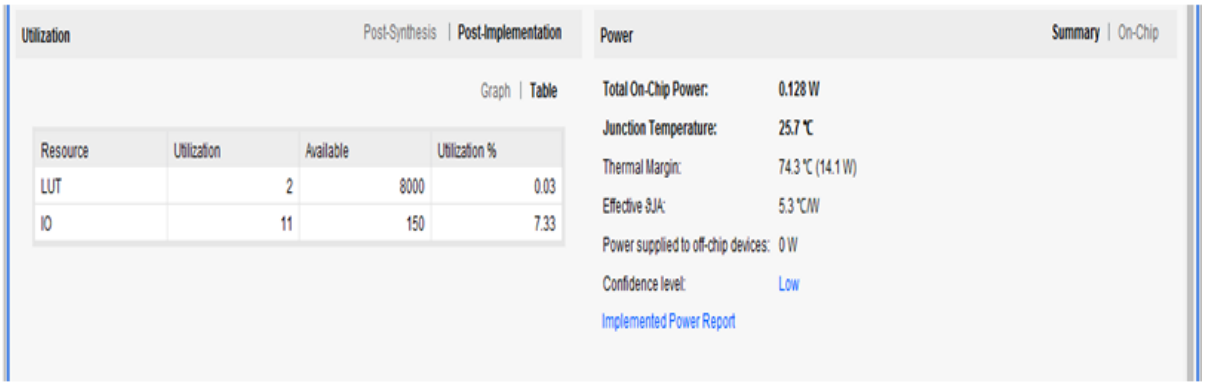

Figure 1.11: Project Summary for problem (iv)

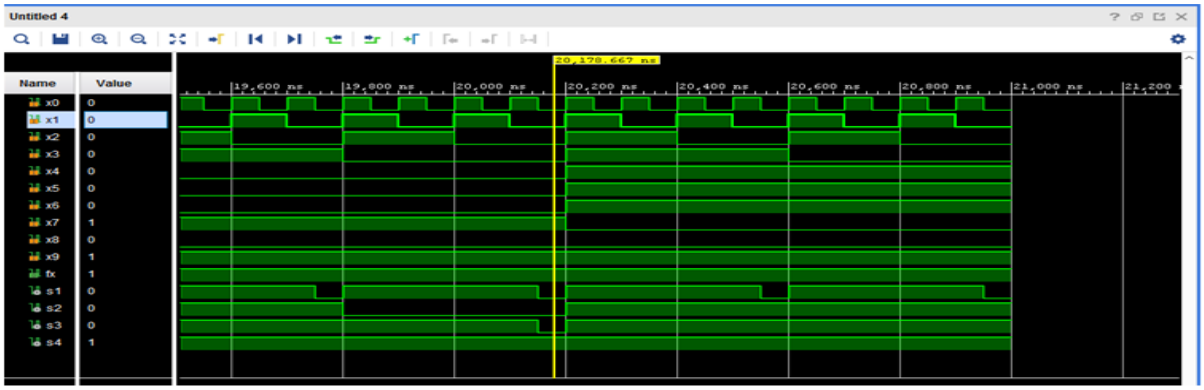

Figure 1.12: Simulation for problem (iv)

1.5 Summary

Name of the Entity	No. of LUT used	Total On chip Power
8-Stages of 2 input or-gate	2	0.128W
3 or gates having 4 input	2	0.129W
3-stage network	2	0.129W
4-stage network	2	0.128W

Table 1.1: Comparison of the power and cell usage in all 4 different implementation..