Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor of Technology
in
Electronics and Communication Engineering

by

Nehil Sood 19UEC036

Course Coordinator
Dr. Kusum Lata

Department of Electronics and Communication Engineering
The LNM Institute of Information Technology, Jaipur

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Contents

Chapter *1*

Experiment - 1

1.1 Aim

Design, simulate and implement Half adder, Full adder using dataflow, behavioral and structural modeling in VHDL.

1.2 Theory

1.2.1 Half Adder

Half Adder adds two binary digits where the input bits are termed as augend and addend and the result will be two outputs one is the sum and the other is carry.To perform the sum operation, XOR is applied to both the inputs, and AND gate is applied to both inputs to produce carry.

1.2.2 Full Adder

In the full adder circuit, it adds 3 one-bit numbers, where two of the three bits can be referred to as operands and the other is termed as bit carried in. The produced output is 2-bit output and these can be referred to as output carry and sum.

1.3 Coding Techniques used

Firstly Half Adder was implemented using Dataflow modelling. Dataflow modelling describes the archi- tecture of the entity without describing its components in terms of flow of data from input towards output.

Then Half Adder was implemented using Behavioral modelling.In Behavioral modelling, the behaviour of the entity is expressed using sequentially executed. Further we implemented Full Adder using Dataflow and Behavioural.Lastly we implemented Full Adder using Structural Modelling. In this modelling we used small structures. We used the half adder as a component and implemented full adder using it.

1.4 Simulation and Results

1.4.1 Half Adder using Dataflow

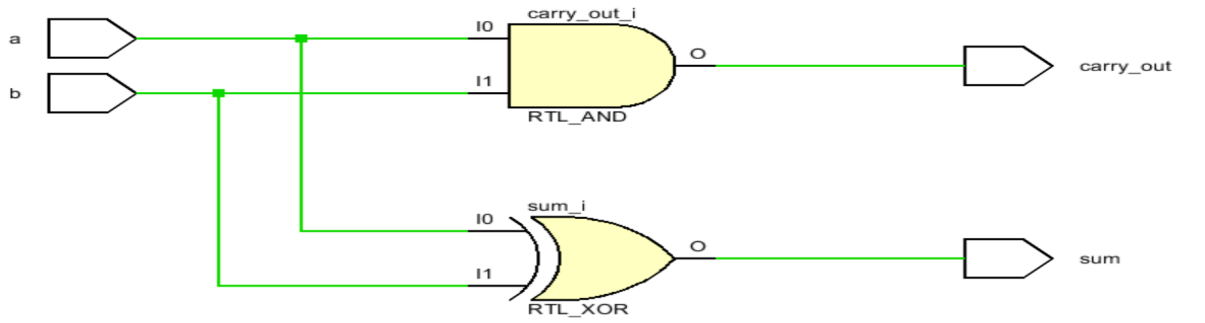

Figure 1.1: Schematic of the Half adder using Dataflow modeling

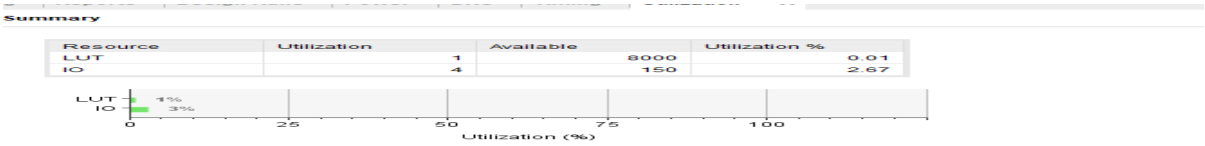

Figure 1.2: Project Summary of the Half adder using Dataflow modeling

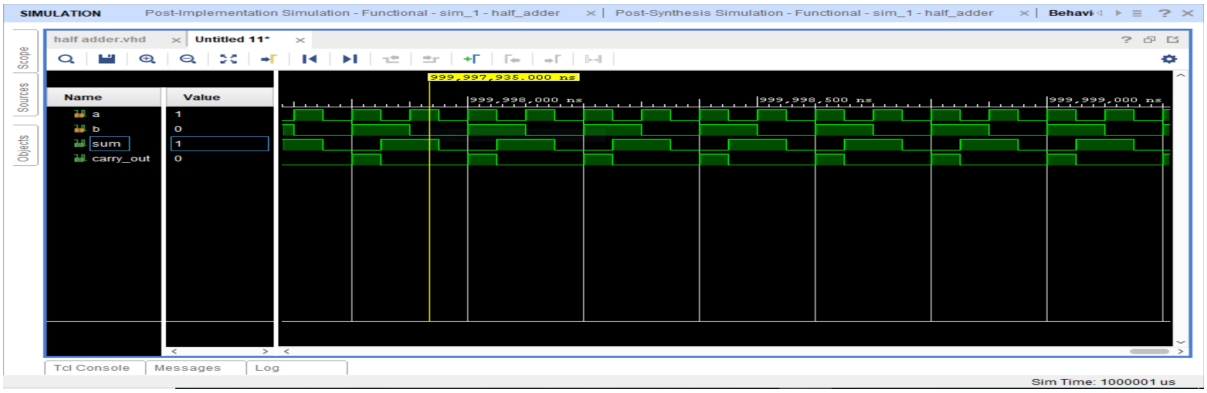

Figure 1.3: Simulation of the Half adder using Dataflow modeling

1.4.2 Half Adder using Behavioural

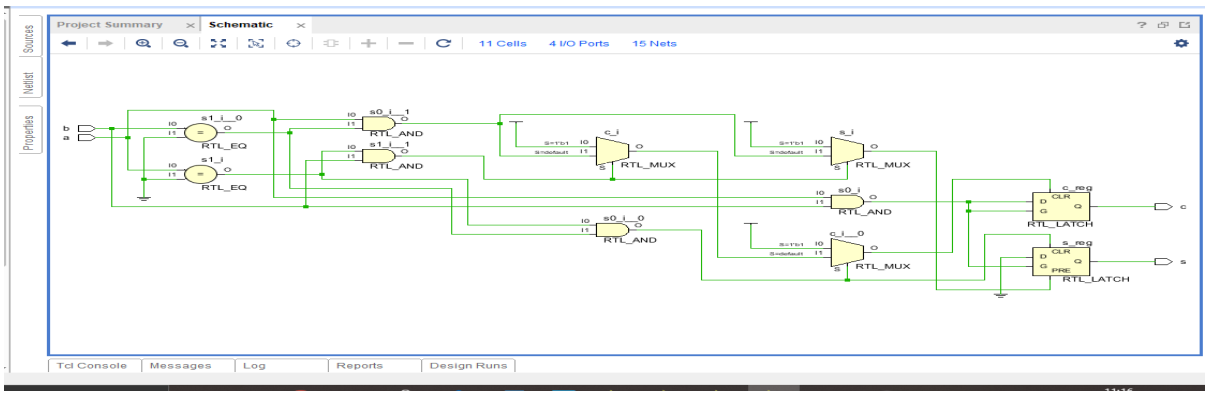

Figure 1.4: Schematic of the Half adder using Behavioural modeling

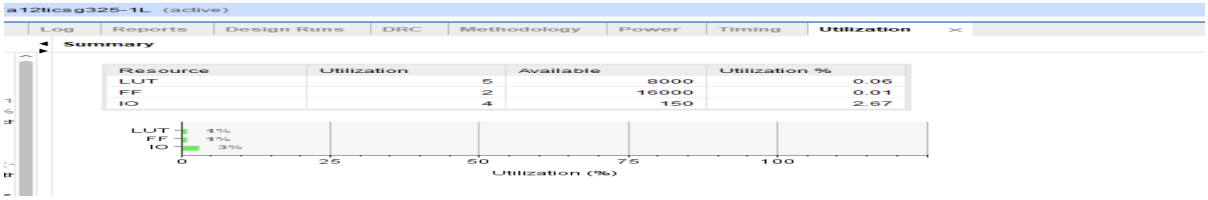

Figure 1.5: Project Summary of the Half adder using Behavioural modeling

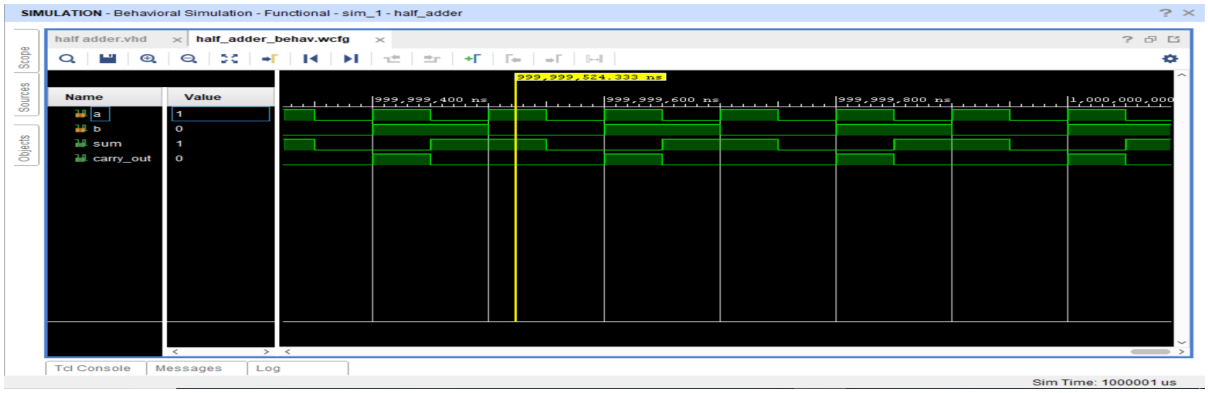

Figure 1.6: Simulation of the Half adder using Behavioural modeling

1.4.3 Full Adder using Dataflow

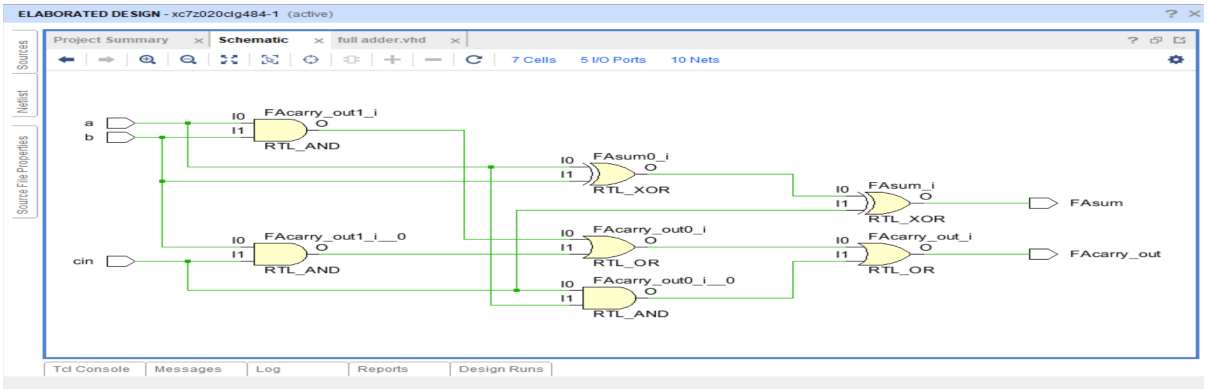

Figure 1.7: Schematic of the Full adder using Dataflow modeling

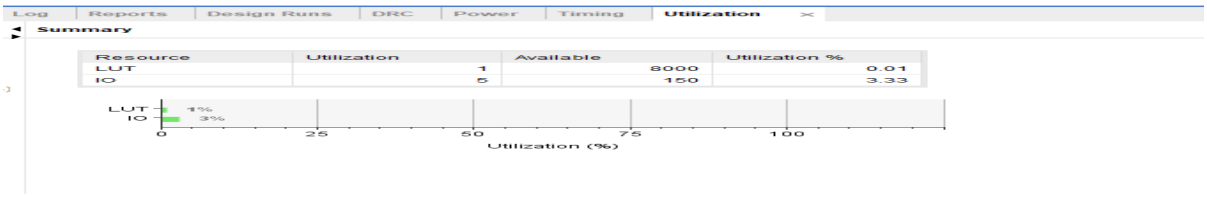

Figure 1.8: Project Summary of the Full adder using Dataflow modeling

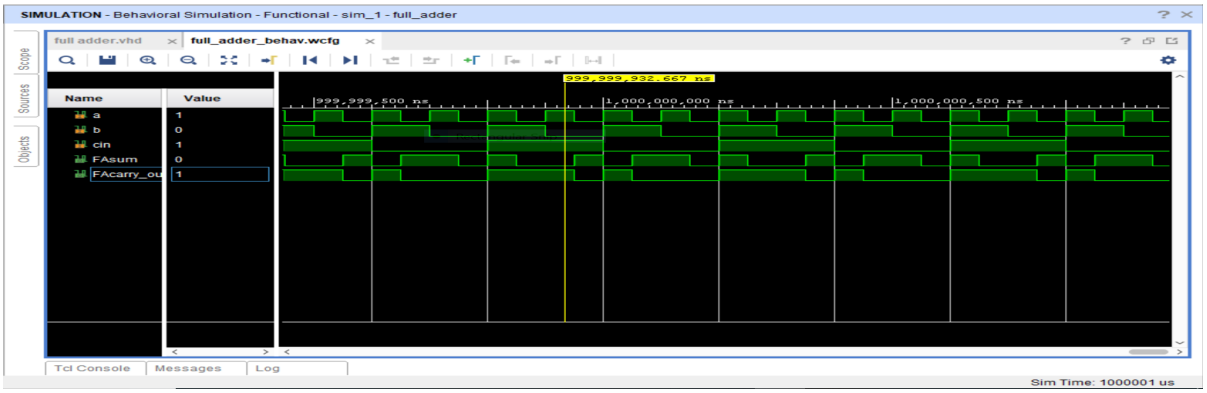

Figure 1.9: Simulation of the Full adder using Dataflow modeling

1.4.4 Full Adder Using Behavioural modeling

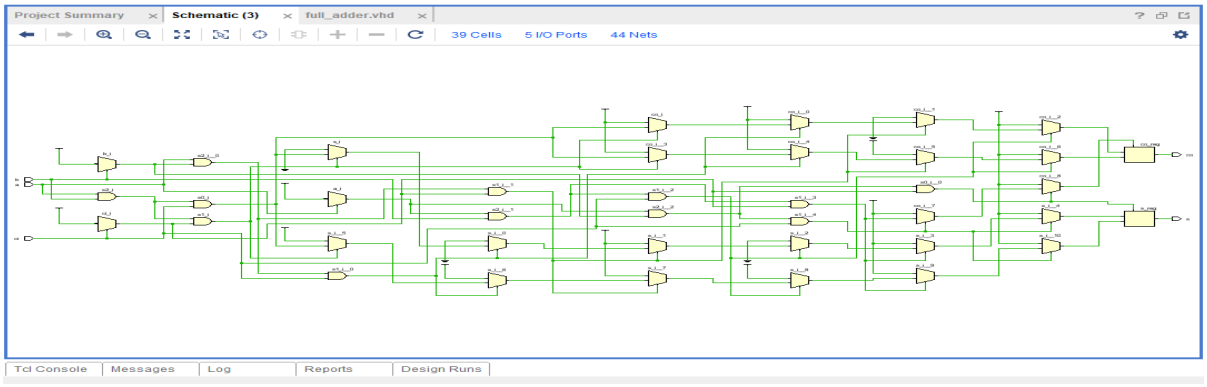

Figure 1.10: Schematic of the Full adder using Behavioural modeling

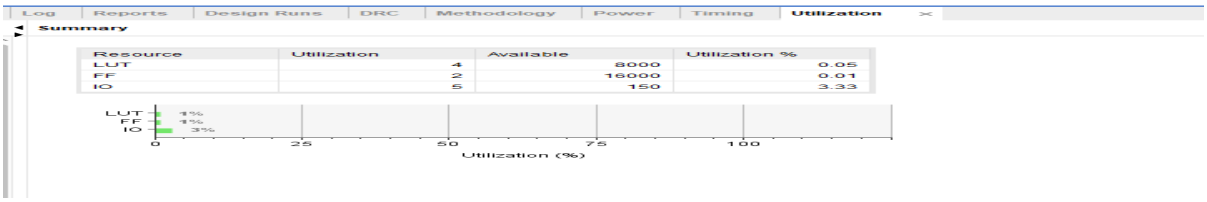

Figure 1.11: Project Summary of the Full adder using Behavioural modeling

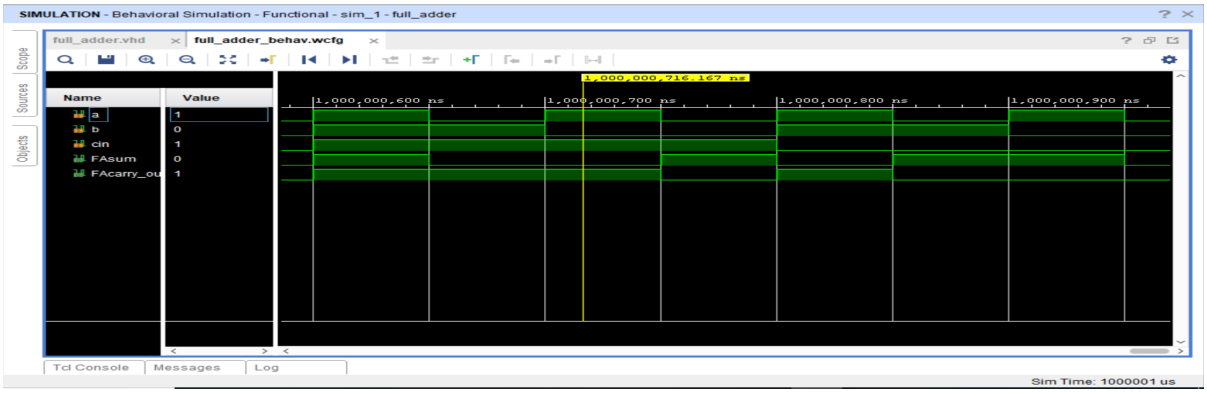

Figure 1.12: Simulation of the Full adder using Behavioural modeling

1.4.5 Full adder Using Structural

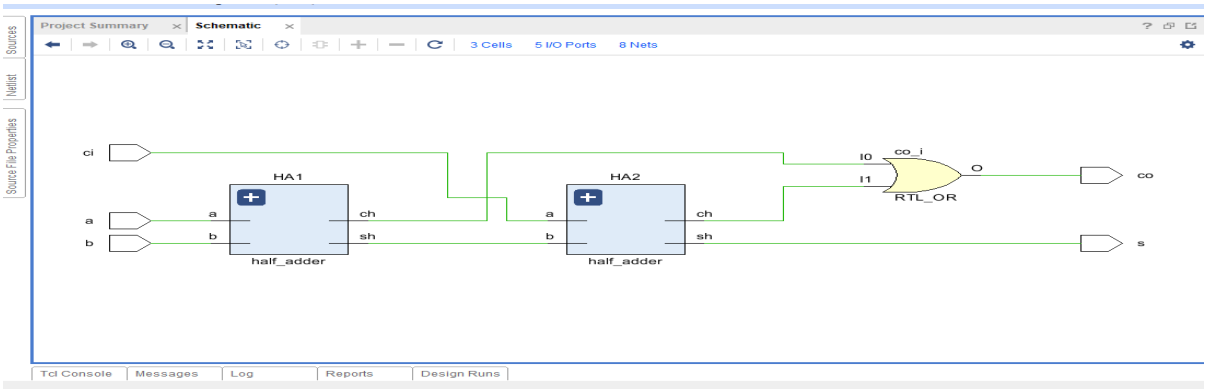

Figure 1.13: Schematic of the Full adder using Structural modeling

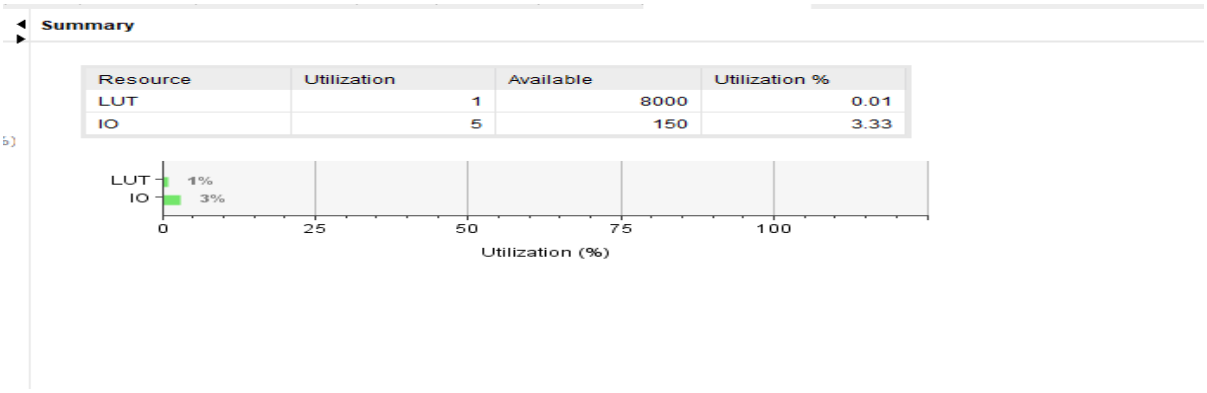

Figure 1.14: Project Summary of the Full adder using Structural modeling

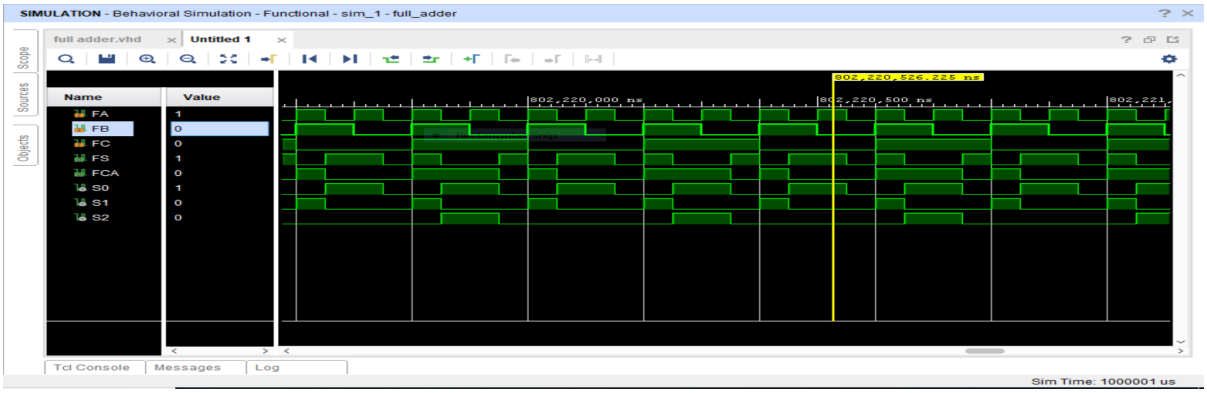

Figure 1.15: Simulation of the Full adder using Structural modeling

1.5 Summary

Name of the Entity	No. of LUT used(in percentage)	Total On chip Power(in Watt)
Half Adder using Dataflow	1	0.721
Half Adder using Behavioural	5	0.208
Full Adder using Dataflow	1	0.956
Full Adder using Behavioural	4	0.101
Full Adder using Structural	1	0.957

Table 1.1 comparision of Area and power requirements for different kinds of adders.