Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor in
Electronics and Communication Engineering

by

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Chapter *6*

Experiment - 6

6.1 Name of the Experiment

Design D latch , D flip flop, JK flip flop, RS flip flop and T flip flop using dataflow and behavioral and structural modeling.

6.2 Theory

Latches and flip-flops are the basic elements for storing information. One latch or flip-flop can store one bit of information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their inputs change. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes. There are basically four main types of latches and flip-flops: SR, D, JK, and T. The major differences in these flip-flop types are the number of inputs they have and how they change state. For each type, there are also different variations that enhance their operations. In this chapter, we will look at the operations of the various latches and flip-flops.

6.3 Coding Techniques used

We use all of the coding techniques, which are: Dataflow, Behavioral and Structural.

6.4 Simulation and Results

6.4.1 Implement D latch using dataflow modeling.

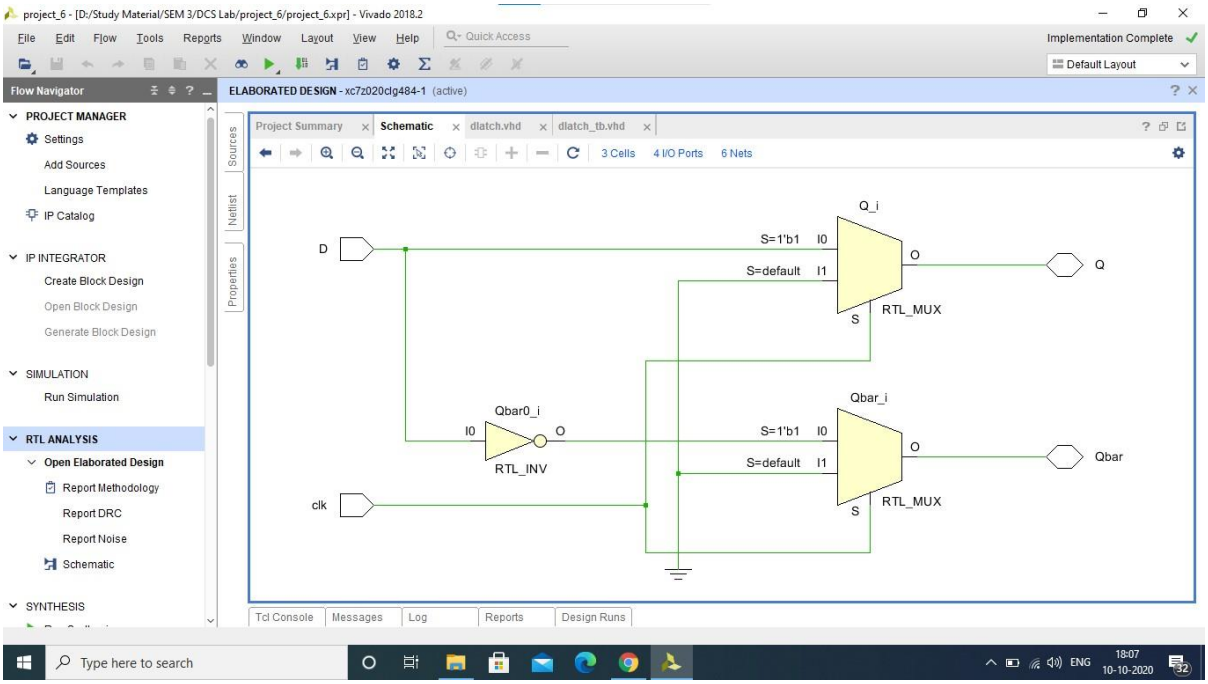

Figure 6.1 Schematic of D latch using dataflow modeling

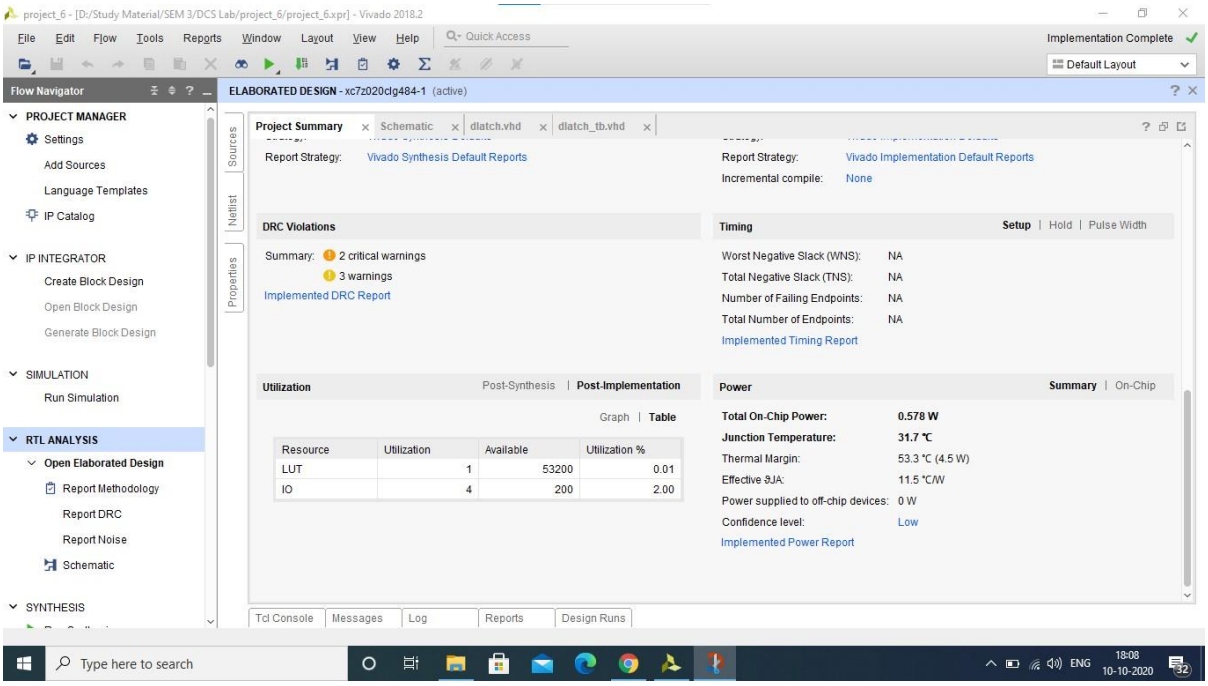

Figure 6.2 Project Summary of D latch using dataflow modeling

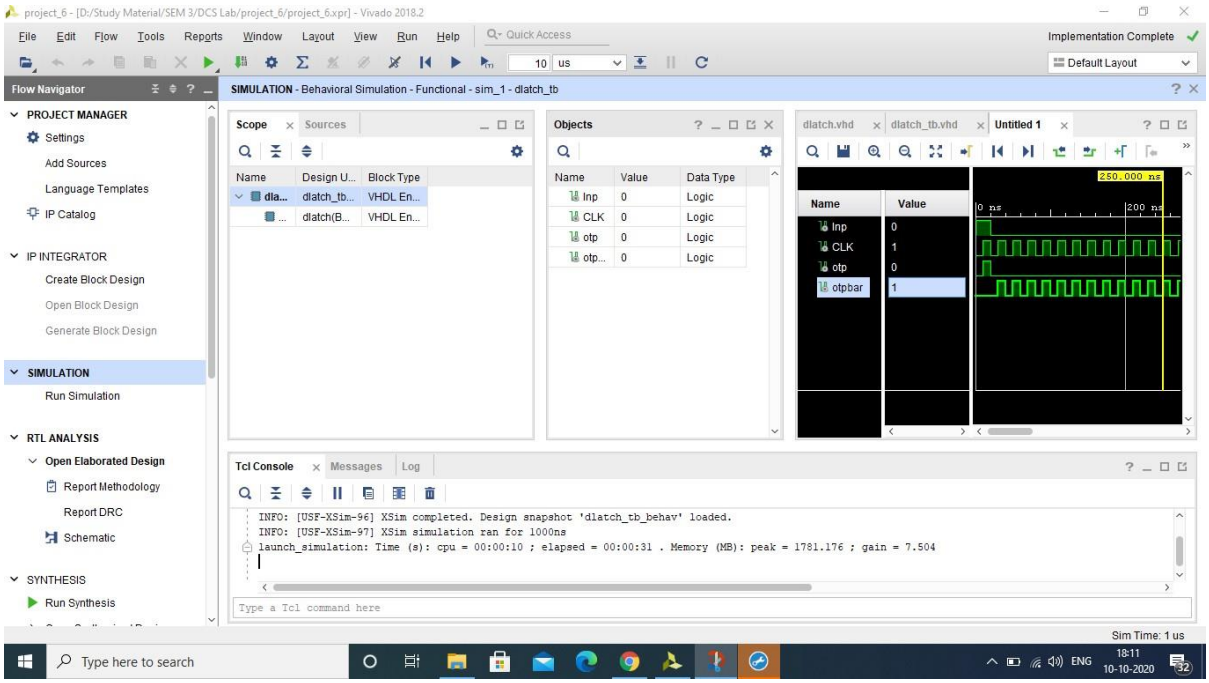

Figure 6.3 Simulation of D latch using dataflow modeling

6.4.2 Implement D flip flop using behavioral modeling.

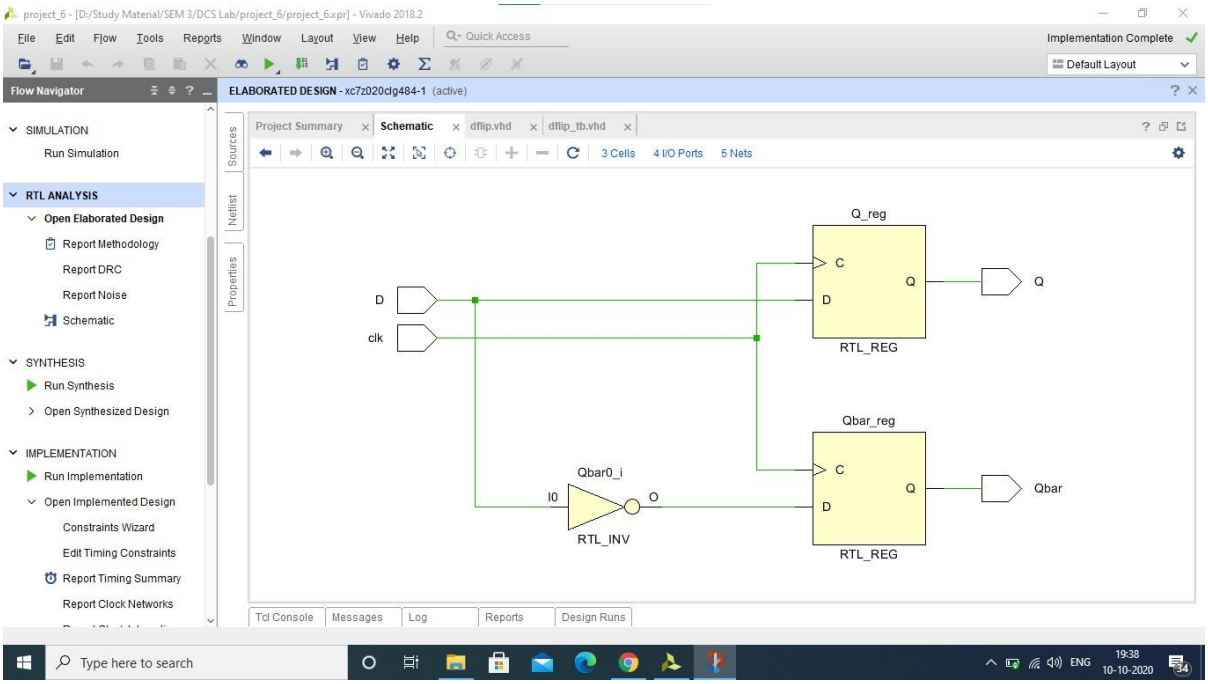

Figure 6.4 Schematic of D flip flop using behavioral modeling

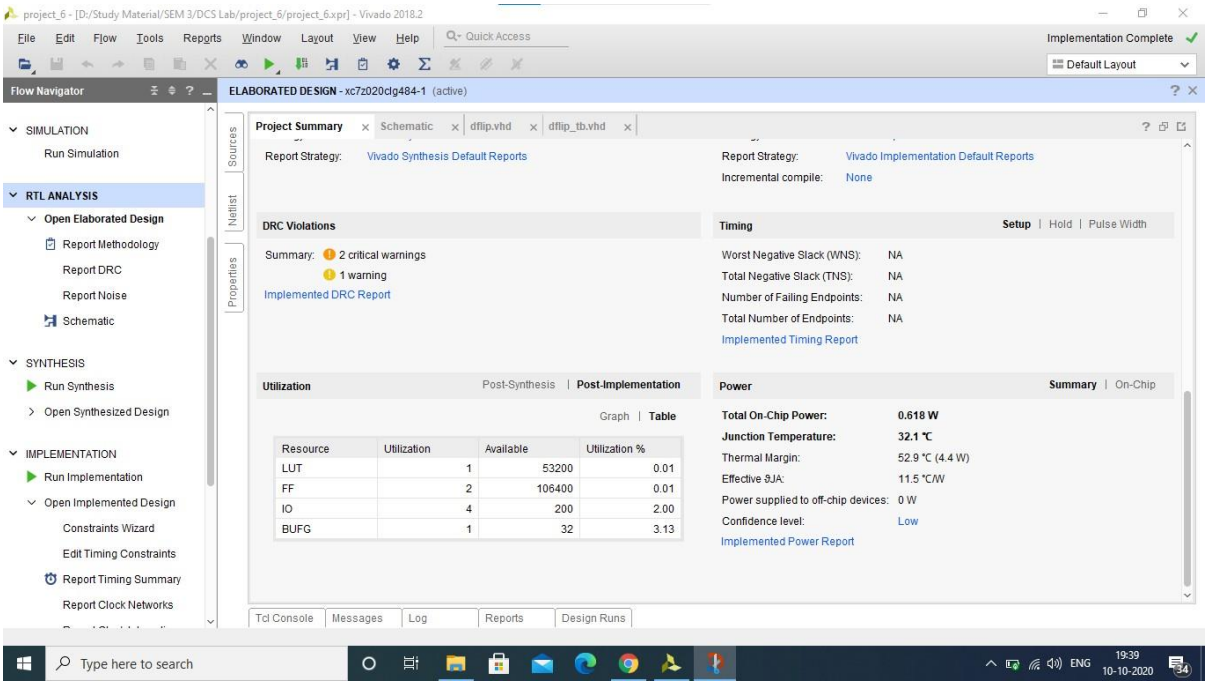

Figure 6.5 Project Summary of D flip flop using behavioral modeling

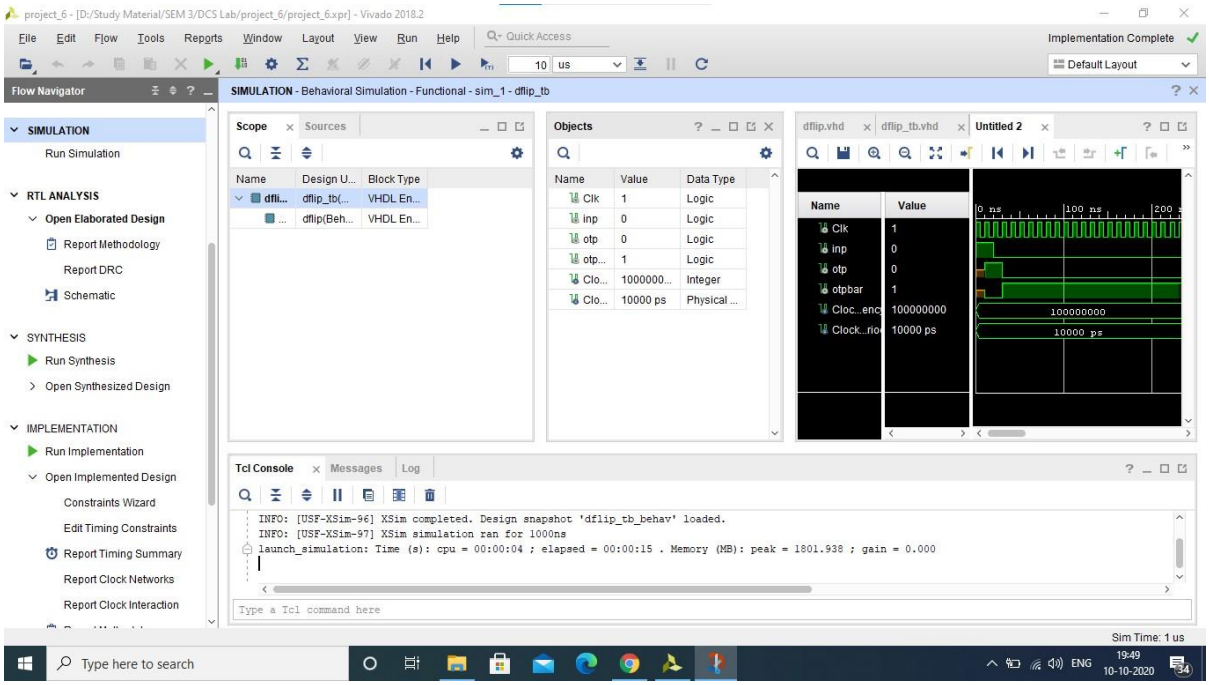

Figure 6.6 Simulation of D flip flop using behavioral modeling

6.4.3 Implement JK flip flop using structural modeling.

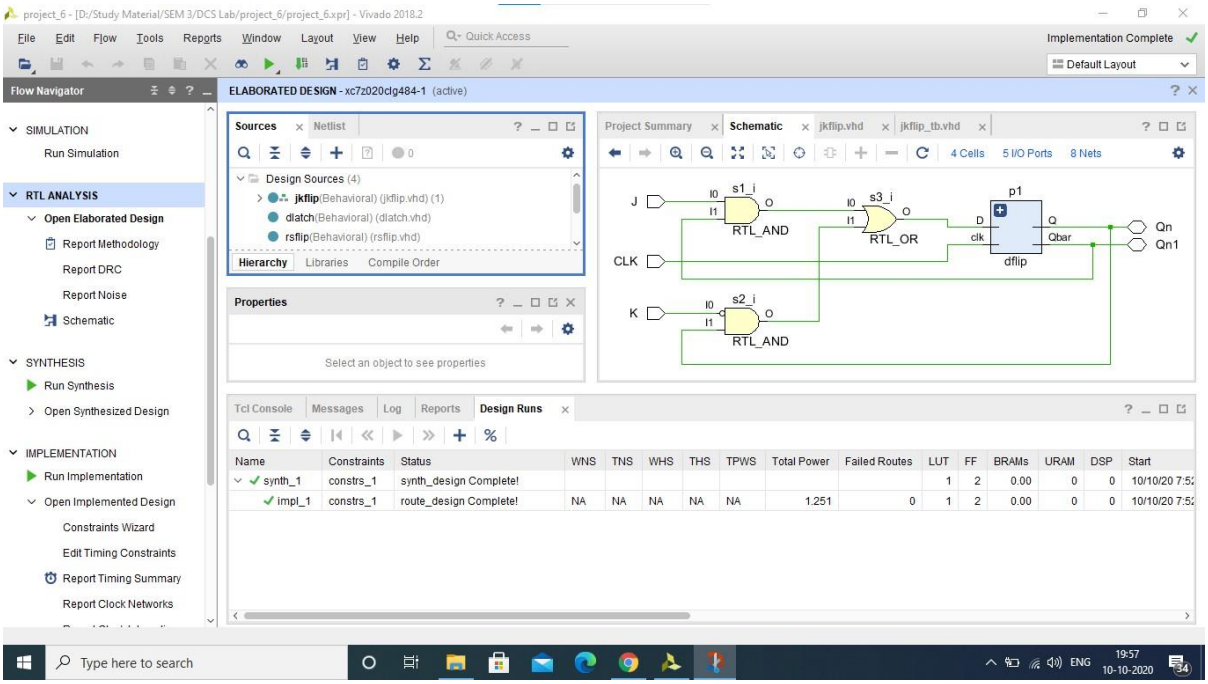

Figure 6.7 Schematic of JK flip flop using structural modeling

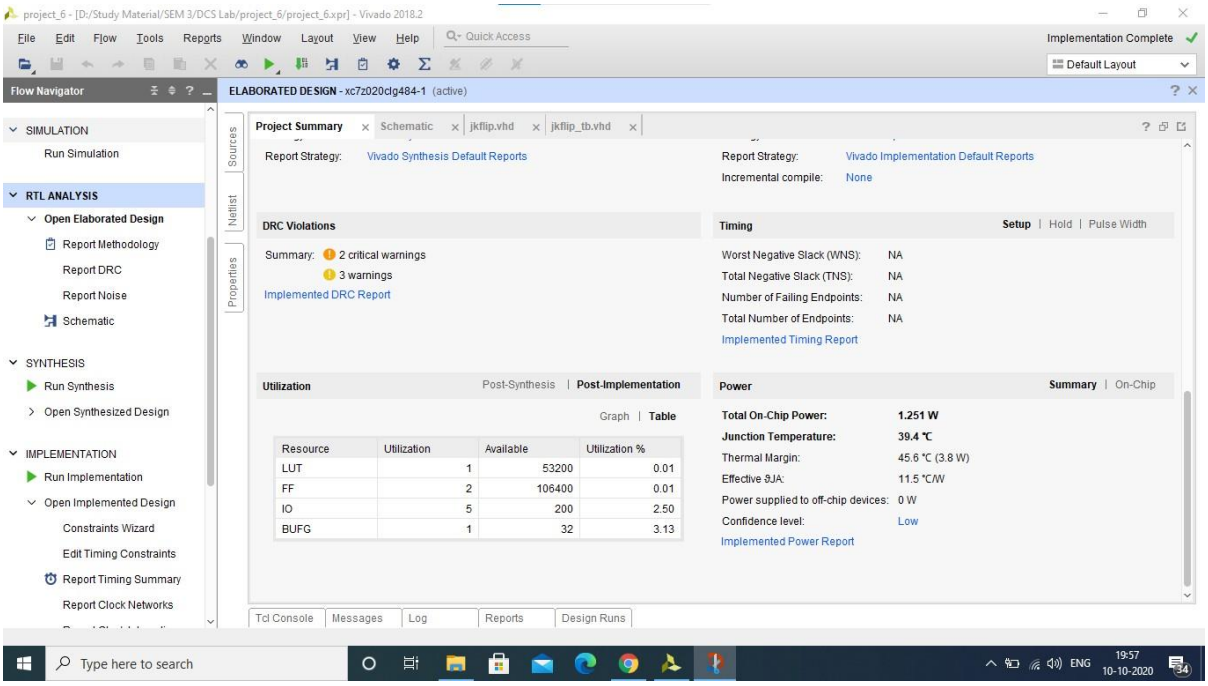

Figure 6.8 Project Summary of JK flip flop using structural modeling

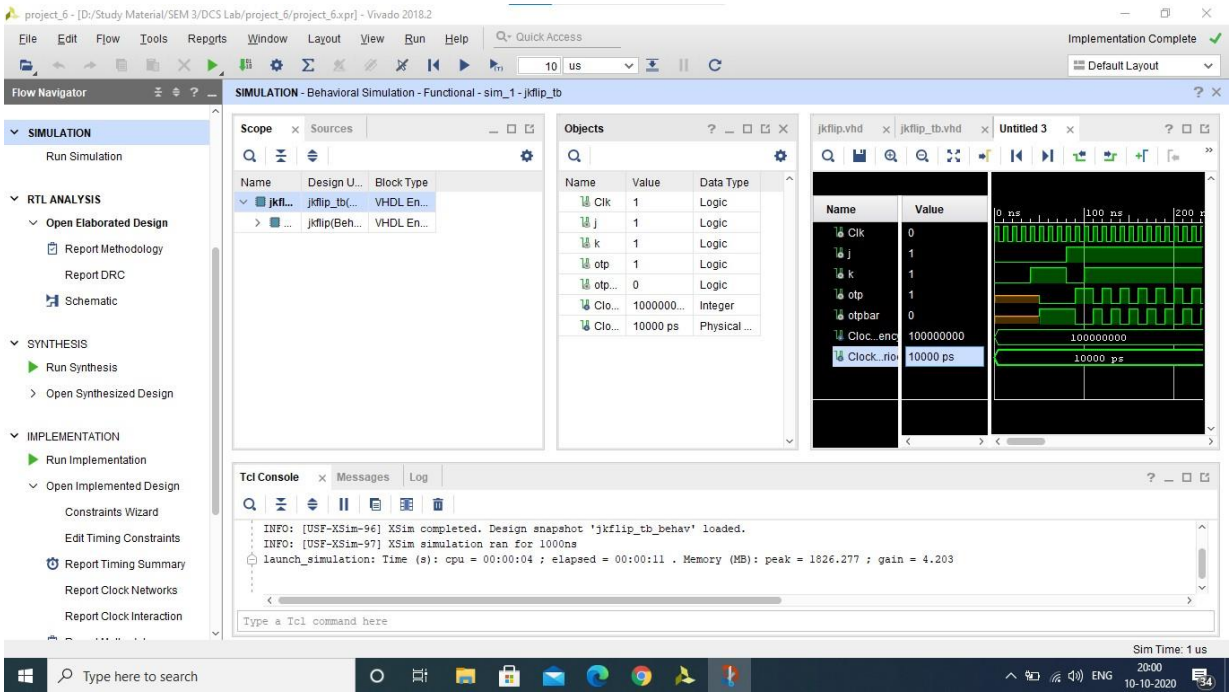

Figure 6.9 Simulation of JK flip flop using structural modeling

6.4.4 Implement RS flip flop using behavioral modeling.

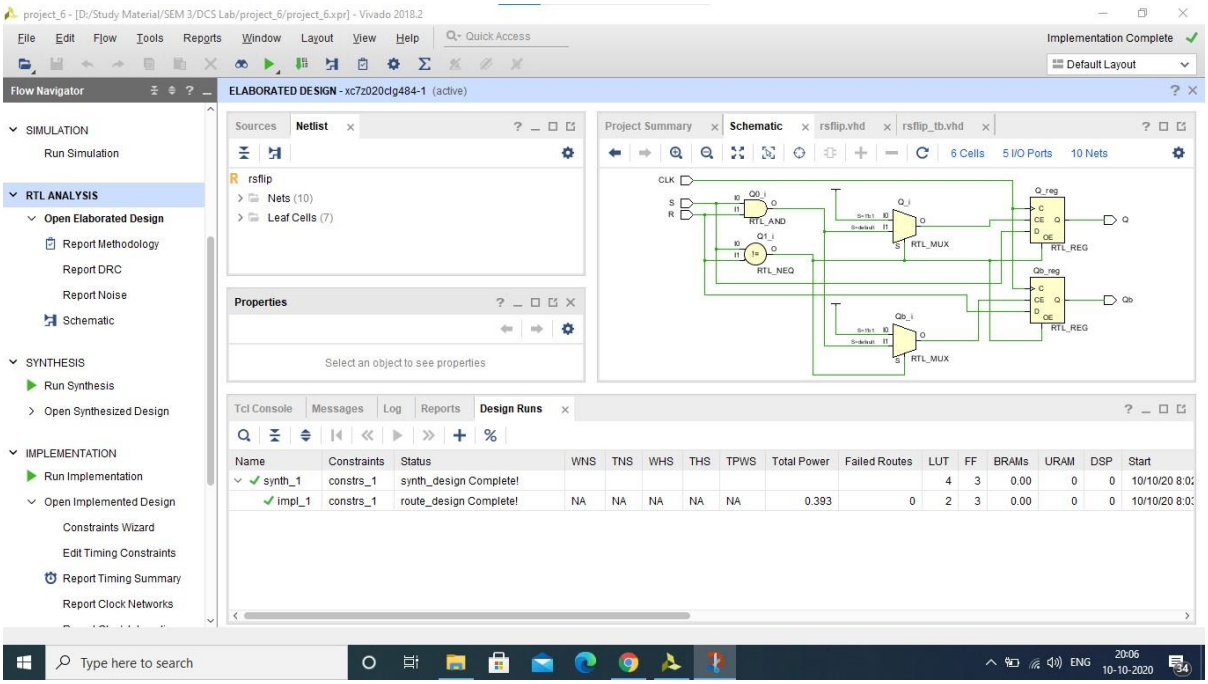

Figure 6.10 Schematic of RS flip flop using behavioral modeling

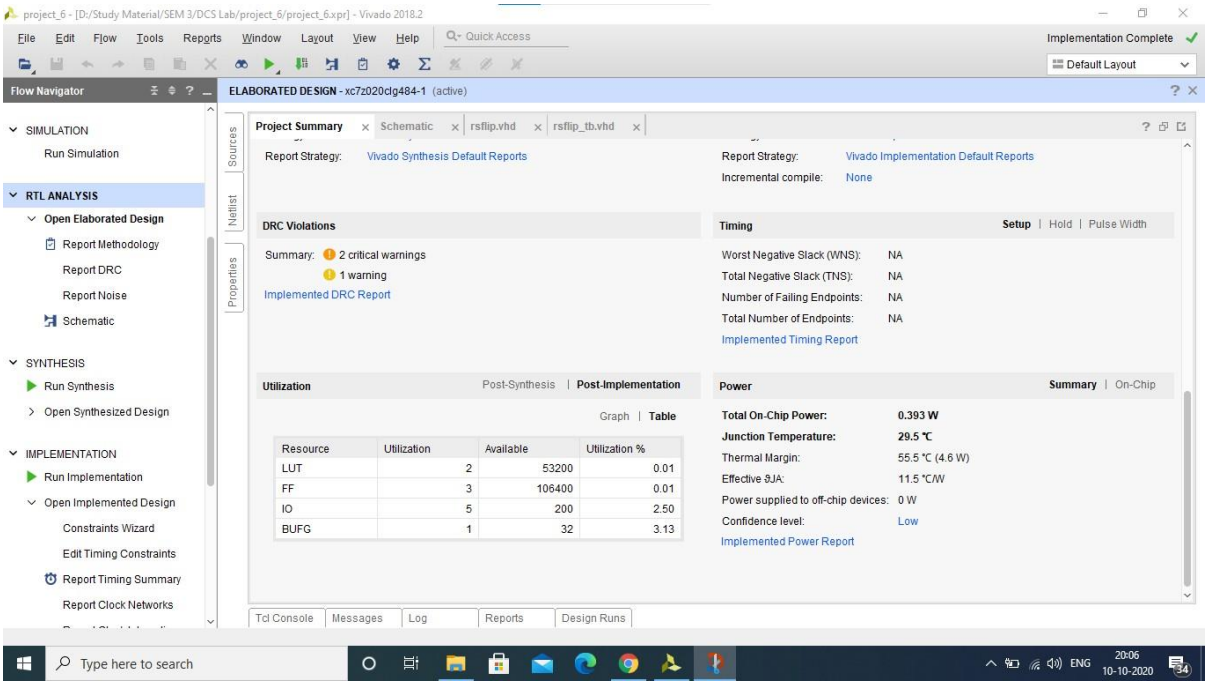

Figure 6.11 Project Summary of RS flip flop using behavioral modeling

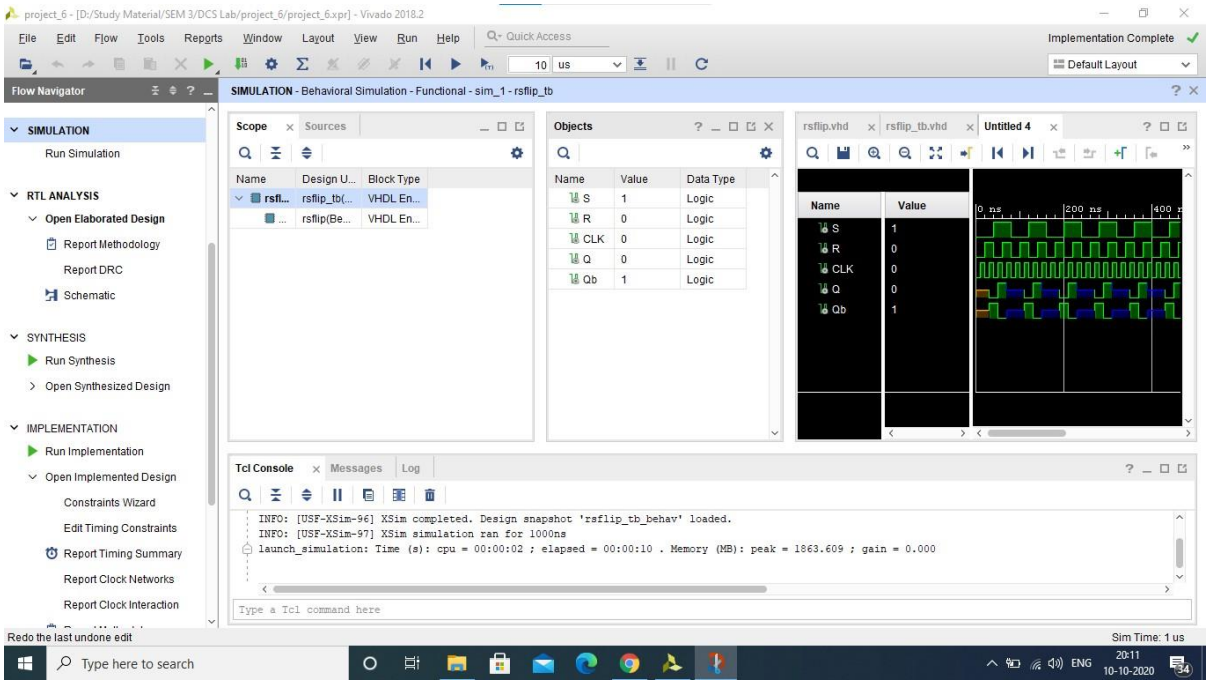

Figure 6.12 Simulation of RS flip flop using behavioral modeling

6.4.5 Implement T flip flop using behavioral modeling.

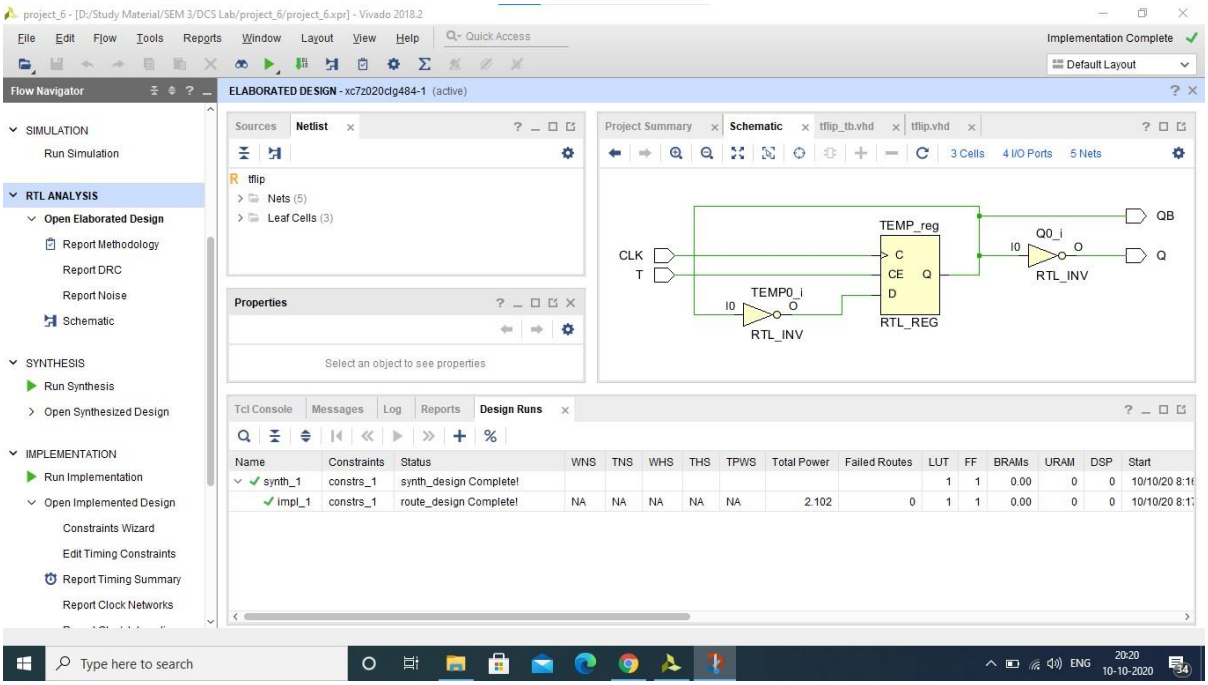

Figure 6.13 Schematic of T flip flop using behavioral modeling

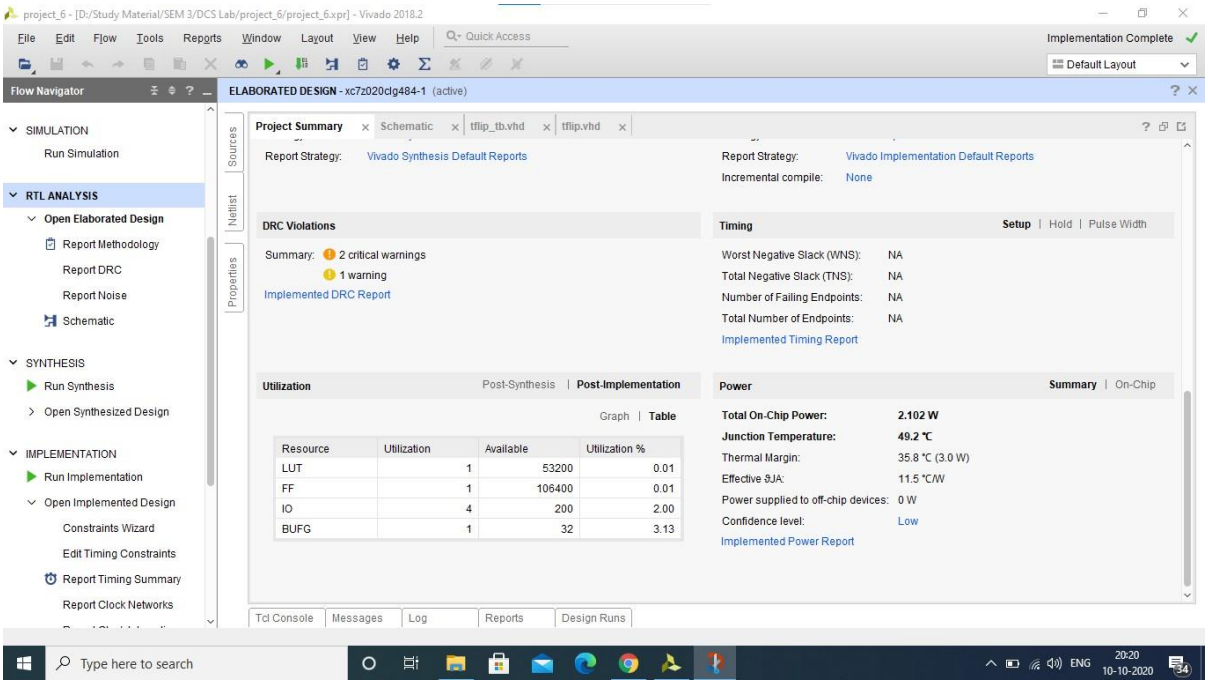

Figure 6.14 Project Summary of T flip flop using behavioral modeling

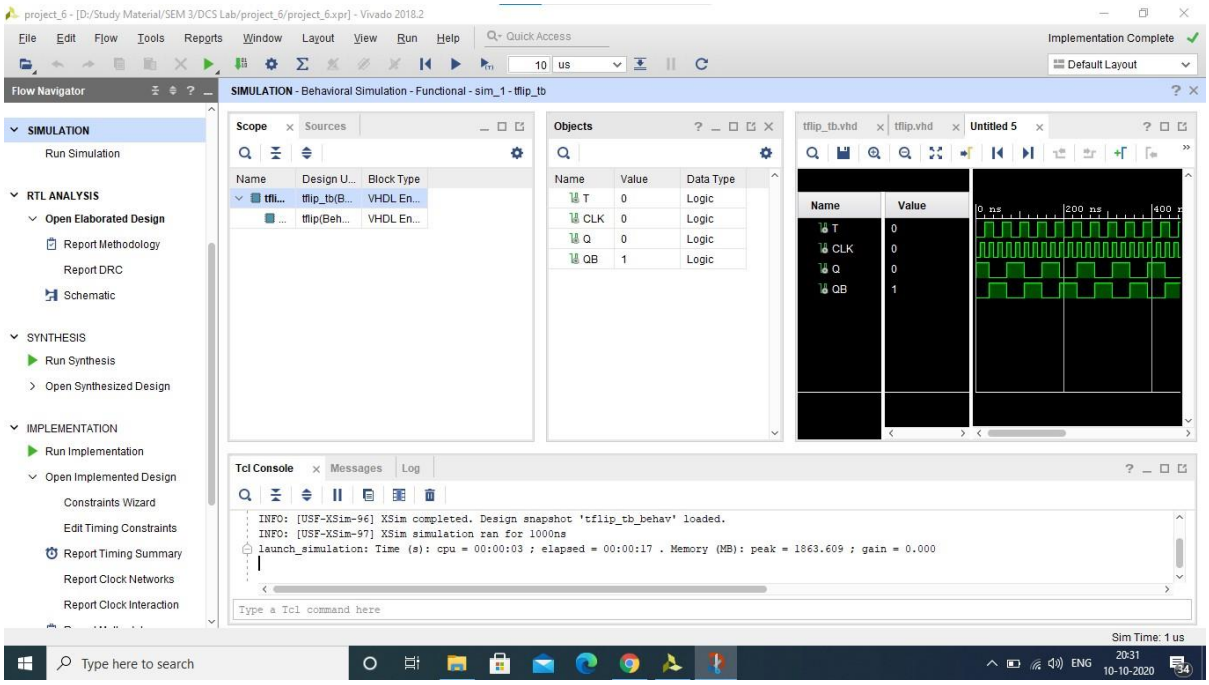

Figure 6.15 Simulation of T flip flop using behavioral modeling

6.5 Summary

Name of the Entity	No. of LUT used	Total On Chip Power
D latch using dataflow modeling	1	0.578W
D flip flop using behavioral modeling.	1	0.618W
JK flip flop using structural modeling	1	1.251W
RS flip flop using behavioral modeling	2	0.393W
T flip flop using behavioral modeling	1	2.102W

Table 6.1 Comparison of Area and power requirements for different kinds of adders.