Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor of Technology
in
Electronics and Communication Engineering

by

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Chapter *1*

Experiment - 7

1.1 Aim

Shift Register Design Using VHDL.

1.2 Description

1.2.1

Write a VHDL code for 8-bit Shift-Left Register with Negative-Edge Clock, Clock Enable, Serial In, and Serial Out. In your testbench show at least 25 cycles and starts loading the data 10001111000111000011001100. Confirm with the help of simulation that the same data is output at Serial Out after 8 cycles.

1.2.2

Repeat the problem statement of part A by adding an extra reset input signal. If reset is 1 then the current state of register becomes 00000000. Load the same serial input data and provide reset = 1 for t = 10 and 19. C. Write a VHDL code

1.2.3

Write a VHDL code for 8-bit Shift-Left Register with Positive-Edge Clock, Serial In, and Parallel Out. In your testbench show at least 25 cycles and starts loading the data 10001111000111000011001100. Confirm with the help of simulation that the same data is output at Parallel Out after 8 cycles.

1.2.4

Write a VHDL code for 16 bit Shift-Left Register with Positive-Edge Clock, Serial In, and Parallel Out. Take 2 different 8-bit Shift-Left Registers as component and implement the final 16 Bit register. Show at least 40 cycles in your testbench and load the data 1000111100011100011001100 serially starting from t =0.

1.3 Theory

A shift register basically consists of several single bit “D-Type Data Latches”, one for each data bit, either a logic “0” or a “1”, connected together in a serial type daisy-chain arrangement so that the output

from one data latch becomes the input of the next latch and so on.

Data bits may be fed in or out of a shift register serially, that is one after the other from either the left or the right direction, or all together at the same time in a parallel configuration.

The number of individual data latches required to make up a single Shift Register device is usually determined by the number of bits to be stored with the most common being 8-bits (one byte) wide constructed from eight individual data latches.

Shift Registers are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format. The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices.

Shift register IC's are generally provided with a clear or reset connection so that they can be "SET" or "RESET" as required. Generally, shift registers operate in one of four different modes with the basic movement of data through a shift register being:

Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.

Serial-in to Serial-out (SISO) - the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.

Parallel-in to Serial-out (PISO) - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.

Parallel-in to Parallel-out (PIPO) - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

1.4 Coding Techniques used

We use all of the coding techniques, which are: Dataflow, Behavioral and Structural.

1.5 Simulation and Results

1.5.1 Implement 8-bit Shift-Left Register with Negative-Edge Clock, Clock Enable, Serial In, and Serial Out.

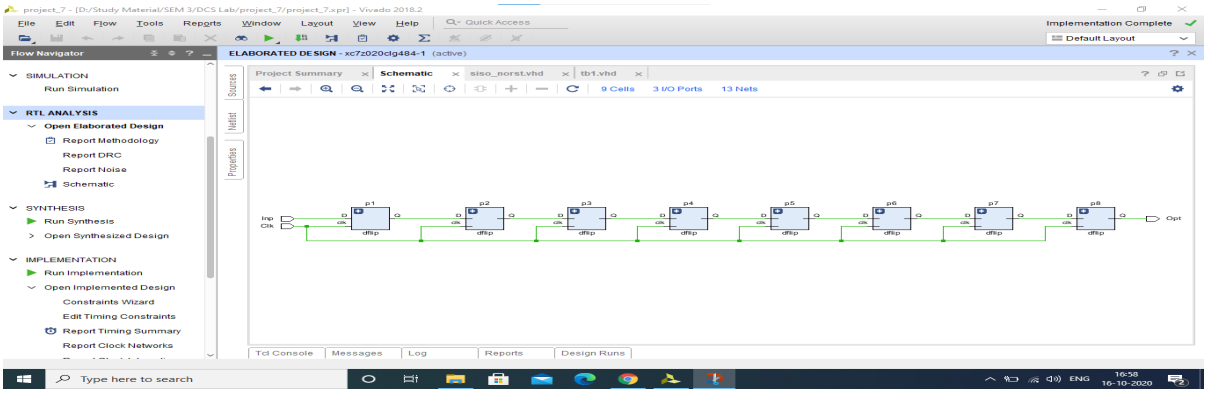

Figure 1.1: Schematic of 8-bit Shift-Left Register with Negative-Edge Clock, Clock Enable, Serial In, and Serial Out

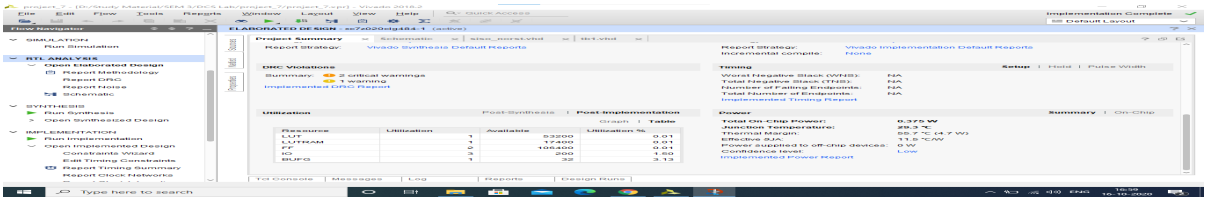

Figure 1.2: Project Summary of 8-bit Shift-Left Register with Negative-Edge Clock, Clock Enable, Serial In, and Serial Out

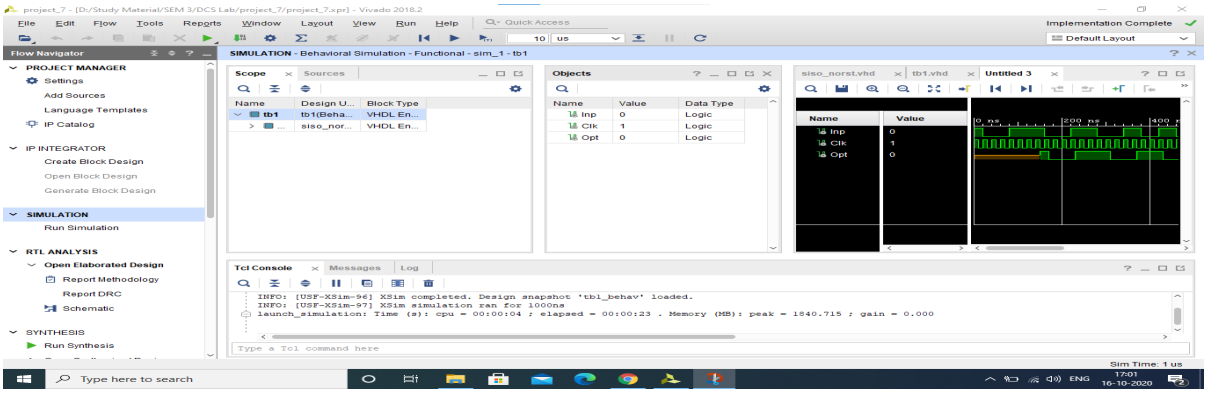

Figure 1.3: Simulation of 8-bit Shift-Left Register with Negative-Edge Clock, Clock Enable, Serial In, and Serial Out

1.5.2 Implement 8-bit Shift-Left Register with Negative-Edge Clock, Clock Enable, Serial In, and Serial Out by adding an extra reset input signal.

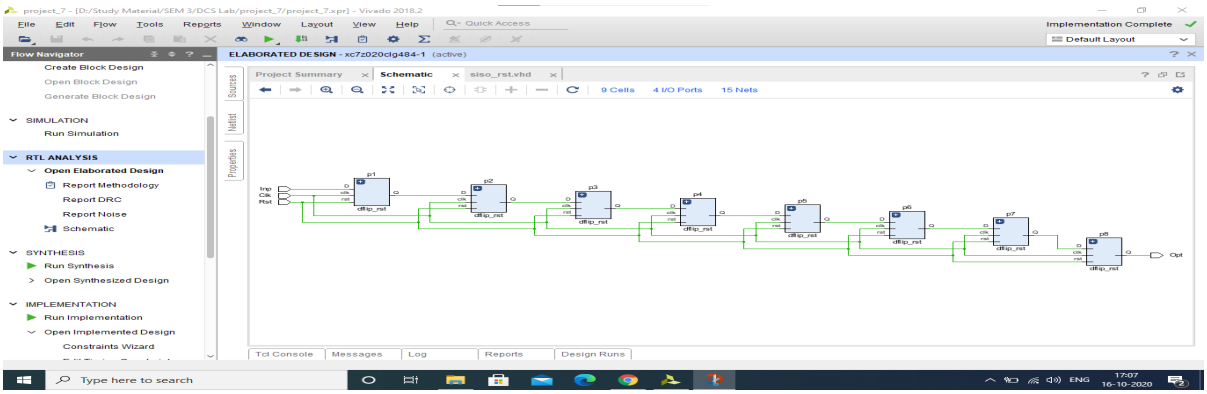

Figure 1.4: Schematic of 8-bit Shift-Left Register with Negative-Edge Clock, Clock Enable, Serial In, and Serial Out by adding an extra reset input signal

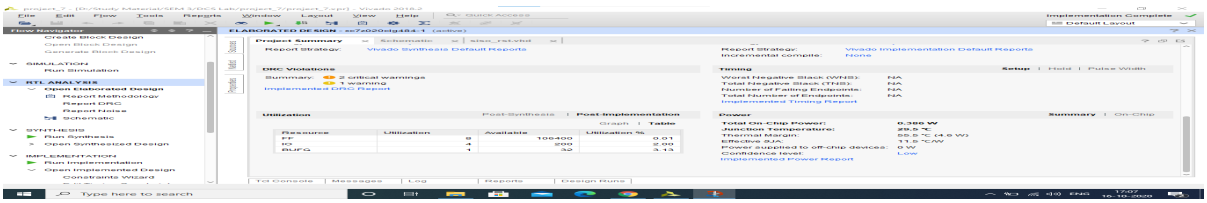

Figure 1.5: Project Summary of 8-bit Shift-Left Register with Negative-Edge Clock, Clock Enable, Serial In, and Serial Out by adding an extra reset input signal

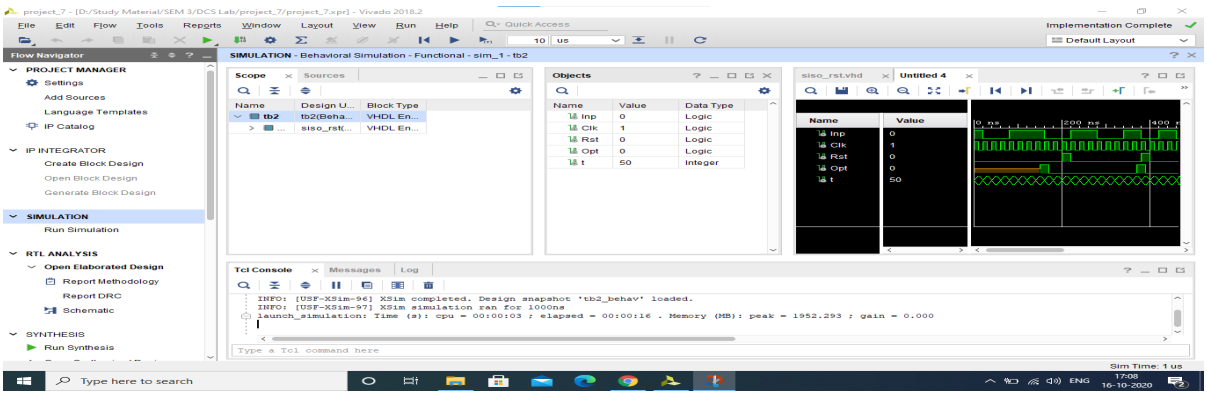

Figure 1.6: Simulation of 8-bit Shift-Left Register with Negative-Edge Clock, Clock Enable, Serial In, and Serial Out by adding an extra reset input signal

1.5.3 Implement 8-bit Shift-Left Register with Positive-Edge Clock, Serial In, and Parallel Out.

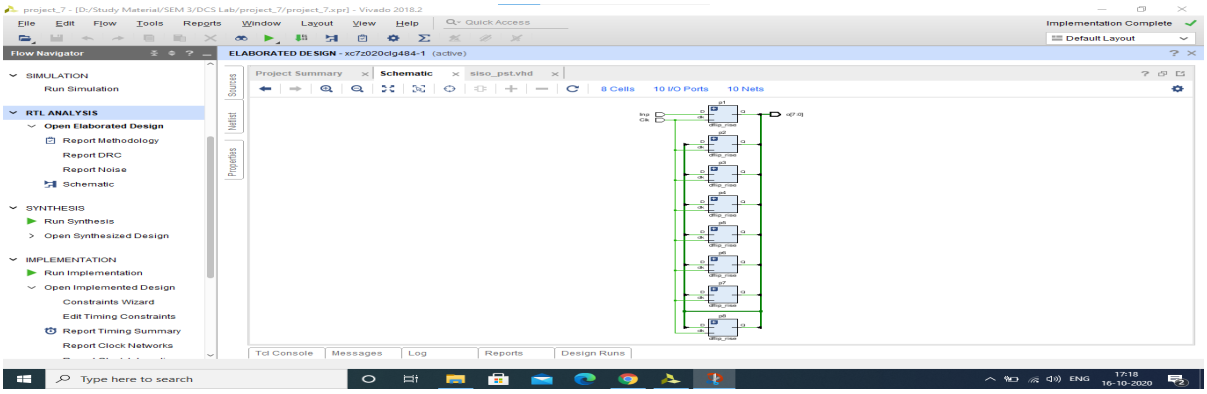

Figure 1.7: Schematic of 8-bit Shift-Left Register with Positive-Edge Clock, Serial In, and Parallel Out

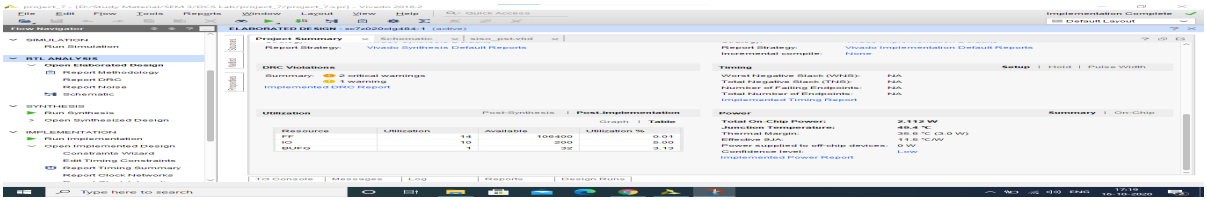

Figure 1.8: Project Summary of 8-bit Shift-Left Register with Positive-Edge Clock, Serial In, and Parallel Out

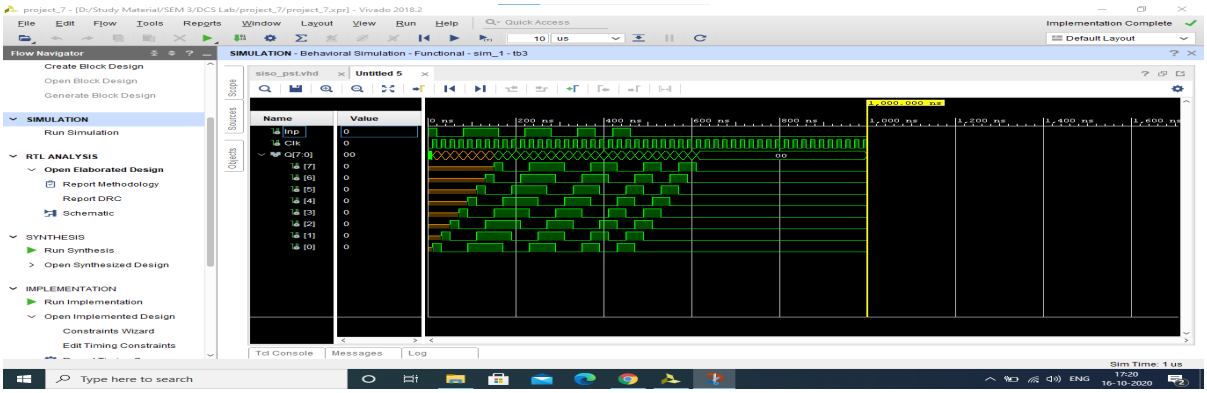

Figure 1.9: Simulation of 8-bit Shift-Left Register with Positive-Edge Clock, Serial In, and Parallel Out

1.5.4 Implement 16 bit Shift-Left Register with Positive-Edge Clock, Serial In, and Parallel Out.

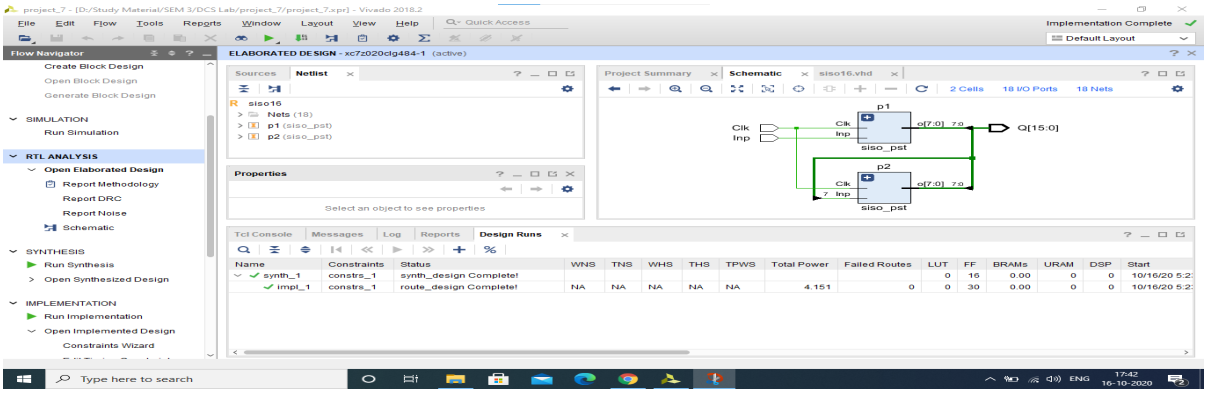

Figure 1.10: Schematic of 16 bit Shift-Left Register with Positive-Edge Clock, Serial In, and Parallel Out

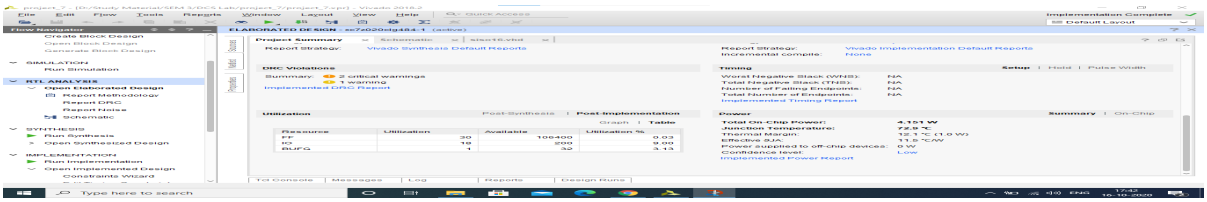

Figure 1.11: Project Summary of 16 bit Shift-Left Register with Positive-Edge Clock, Serial In, and Parallel Out

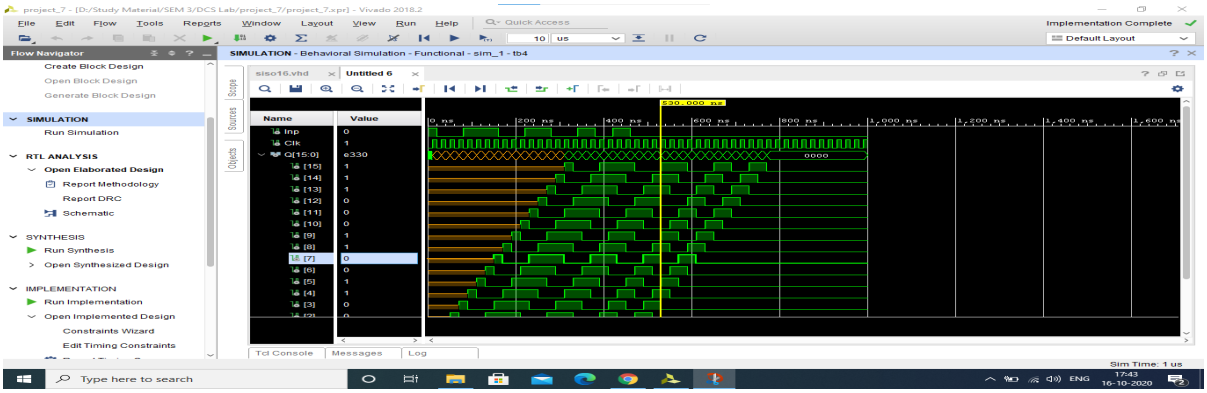

Figure 1.12: Simulation of 16 bit Shift-Left Register with Positive-Edge Clock, Serial In, and Parallel Out

1.6 Summary

Name of the Entity	No. of LUT used	Total On Chip Power
8-bit Shift-Left Register with Positive Edge-Clock, SISO	1	0.38W
8-bit Shift-Left Register with SISO and an extra reset input signal	0	0.39W
8-bit Shift-Left Register with Positive Edge-Clock, SIPO	0	2.12W
16 bit Shift-Left Register with Positive Edge-Clock, SIPO	0	4.15W

Table 1.1 Comparison of Area and power requirements for different kinds of adders.