Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor of Technology
in
Electroincs and Communication Engineering

by

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Contents

Chapter *1*

Experiment - 4

1.1 Aim

Implement 4 bit ripple carry adder using structural modeling. Implement 4 bit adder/subtractor using structural modeling.

1.2 Theory

4 bit Ripple Carry Adder. Ripple carry adder is a combinational logic circuit used for the purpose of adding two n-bit binary numbers. 4-bit ripple carry adder is used for adding two 4-bit binary numbers. N-bit ripple carry adder is used for adding two N-bit binary numbers.

In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs.

Propagation delays inside the logic circuitry is the reason behind this. Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output.

Illustrating the delay of the carry bit. The disadvantage of the ripple-carry adder is that it can get very slow when one needs to add many bits. To reduce the computation time, there are faster ways to add two binary numbers by using carry look ahead adders.

1.3 Coding Techniques used

First of all we implement a binary adder precisely a four-bit adder using full adders (by Structural Modelling).
Second and at last we implement a binary adder/subtractor precisely a four-bit adder/subtractor using full adders (by Structural Modelling).

1.4 Simulation and Results

1.4.1 4-bit adder using Structural Modelling

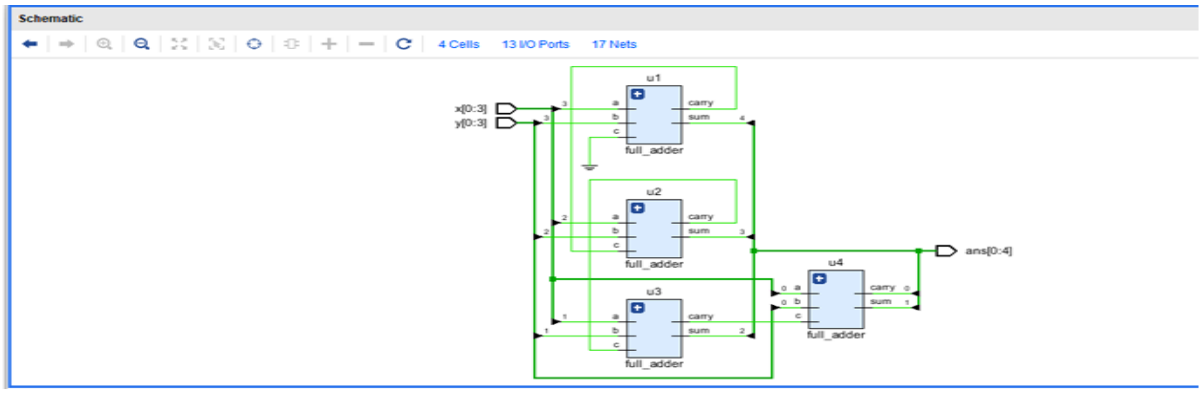

Figure 1.1 Schematic of the 4-bit adder

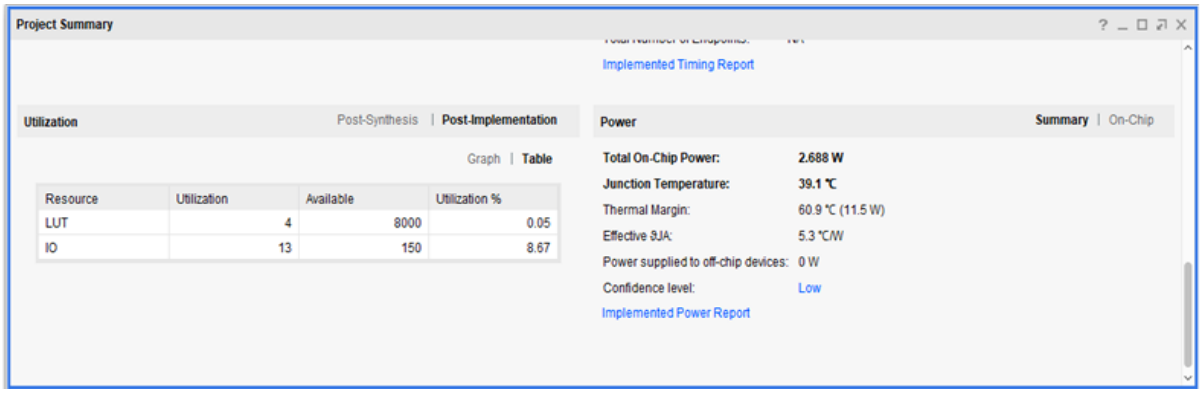

Figure 1.2 Project Summary of the 4-bit adder

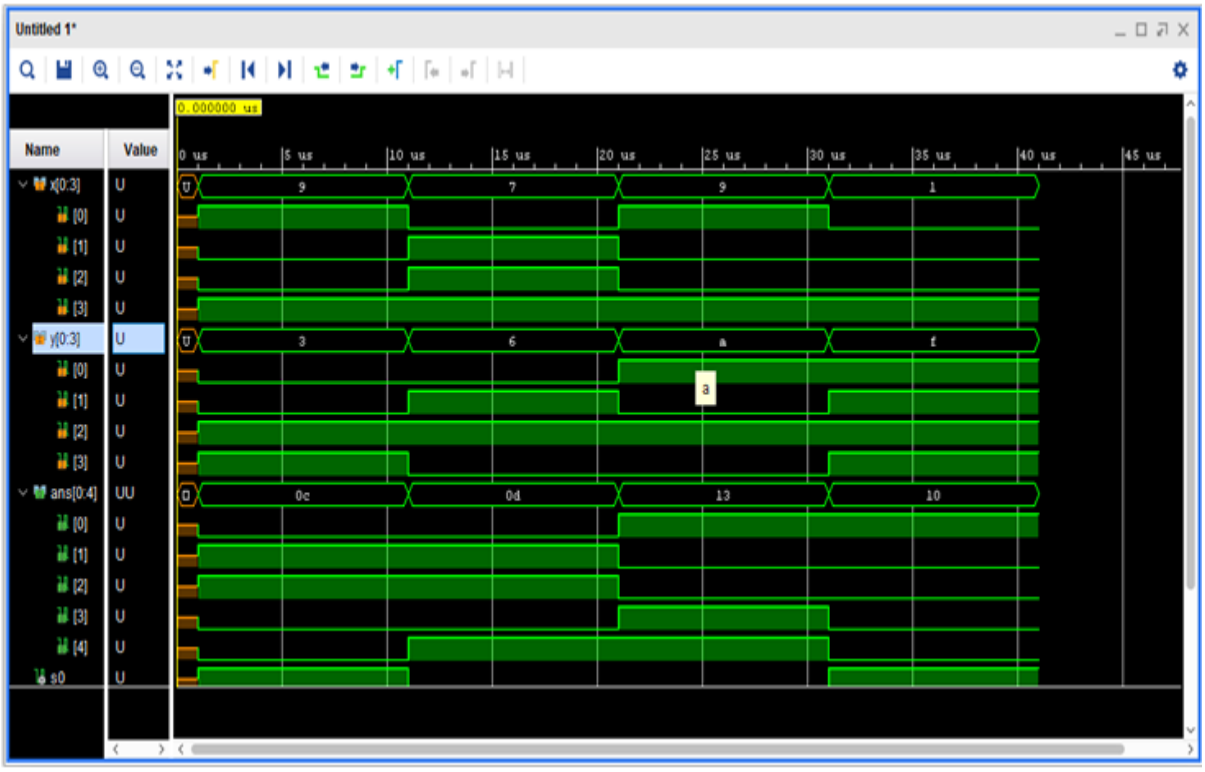

Figure 1.3 Simulation of the 4-bit adder

1.4.2 4-bit adder/Subtractor using Structural Modelling

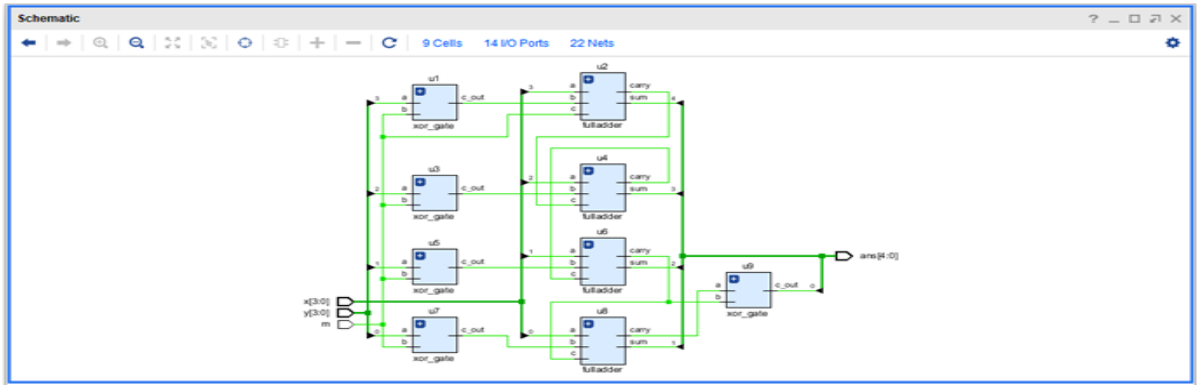

Figure 1.4 Schematic of the 4-bit adder/Subtractor

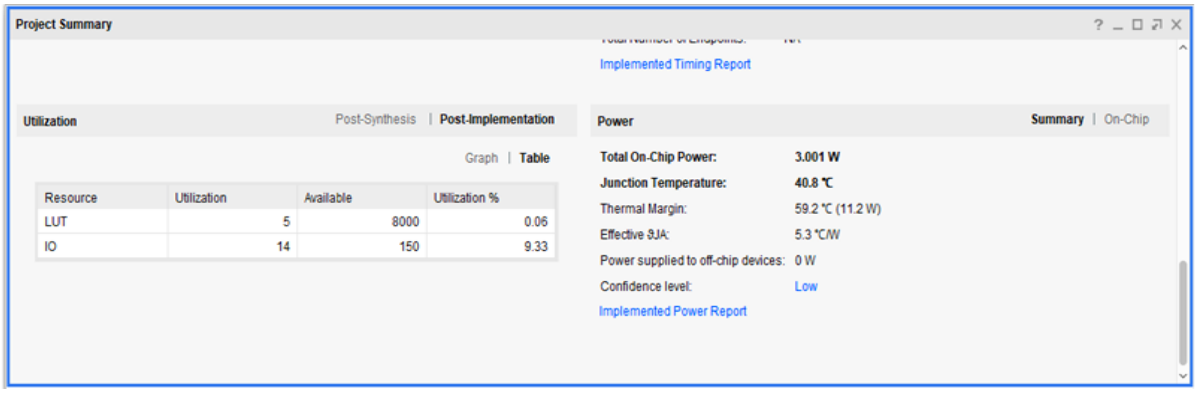

Figure 1.5 Project Summary of the 4-bit adder/Subtractor

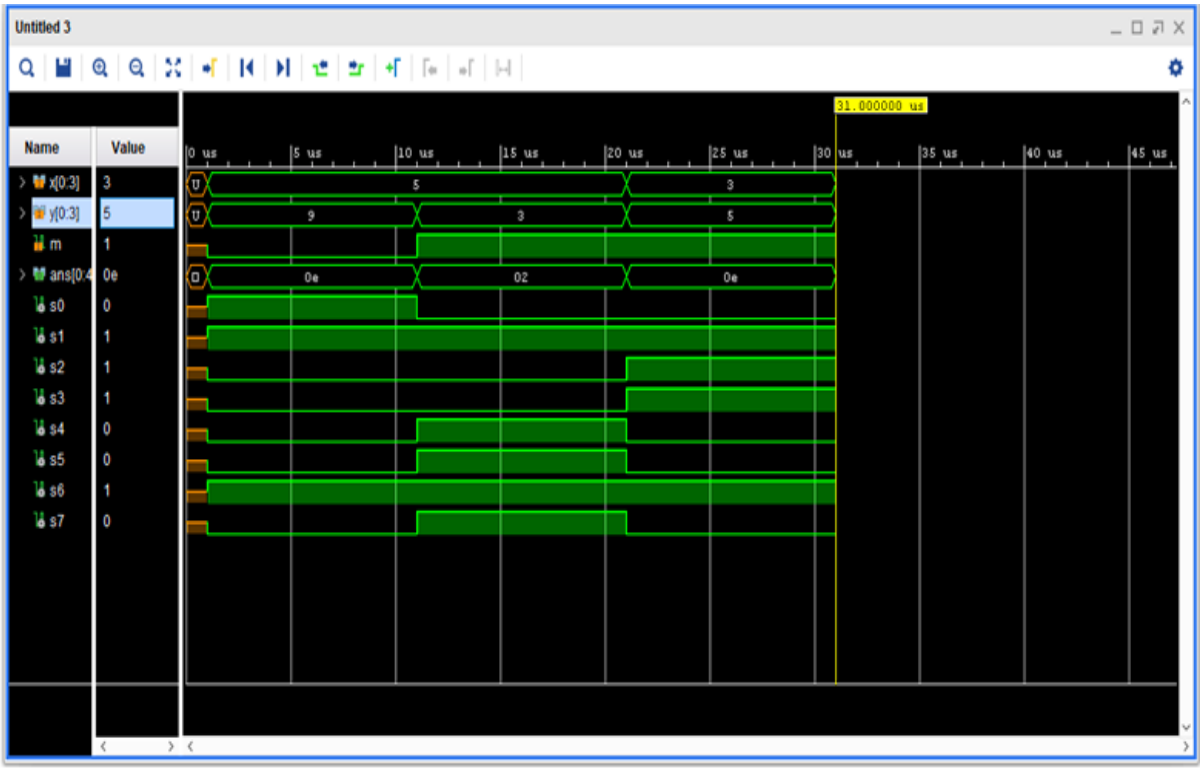

Figure 1.6 Simulation of the 4-bit adder/Subtractor

1.5 Summary

Name of the Entity	No. of LUT used	Total On chip Power
4-bit Adder	4	2.688W
4-bit Adder/Subtractor	5	3.001W

Table 1.1 Comparison of Area and Power requirements for different kinds of adders.