

Antenna & Radio Interface

The schematic diagram illustrates the Antenna & Radio Interface for the EFR32MG24-QFN40-Standard (U1B). The chip is divided into four main functional blocks: RF Crystal, RF I/O, RF Analog Power, and PA Power.

Power Connections:

- VDCDC (RFVDD):** Connected to pin 12. The signal path includes an inductor L3 (BLM03AG700SN1D) and capacitors C4 (2U2) and C5 (18P) to ground.
- PAVDD (PA Power):** Connected to pin 15. The signal path includes an inductor L4 (BLM03AG700SN1D) and capacitors C6 (1U), C7 (18P), and C8 (0P5) to ground.

Crystal Connection:

- High Frequency Crystal (X1):** A 39.000 MHz crystal connected to pins 9 (HFXTAL_I) and 10 (HFXTAL_O).

RF I/O and Matching Network:

- RF I/O:** Connected to pin 14 (2G4RF1).
- 2.4 GHz matching network:** Consists of inductors L1 (1N2) and L2 (2N9), and capacitors C1 (2P3), C2 (1P6), and C3 (0P3) to ground.
- 50R IFA:** A 50 Ohm Impedance Fitting Attenuator connected to the matching network.
- Connector (J1):** An SMA-J-P-H-ST-EM1 connector connected to the 50R IFA.

Ground Connections:

- RFVSS (pin 13) is connected to ground.
- Multiple ground connections are shown for the capacitors and the matching network components.

PAVDD Configuration

	Power Config 1 VMCU to PAVDD	Power Config 2 DCDC to PAVDD
R1	Mount	Not mount
R2	Not mount	Mount

The diagram illustrates a circuit configuration for PAVDD. It shows two input sources, VMCU and VDCDC, each with a red triangle symbol. VMCU is connected to a resistor labeled R1 (0R). VDCDC is connected to a resistor labeled R2 (0R). Both resistors are connected to a common node, which is then connected to PAVDD, indicated by a red triangle symbol. The resistors are represented by blue rectangles with red lines indicating the connection points.

Power & Decoupling

The schematic diagram illustrates the power and decoupling circuit for the EFR32MG24-QFN40-Standard. The chip is divided into several functional blocks, each with its own supply and ground pins:

- DC/DC Regulator:** VREGSW (31), VREGVSS (33), VSS_PAD (41).
- Digital Regulator:** VREGVDD (32), DVDD (34).
- Analog Supply:** AVDD (35).
- I/O Supply:** IOVDD_0 (36).
- Ground:** VREGVSS (33), VSS_PAD (41).

The external components and their connections are as follows:

- VMCU Supply:** Derived from the digital supply (VREGVDD) and the VDCDC supply. It is decoupled by capacitors C11 (10U), C12 (100N), C14 (1U), C15 (10N), C19 (1U), and C16 (100N).
- VDCDC Supply:** Derived from the DC/DC regulator output (VREGSW) and the VDCDC supply. It is decoupled by capacitors C10 (4U7), C13 (100N), C17 (100N), and C18 (1U).
- RESET:** Connected to the RESET pin (11) through a 100N capacitor (C9).
- Grounding:** All ground connections are made to a common GND plane.

I/O Port Pins

		U1A
		EFR32MG24-QFN40-Standard
PA0	21	PA00
PA1/CLK	22	PA01
PA2/DIO	23	PA02
PA3	24	PA03
PA4	25	PA04
PA5	26	PA05
PA6	27	PA06
PA7	28	PA07
PA8	29	PA08
PB0	20	PB00
PB1	19	PB01
PB2	18	PB02
PB3	17	PB03
PB4	16	PB04
PC0	1	PC00
PC1	2	PC01
PC2	3	PC02
PC3	4	PC03
PC4	5	PC04
PC5	6	PC05
PC6	7	PC06
PC7	8	PC07
PD0	40	PD00
PD1	39	PD01
PD2	38	PD02
PD3	37	PD03

EXP Header

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The diagram illustrates the EXP Header connections for three connectors: J2, J3, and J4.

J2 (20-pin connector):

- Pins 1-10: PA0, PA1/CLK, PA2/DIO, PA3, PA4, PA5, PA6, PA7, PA8, PB0, PB1, PB2, PB3, PB4.
- Pins 11-12: GND.
- Pins 13-14: GND.
- Pins 15-16: GND.
- Pins 17-18: VMCU.
- Pins 19-20: VMCU.

J3 (20-pin connector):

- Pins 1-10: PC0, PC1, PC2, PC3, PC4, PC5, PC6, PC7, PD0, PD1, PD2, PD3.
- Pins 11-12: GND.
- Pins 13-14: RESET.
- Pins 15-16: GND.
- Pins 17-18: VMCU.
- Pins 19-20: VMCU.

J4 (4-pin connector):

- Pins 1-4: PA2/DIO, PA1/CLK, GND.

Designed		Approved	
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		Board Name	
		EFR32MG24-QFN40-Standard	
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		Sheet 1 of 1	