

Improving Performance in Structured GPGPU Workloads via Specialized Thread Schedules

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Abstract

[TODO] Write thisss

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	[TODO] Make sure equations are consistent:	
	• L Cache line size (elements)	
	• M Cache size (elements)	
	• M_L Cache size (number of cache lines)	
	• F Memory fetches	
	• I_w, I_h input size (number of tasks to produce the output)	
	• S_w, S_h stencil size	

Chapter 1

Introduction

Graphics Processing Units (GPUs) are specialized hardware that can manipulate large amounts of data in a highly parallel manner. The hardware's main purpose is processing graphical data, however modern use of GPUs is in the form of general-purpose computing on the GPU (GPGPU) where we exploit the GPUs many cores to run computations normally run on CPUs in parallel.

This high performance GPU computing has become very accessible via high level frameworks, which provide a limited set of operators, such as stencil, permute, fold, scan, which can manipulate data on a GPU [1]. However, in most cases the compiled assembly has inefficient memory accesses with lower cache hit rates and uncoalesced accesses than manually tweaked code. Threads can be scheduled in such a way to minimize these inefficiencies. In such cases, a smarter scheduler can achieve better cache and memory utilization [2]. We propose a simple schedule to improve performance by leveraging the structure of memory accesses in the high level GPGPU framework Accelerate [1].

1.1 Motivation

1.2 Contributions

This thesis shows that the cache with tiled implementations for stencil and matrix multiplication can be improved by rescheduling via index mapping. While the main focus lies in improving the performance on GPU, the techniques presented can also be applied on a CPU.

The main contributions of this thesis are:

- An analysis for the theoretical cache utilization and efficiency of both linear and multithreaded (GPU) execution for naive and tiled implementations of stencil and matrix multiplication operations.
- A simple implementable schedule for stencil and matrix multiplication operations that better utilize the cache, which results in equal or better performance than the naive and tiled implementation.
- An analysis for the theoretical cache utilization and efficiency of a column-based scheduler.

1.3 Outline

[TODO] Chapter x introduces yada, yada

Chapter 2

Background

2.1 GPU Architecture

Since the GPU backend of Accelerate only works with CUDA capable devices (see section 2.3), we will mostly focus on the architecture of newer NVidia GPUs. Massive parallel workloads are executed on numerous cores clustered in streaming multiprocessors (SMs). The memory is structured in a multi-level hierarchy containing an L1 cache for each SM, a shared L2 cache for all SMs and multiple banks of DRAM [3, 4].

When working with CUDA the programmer defines a kernel. This is normally done with CUDA C++, an extension on C++ programming language, but in our case Accelerate will handle the generation of kernels (section 2.3) [5].

2.1.1 Hardware

On modern Nvidia GPU architectures the compute units are grouped in graphics processing clusters (GPC). Since GPUs are primarily used in graphics applications, the GPC contains some specialized components: a raster engine, Texture Processing Clusters (TPCs), **[TODO] ...**. The main point of interest are streaming multiprocessors (SMs) in the TPCs. Each SMs has its own instruction scheduler and various execution pipelines. Jia et al. suggests that a threadblock should contain at least 128 threads due to SMs on Turing, Volta, and Ampere being split into four processing blocks [3, 4, 6, 7].

[TODO] More specific + figure

2.1.2 Software

Executions on a GPU are directed on both the host and device (GPU). *Kernels* define the functions that should be executed on the GPU. The host side controls how these kernels should be executed, namely how the threads should be launched and executed. Threads are grouped and defined on a 2 level hierarchy: threads are grouped together in *cooperative thread arrays* (CTAs), also known as thread blocks, and multiple CTAs can be queued for the execution of a single kernel. Both can be controlled upon executing a kernel: the amount of threads per CTA (threadblock size) and the total amount of CTAs (gridsize). CTAs get assigned to SMs in a round-robin fashion.

When an SM executes a CTA, it splits the work into warps, a grouping of 32-threads. On architecture before Volta, a single warp is executed in a single instruction, multiple threads fashion, where a single program counter is shared amongst the 32 threads. With the volta architecture, independent thread scheduling allows full concurrency between threads and the scheduler can group multiple threads into SIMT units.

[TODO] SM can context switch between multipel warps to hide latency

[TODO] Figure visualizing the whole thing because text is confusing... probably

2.1.3 GPU Caches

To the programmer, the memory hierarchy is very simplified: there is the compute unit and the memory. Caches are hidden from this model as on most architectures they are managed by hardware.

Memory can become a significant bottleneck due to the large amount of threads running concurrently. Caches can alleviate this but are limited in size, and given a large enough problem can cause cache

trashing – the premature eviction of data before any significant reuse [8]. To improve efficiency of caches, caches assume spatial locality via cache lines. A cache line is the smallest unit of data that a cache can hold. For example, an L1 cache on a Turing GPU uses cache lines that hold 128 bytes of data. Therefore, fetching data from memory also brings extra nearby data with it.

Data shared between threads through the cache can happen in a read-after-write (RAW) or read-after-read (RAR) manner. RAW has data dependency among tasks, for example in scan operations. RAR has no data dependency and can be executed in any order [9].

The L1 cache in older Nvidia GPU architectures (Maxwell, Pascal) uses the least recently used (LRU) eviction policy. When caches become full, we need to remove data (a cache line) from the cache to allow newer data to be cached. An LRU eviction policy evicts data that is the least recently used. Jia et al. [6] have shown that in Turing and Volta GPUs, the P-chase benchmark that is used to detect the LRU eviction policy presented by Mei and Chu [10] fails to complete over the full L1 cache. Jia et al. conclude that newer architectures (Turing, Volta) use a non-LRU eviction policy [6, 10, 11]. When the L1 cache in Turing and Volta GPU saturates, 4 consecutive cache lines are chosen randomly to be evicted. This is in line with a new eviction policy mechanism introduced with Volta, where cache lines can be assigned a priority [5, 6].

Modern Nvidia GPUs are able to handle various types cache operations and eviction hints. By default, loads are cached at all levels (L2, L1) with an LRU policy. This brings a problem with it: if data is written to a cached value, we need to evict this cache line from all other L1 caches first, since that value is no longer up to date after our update. As an example, it is also possible to only cache on L2, bypassing L1. Another option is to hint cache streaming, where the loaded cache line will have an evict-first policy to prevent pollution of the cache. Similar operations exist for writing data to memory. In both cases it is up to the compiler and programmer to exploit this for extra performance [5].

2.1.4 Performance of Access Patterns

Lam et al. and Meyer et al. describe two types of reference reuse [12, 13]:

- **Spatial reuse** occurs when accessing data from the same cache line, increasing spatial locality.
- **Temporal reuse** occurs when the same data is accessed at a later time, increasing temporal locality.

The reuse factor can be kept track of by counting the two types of reuse. Loading data horizontally (sequentially) exploits spatial locality and is therefore cheaper than loading data vertically. Additionally, temporal reuse can only happen when other memory accesses do not displace reusable data from the cache.

Lam et al. proposed a method to model cache interference. In the simplest case where all data used is cached in different locations (and therefore no data is evicted), the number of misses per variable v is described by $D(v)/R(v)$, where $D(v)$ is the total number of references (loads) of v and $R(v)$ is the reuse factor. However, with interference misses when data gets displaced from cache, the total number of misses for v is

$$D(v) \left(\frac{1}{R(v)} + \frac{R(v) - 1}{R(v)} M(v) \right)$$

With missrate being

$$M(v) = 1 - (1 - S(v)) \prod_{u \in V - \{v\}} (1 - F(u))$$

$F(u)$ is defined as the fraction of cache used by variable u , and self interference $S(v)$ is defined to be the fraction of accesses that map to non-unique location in the cache.

[TODO] Illustrations for interference

2.2 CPU vs GPU based multi-threading

[TODO] Aka, the limits of GPUs, segway to introduce Accelerate

2.3 Accelerate

[TODO] Generalize to Array DSLs Accelerate is an embedded purely functional array language in Haskell [1]. Accelerate has a frontend containing the embedded language, and the backend which handles

code generation and execution. The frontend handles general optimizations such as sharing recovery and array fusion [14, 15]. Further hardware specific optimization is handled on the various backends. There are two LLVM [16] backends provided: one that targets multicore CPUs `accelerate-llvm-native` and one that targets Nvidia GPUs `accelerate-llvm-ptx`. In both backends we compile Accelerate code to LLVM IR. When we want to run Accelerate on a GPU, LLVM will handle the compilation from LLVM IR to PTX, the instructions set for Nvidia’s CUDA programming environment [5, 16, 17]. The GPU backend implements a series of skeletons which implement primitive operations such as stencils, generate, permute, and scan. These skeletons define how a program should be compiled and is the part where a custom thread scheduler can be implemented. Further customizations to the scheduler can be done on the executing side of the backend as it controls how kernels are launched.

2.4 Commonly Applicable Cache Improvements

2.4.1 Optimizations of Blocked Algorithms

Lam et al. expands on the well known idea of working on blocks instead of entire rows or columns.

If all data fits onto cache without eviction, the misses that occur are *intrinsic misses*. In the real world however, data can be evicted by other memory accesses. This interference of reuse is categorized between two cases: *cross interference* and *self interference*. Cross interference assumes the location of data in memory is unrelated to the location in cache, and instead is measured by probability that the reuse falls within the footprint of the variable. Self interference extends this by taking the cache locations of variables into account, which can happen when the data for a single iteration no longer fits in cache. [12]

2.4.2 CTA Clustering

[TODO] Write

2.4.3 PAVER

[TODO] wRITE

Chapter 3

Analysis of Existing Approaches

3.1 Spatial Temporal Analysis

The memory accesses of algorithms can be plotted in a spatial-temporal diagram, with the address space on the spatial axis and order of access on the temporal axis. Since only the thread order can be manipulated, elements on the temporal can be condensed by grouping them by thread. Additionally, a cache simulation can annotate this diagram with the cache level (L1, L2, RAM) of each memory address.

[TODO] Example diagrams, cache simulation

3.2 Stencil Operations

Stencil operation produces an N-dimensional array from a same sized input. For each element it reads a fixed sized neighborhood and writes a single element. Stencils are used for image operations (edge detection, filters, noise reduction), but can also find their use in other fields such as solving partial differentiation[18] and cellular automata.

3.2.1 Naive

The naive implementation iterates over each of the outputs linearly, horizontally first. The temporal linearity translates to parallelism on GPUs where multiple threads work concurrently on each element of the output array.

While the naive implementation of stencil operations works well enough when enough rows of the input fit in the cache, it begins to fall in performance on larger inputs.

[TODO] Split figure 3.1 up into their respective parts

The minimum amount of cachelines cached M_l , and therefore needed, of cache line size of L elements to stay in the ideal case is correlated by the stencil size and width of the input array:

[TODO] Maths

$$M_l \geq \left\lceil \frac{I_w + S_w}{L} \right\rceil S_h \quad (3.1)$$

While in most cases **[TODO] examples** this enough to fully exploit L2 caches, this can be unoptimal in regard to the L1 cache. **[TODO] Example** The amount of cache lines needed to be fetched from memory F is bound by the worse case (eq. 3.1 is not satisfied) where we consistently evict data from cache before we can reuse:

$$F \leq \left\lceil \frac{I_w + S_w}{L} \right\rceil I_h S_h$$

If equation 3.1 is satisfied, the amount of fetches F is no longer dependent on the stencil height S_h

$$F = \left\lceil \frac{I_w + S_w}{L} \right\rceil I_h$$

[TODO] GPU threading is different from CPU stuff yada yada With multiple threads active, even more data is required to be kept in cache for optimal usage. In the best case, all threads are cohered

with overlapping accesses, and in the worst case, threads will be spread out more with less overlapping accesses. Threads in GPUs are grouped by warps, threads contained within are always cohered, and therefore a guarantee for overlapping accesses. Therefore, only when multiple warps are executed on the same SM, divergence in accesses can occur. A single warp of 32 threads uses $\lceil \frac{32+S_w}{l} \rceil S_h$ cache lines when the threads cover a single rows. When the warp is split between 2 rows, the cache needs to be slightly bigger: $\lceil \frac{32+2S_w}{l} \rceil S_h$.

Ideally, the whole input array would fit on the cache, but a sufficiently large input (i.e. a 2048×2048 32-bit floating point array uses 16 MiB) will not fit on the L2 caches of modern GPUs (≈ 6 MiB of L2 data cache, Volta V100) and cache misses are unavoidable. Even if data would fit on the L2 cache, there would still be potential cache misses at the L1 cache (128 KiB, Volta V100).

[TODO] More figures like in fig. 3.2, but for GPU/multithreading

Using the model described in section 2.1.3 can be used to estimate the cache misses of the naive implementation and the model parameters are summarized in table 3.1. Calculating the reuse for an iteration of s_y , i_x , and i_y is fairly trivial.

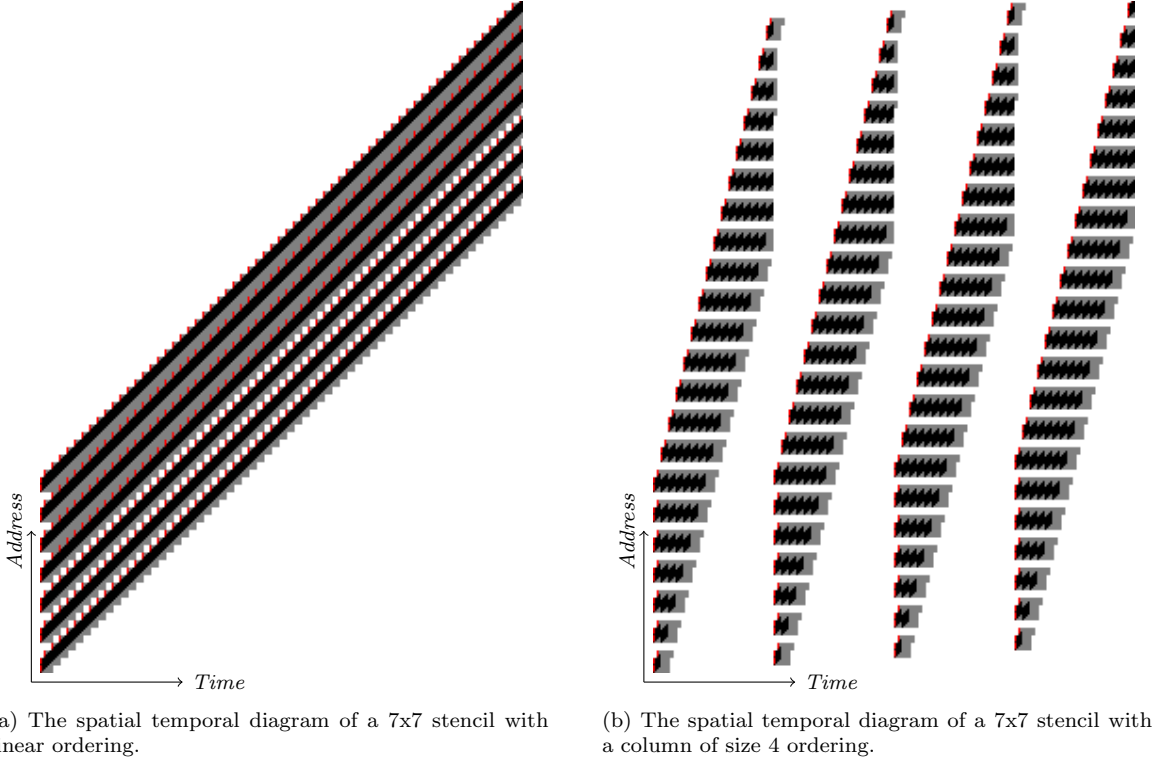


Figure 3.1: The spatial temporal diagrams of a 7x7 stencil. The vertical axis describes the location in a 2D array which is mapped to 1D address space. The horizontal axis describes time. ■ are addresses of cache lines that are brought into cache. ■ are addresses being accessed. ■ are addresses in cache.

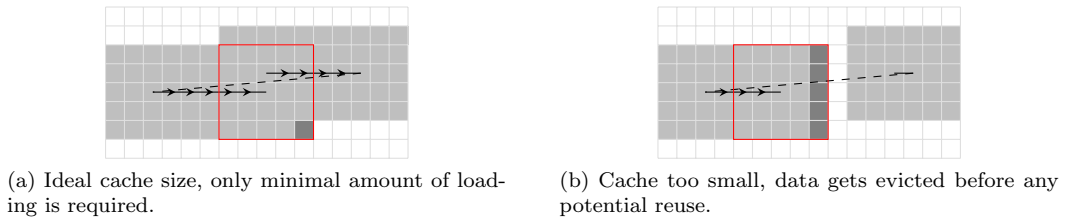


Figure 3.2: **[TODO] write this**

[TODO] These are the calculations adapted from Lam et al. 1991. I'm not really sure if I should do this. They feel not very elegant, and more like a black box system... s_x is omitted due to it only loading a singular value during one loop and has therefore no reuse. During a single step of s_y an entire row of all S_w elements from the stencil has been loaded. A single step on i_x processes the output of a singular element, which means an entire stencil is read.

Array	Reuse				Self-Interference			
	i_x	i_y	s_x	s_y	i_x	i_y	s_x	s_y
X	$(S_w - 1)S_h$	$(S_h - 1)S_w I_w$	-	S_w			0	0
Array	Footprint				References			
	i_x	i_y	s_x	s_y				
X	$S_w S_h / C$	$I_w S_h / C$	$1/C$	S_w / C	$I_w I_h S_w S_h$			

Table 3.1: The reuse, self-interference, and footprint of the naive implementation of stencils during a single step of iterating on i_x , i_y , s_x , and s_y . [TODO] Calculate self interference

3.2.2 Tiling

A common used optimization is by dividing the work into works as described in 2.4.1. [TODO] blablabla

The minimum required cache for optimal tiling is dependent on [TODO] ... tiling size t

$$M_l \geq \left\lceil \frac{t + S_w}{L} \right\rceil S_h \quad (3.2)$$

The largest possible tiling size t is derived by inverting equation 3.2

$$t \leq \frac{LM_l}{S_h} - S_w \quad (3.3)$$

Since equation 3.2 can always be satisfied by adjusting t , we can have a lower upper bound on the amount of cache line fetches F :

$$F \leq \left\lceil \frac{I_w}{t} \right\rceil \left\lceil \frac{t + S_w}{L} \right\rceil \left\lceil \frac{I_h}{t} \right\rceil (t + S_h) \quad (3.4)$$

[TODO] Maybe remove this. Probably just keep it, so we can plot our expected number of cache line fetches We can define the number cache lines fetched in terms of the available cache by substituting equation 3.2 into equation 3.4:

$$F \leq \left\lceil \frac{I_w}{\frac{LM_l}{S_h} - S_w} \right\rceil \left\lceil \frac{\frac{LM_l}{S_h} - S_w + S_w}{L} \right\rceil \left\lceil \frac{I_h}{\frac{LM_l}{S_h} - S_w} \right\rceil \left(\frac{LM_l}{S_h} - S_w + S_h \right) \quad (3.5)$$

$$F \leq \frac{I_w I_h M_l}{(\frac{LM_l}{S_h} - S_w)^2 S_h} \left(\frac{LM_l}{S_h} - S_w + S_h \right) \quad (3.6)$$

[TODO] simplify this further by relaxation perhaps?

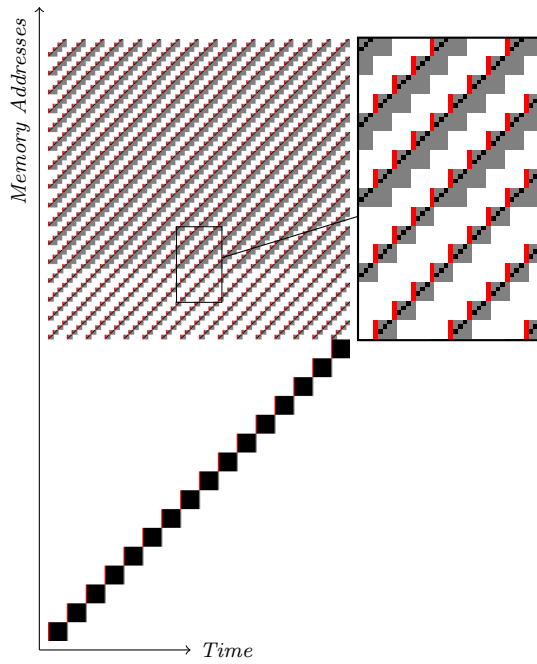
[TODO] GPU/multithreading notes

3.3 Matrix Multiplication

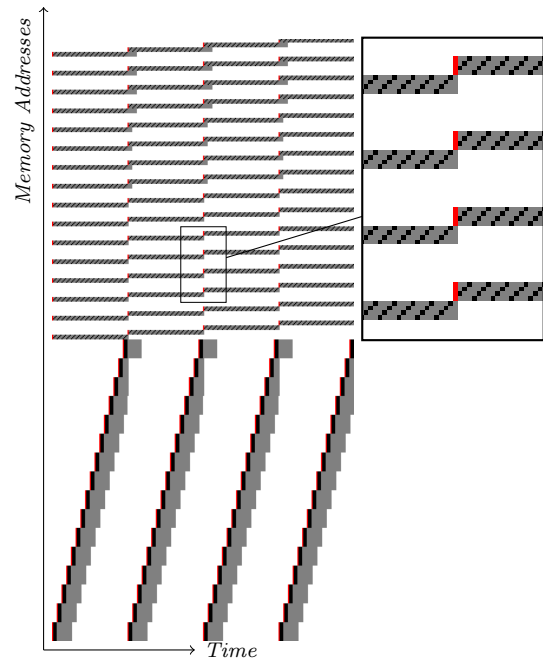
3.3.1 Naive

[TODO] Split figure 3.3 up into their parts for better flow

3.3.2 Tiling



(a) The spatial temporal diagram of matrix multiplication with linear ordering.



(b) The spatial temporal diagram of a matrix multiplication with a column of size 4 ordering.

Figure 3.3: The spatial temporal diagrams of a matrix multiplication. The vertical axis describes the location in a 2D array which is mapped to 1D address space. The horizontal axis describes time. ■ are addresses of cache lines that are brought into cache. ■ are addresses being accessed. ■ are addresses in cache.

Chapter 4

Column Based Iteration

[TODO] Consider splitting in two chapters if they get too big

While tiling itself is a well-known optimization technique, we most consider the parts of why it works.

[TODO] ...

In a sense, grouping columns is similar to striding clusters of data, except in the case when a row of work can't be perfectly strided. When the width of a multidimensional array is not a multiple of the stride, the loads will not align column wise (**[TODO] figure**). To work around this, in the column approach we allow the last column to be narrower.



Figure 4.1: **[TODO] write this**

[TODO] implementation details

We can construct the index mapping $i \mapsto j$. First, we calculate the offset for the starting index of the column we need to map to

$$o = \left\lfloor \frac{i}{I_h w} \right\rfloor w \quad (4.1)$$

Then, modify the width value such that the last column does not exceed the input width

$$w' = \begin{cases} ((I_w - 1) \bmod w) + 1 & \text{if last column} \\ w & \text{otherwise} \end{cases} \quad (4.2)$$

And take i' as the index within a column.

$$i' = i \bmod I_h w' \quad (4.3)$$

So that we can calculate j

$$j = (i' \bmod w')' + \left\lfloor \frac{i'}{w'} \right\rfloor I_w + o \quad (4.4)$$

[TODO] should i add a figure showing the relation between the equation and the column pattern?

[TODO] What are the effects of GPU warps (32 threads) with this schedule?

4.1 Zigzagging variation

[TODO] If we make columns fit for L2 cache, zigzagging may improve locality for lower level cache (L1) when columns sizes aren't a nice power of 2 (or)

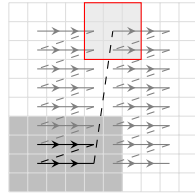
4.2 Implementation in Accelerate

[TODO] AAAAAAAAAAAAAA

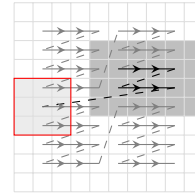
4.3 Stencil Operation

The naive stencil operations had problems of chasing the cache on sufficiently large input sizes which tiling does resolve (section 3.2.2). Consider what the tiling implies: we split the work on all axis, to improve locality. However, all tiling except horizontal is unnecessary [TODO] **bold claim, needs support** and may cause even more discontinuity in favourable access pattern.

Let us first consider the single threaded case of column based iteration: by controlling the column width we can force the ideal scenario of the naive stencil implementation (figure 3.2a) to occur, similarly to tiling. The column based approach is similar to tiling, but also allows the ideal memory access pattern to continue accross tiles vertically. In GPUs this translates to less cohesive threads as threadblocks get assigned in a round-robin fashion to SMs, eliminating possibilities of L1 cache reuse.



(a) Grouping by column only incurs a heavy load every time a new column is started.



(b) Grouping by column and row (tiling) also incurs a heavy load when starting a new row, and due to having more rows also has more column starts.

Figure 4.2: Visualisation of cache bottlenecks for both column based and tiling approaches. ■ Memory required by the next task. ■ Tasks that still have their memory in cache. ■ Memory in cache. ■ Previous and upcoming tasks.

[TODO] WRITEAAAAAAAAAAAAA

The size of the cache needed M_{size} can be approximated given the unit byte size u , column width c , stencil width s_w and height s_h , and the number of active threads t . The required memory is independent of the size of the input data.

$$M_{size} = u(c + s_w) \left(s_h + \left\lceil \frac{t}{c} \right\rceil \right)$$

Solving for c gives an unneedly complex solution, so instead we approximate M_{size} using the asymptote.

$$M_{size} = u(t + s_h(c + s_w))$$

Solving for column width c gives

$$c = \frac{M_{size} - u(s_h s_w + t)}{s_h u}$$

[TODO] amount cache line fetches text here The amount of fetches is similar to equation 3.4, however, since we do not divide the work horizontally anymore, the amount of cache line fetches is slightly less:

$$F \leq \left\lceil \frac{I_w}{c} \right\rceil \left\lceil \frac{c + S_w}{L} \right\rceil (I_h + S_h) \quad (4.5)$$

[TODO] Is a difference useful?

$$\Delta F \approx \quad (4.6)$$

[TODO] Calculate column parameters, spatial temporal diagrams

4.4 Matrix Multiplication

A matrix multiplication of $A \cdot B = C$ consist out of three parts: reading horizontally from matrix A , reading vertically from matrix B , and writing to matrix C . Since writing the output does not block any further instructions, it can be ignored. Reading horizontally is significantly cheaper due to cache locality.

$$M_{size} = u \left(hc + w \left\lceil \frac{t}{c} \right\rceil \right)$$

Similarly to stencil operations, approximate M_{size} using the asymptote

$$M_{size} = uhc$$

Then solving for c

$$c = \frac{M_{size}}{uh}$$

[TODO] Calculate column parameters, spatial temporal diagrams

Chapter 5

Results

[TODO] Benchmark results, Nvidia profiler statistics

5.1 Execution Times

5.2 Cache Hitrate

5.3 Hardware Utilization

Chapter 6

Conclusion

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