Automatic RFIC Synthesis for Passive Downconversion Mixers

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Aim

- In this project, I have automated the schematic design of Passive Downconversion Voltage mode and Current mode Mixers.
- The automation uses the popular **Gradient Descent** algorithm.

Why ML in circuit design?

- The complexity and density of integrated circuits continue to grow exponentially in the VLSI industry. Today a processor chip can have over a **billion** transistors..
- AI and ML offer innovative solutions to optimize various processes and improve efficiency.

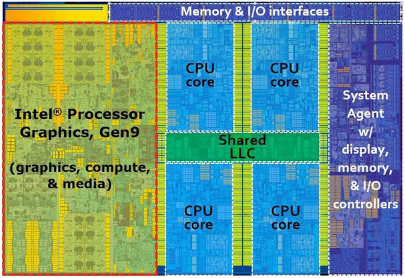


Figure 1: microprocessor chip with over 10^9 transistors

Introduction (cont.)

Active ML applications today

- **Performance Optimization** ML-driven optimization techniques enhance circuit performance by fine-tuning design parameters.
- **Design Automation** ML algorithms assist in automating layout generation and optimizing power, performance, and area.
- **Fault Detection and Testing** ML algorithms increase the accuracy of fault detection checks in designs where manual checking is near impossible.

Downconversion Mixers

- In a direct conversion RF receiver, a mixer translates the received signal from RF to baseband.
- Passive mixers are a class of mixers in which the transistors do not operate as amplifying devices. Instead, they function as switches.

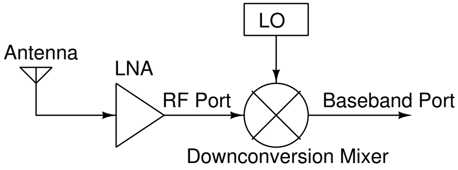


Figure 2: Downconversion mixer in receiver path

Introduction (cont.)

Passive mixers are a suitable option for applications requiring low noise figures and good impedance matching over a wide range of frequencies, such as,

- Wireless communication - cellular base station transceivers
- AM/FM and two-way radio systems
- RADARs used in defence

Types of Passive Mixers

1) Based on whether the input is an RF voltage or RF current:

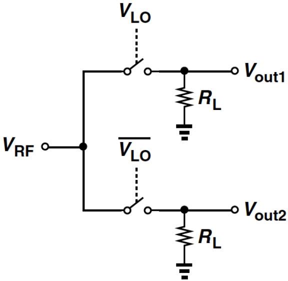


Figure 3: Voltage mode passive mixer

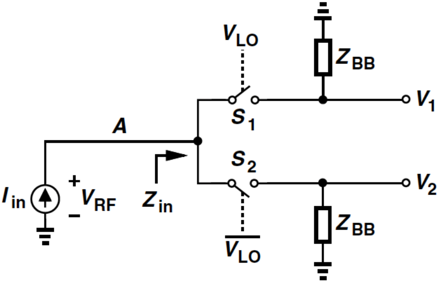


Figure 4: Current mode passive mixer

Introduction (cont.)

2) Based on whether the load used is a resistor or capacitor:

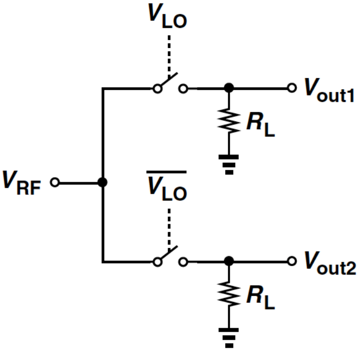


Figure 5: Return-to-zero mixer

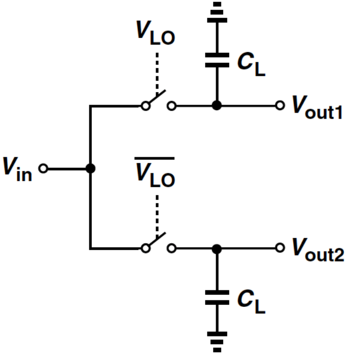


Figure 6: Non-return-to-zero/sampling mixer

3) Based on whether the input is single-ended or differential:

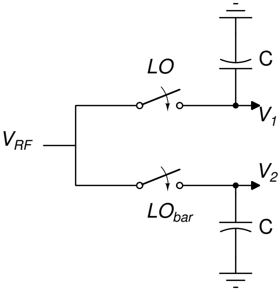


Figure 7: Single-balanced mixer

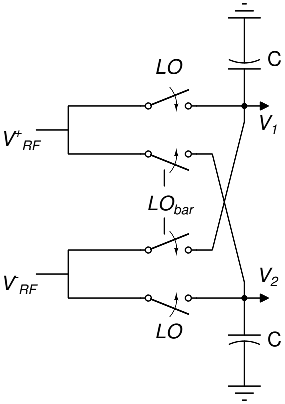


Figure 8: Double-balanced mixer

Optimisation Algorithm - Gradient Descent

Principle

The **loss function** is minimised by iteratively adjusting the model parameters in the opposite direction of the *gradient* of the loss function with respect to those parameters.

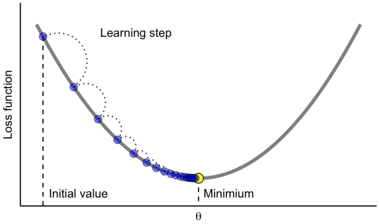


Figure 9: 1-D gradient descent

Key parameters in gradient descent: Loss function, loss weights, gradient of the loss function, learning rate (α), model parameter updation.

Gradient Descent - Optimising Schematic design

The specifications of the passive mixer that are of importance are input impedance matching S_{11}, conversion gain, integrated single sideband (SSB) noise figure, IIP_3 and power consumption.
The automation routine implements gradient descent on the mixer netlist

- starting with hand-calculated circuit parameters
- The loss function and its gradient with respect to the circuit parameters used in optimisation are evaluated in every iteration.
- Every iteration, the circuit parameters are updated using the gradient.

Gradient Descent - Loss Function

Mixer specifications used to define the Loss-input impedance matching S_{11}, conversion gain, integrated single sideband (SSB) noise figure, IIP_3 and power consumption.
The Rectified Linear Unit function $ReLU(x)$ is used to define loss.

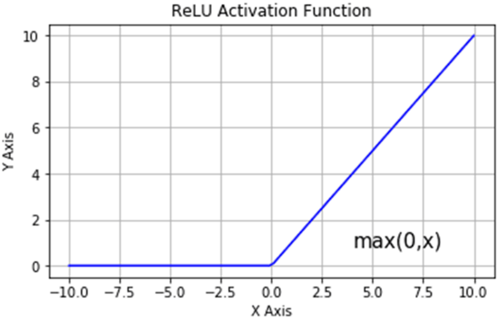


Figure 10: Rectified Linear Unit

Gradient Descent - Loss Function (cont.)

$$\text{Loss } S_{11} = ReLU(\text{ Simulation } S_{11} - \text{ Reference } S_{11} \text{ }) \tag{1}$$

$$\text{Loss gain } = ReLU(\text{ Reference gain } - \text{ Simulation gain }) \tag{2}$$

$$\text{Loss } NF = ReLU(\text{ Simulation } NF - \text{ Reference } NF \text{ }) \tag{3}$$

$$\text{Loss } IIP_3 = ReLU(\text{ Reference } IIP_3 - \text{ Simulation } IIP_3 \text{ }) \tag{4}$$

$$\text{Loss Idd } = \text{Idd} \tag{5}$$

Total Loss function:

$$\begin{aligned}\text{Loss} = A_1 \cdot \text{Loss } S_{11} \ + \ A_2 \cdot \text{Loss gain } + \ A_3 \cdot \text{Loss } NF \ + \\ A_4 \cdot \text{Loss } IIP_3 \ + \ A_5 \cdot \text{Loss Idd}\end{aligned} \tag{6}$$

Gradient Descent - Updating Circuit Parameters

In the k^{th} iteration, $x_j(k)$ indicates the j^{th} circuit parameter

$$\frac{\partial Loss}{\partial x_j} \approx \frac{\Delta Loss}{\Delta x_j} \tag{7}$$

$$x_j(k+1) = x_j(k) - \alpha_j \frac{\partial Loss}{\partial x_j} x_j^2(k) \tag{8}$$

Equation (7) - computation of gradient with respect to x_j
Equation (8) - Updating x_j

Circuit diagram

The schematic chosen for optimisation is the double-balanced, fully differential voltage mode downconversion mixer.

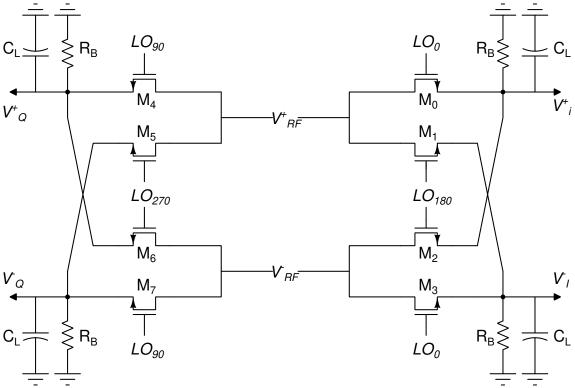


Figure 11: Double-balanced fully differential Voltage mode mixer

Voltage Mode Passive Mixer

- Quadrature LO signalling with 25% duty cycle (figure 23)
- LO Range of operation - 100 MHz to 1 GHz
- Input impedance looking in from the differential RF inputs matched to 50Ω
- LO input is fed to the gate of the switching nMOSFET through buffers built with inverters (figure 24)

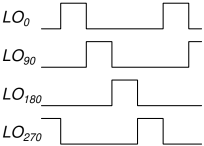


Figure 12: quadrature LO with 25% duty cycle

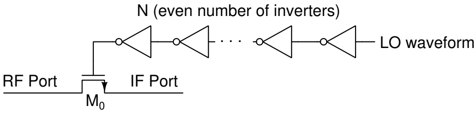


Figure 13: Buffer connecting LO to switching transistor

Voltage Mode Passive Mixer - Small signal

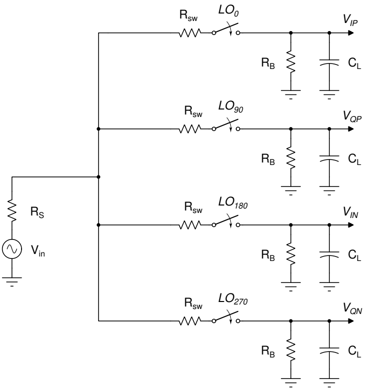


Figure 14: single-balanced mixer, small signal LPTV model

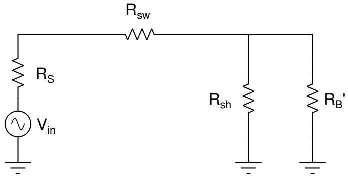


Figure 15: LTI model for input impedance matching

Voltage Mode Passive Mixer - Equations

Equations based on figures 14 and 15 are used to set up the netlist before optimisation

$$R_{sw} \cdot C_L \ll T_{on} \text{ , during the on-time of the switch} \tag{9}$$

$$R_B \cdot C_L \gg T_{off} \text{ , during the off-time of the switch} \tag{10}$$

$$R_{sh} = (R_{sw} + R_s) \cdot \frac{4\gamma}{1 - 4\gamma} \tag{11}$$

$$Z_{in} = R_{sw} + (\gamma R_B) \parallel R_{sh} \tag{12}$$

$$\text{Number of Inverters } = N = \log_{\rho}\left(\frac{2C_{sw}}{C_i}\right) \tag{13}$$

$R_s = 50\Omega$ and $\gamma = \frac{2}{\pi^2} = 0.203$

Voltage Mode Passive Mixer

Updating the circuit parameters in each iteration

$$W_r \leftarrow W_r - \alpha \frac{\partial Loss}{\partial W_r} W_r^2 \tag{14}$$

$$W_c \leftarrow W_c - \alpha \frac{\partial Loss}{\partial W_c} W_c^2 \tag{15}$$

$$W_{sw} \leftarrow W_{sw} - \alpha \frac{\partial Loss}{\partial W_{sw}} W_{sw}^2 \tag{16}$$

$$\rho \leftarrow \rho - \alpha \frac{\partial Loss}{\partial \rho} \rho^2 \tag{17}$$

$W_r =$ width of resistance R_B
$W_c =$ width of capacitance C_L
$W_{sw} =$ width of nMOSFET
$\rho =$ inverter size ratio

Voltage Mode Passive Mixer - Optimisation Results

	Pre-optimisation	Specification	Post-optimisation
S_{11}	-23.98 dB	< -15 dB	-16.05 dB
Gain	2.61 dB	> 4 dB	4.27 dB
SSB NF	6.86 dB	< 7 dB	6.01 dB
IIP_3	24.78 dBm	> 15 dBm	26.42 dBm
Power	3.692 mW	Minimise	3.529 mW

Table 1: Specifications at $f_{LO} = 550$ MHz before and after optimisation

Loss	Starting value	Post-optimisation
S_{11}	0	0
Gain	0.421	0
SSB NF	0	0
IIP_3	0	0
Power	9.23×10^{-4}	8.82×10^{-4}
Total loss	0.422	8.82×10^{-4}

Table 2: Loss values before and after optimisation

Loss vs iterations

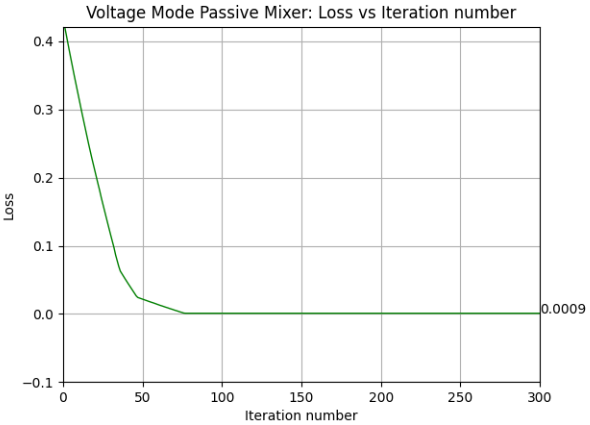


Figure 16: Loss vs iterations for voltage mode mixer

Voltage Mode Passive Mixer - Optimisation Results (cont.)

S_{11} process and temperature variations

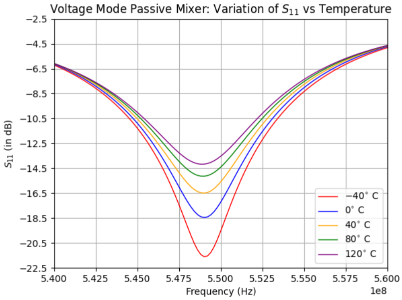


Figure 17: Temperature

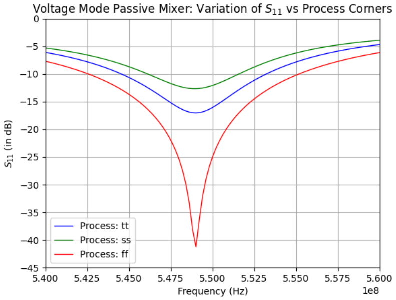


Figure 18: Process variations at 27°C

Gain process and temperature variations

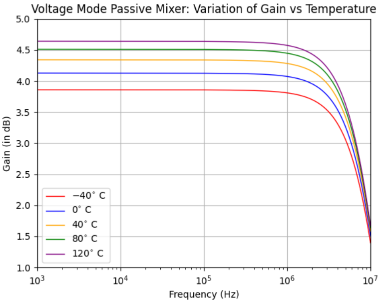


Figure 19: Temperature

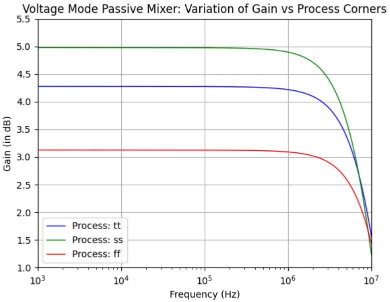
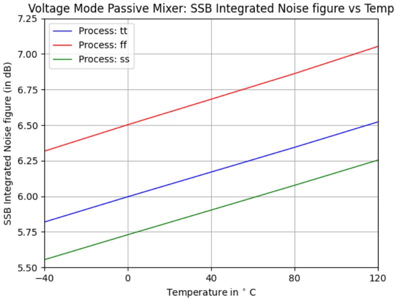
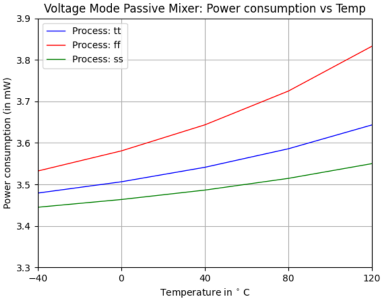


Figure 20: Process variations at 27°C

Voltage Mode Passive Mixer - Optimisation Results (cont.)





Circuit diagram

The schematic chosen for optimisation is the double-balanced, fully differential current mode downconversion mixer.

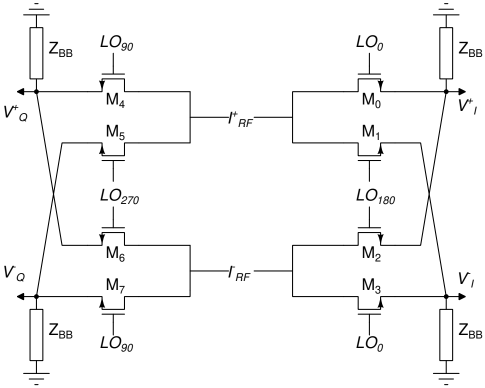


Figure 21: Double-balanced fully differential Current mode mixer

Current Mode Passive Mixer

Z_{BB} is a **trans-impedance amplifier (TIA)**. The trans-impedance amplifier (figure 22) translates the switching current from the RF side to a baseband output voltage. The trans-impedance, $Z_{BB}(j2\pi f)$ (or current to voltage gain) of the amplifier is given by (the OPAMP is assumed to be ideal)

$$Z_{BB}(j2\pi f) = \frac{V_{out}}{I_{in}} = \frac{R_L}{1 + j2\pi f C_L R_L} \quad (18)$$

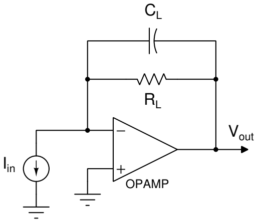


Figure 22: Trans-impedance amplifier

Current Mode Passive Mixer

- Quadrature LO signalling with 25% duty cycle (figure 23)
- LO Range of operation - 100 MHz to 1 GHz
- Input impedance looking in from the differential RF inputs matched to 0Ω
- LO input is fed to the gate of the switching nMOSFET through buffers built with inverters (figure 24)
- The input impedance looking into the mixer from the differential RF port resembles a frequency-translated version of $Z_{BB}(j2\pi f)$

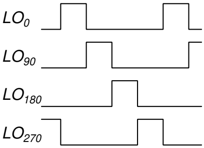


Figure 23: quadrature LO with 25% duty cycle

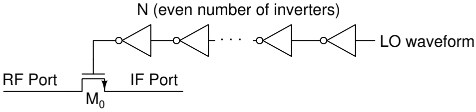


Figure 24: Buffer connecting LO to switching transistor

Current Mode Passive Mixer

Updating the circuit parameters in each iteration

$$W_r \leftarrow W_r - \alpha \frac{\partial Loss}{\partial W_r} W_r^2 \tag{19}$$

$$W_c \leftarrow W_c - \alpha \frac{\partial Loss}{\partial W_c} W_c^2 \tag{20}$$

$$W_{sw} \leftarrow W_{sw} - \alpha \frac{\partial Loss}{\partial W_{sw}} W_{sw}^2 \tag{21}$$

$$\rho \leftarrow \rho - \alpha \frac{\partial Loss}{\partial \rho} \rho^2 \tag{22}$$

$W_r =$ width of resistance R_B
$W_c =$ width of capacitance C_L
$W_{sw} =$ width of nMOSFET
$\rho =$ inverter size ratio

Current Mode Passive Mixer - Optimisation Results

	Pre-optimisation	Specification	Post-optimisation
S_{11}	-5.66 dB	$\|S_{11}\| < 5$ dB	-4.953 dB
Gain	61.847 dB	> 60 dB	60.532 dB
SSB NF	7.28 dB	< 8 dB	7.3 dB
IIP_3	25.63 dBm	> 15 dBm	27.46 dBm
Power	12.431 mW	Minimise	10.09 mW

Table 3: Specifications at $f_{LO} = 550$ MHz before and after optimisation

Loss	Starting value	Post-optimisation
S_{11}	0.098	0
Gain	0	0
SSB NF	0	0
IIP_3	0	0
Power	3.1×10^{-3}	2.523×10^{-3}
Total loss	0.101	2.523×10^{-3}

Table 4: Loss values before and after optimisation

Current Mode Passive Mixer - Optimisation Results (cont.)

Loss vs iterations

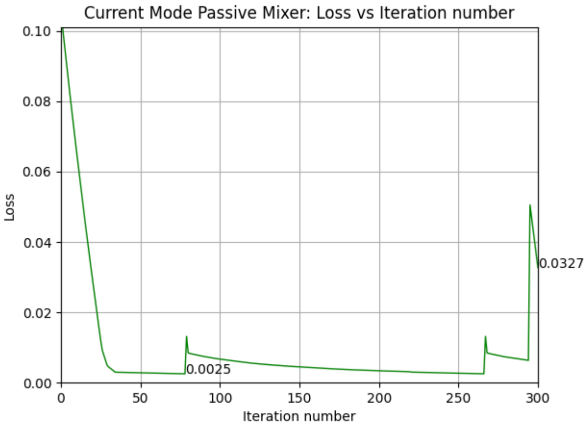


Figure 25: Loss vs iterations for current mode mixer

Current Mode Passive Mixer - Optimisation Results (cont.)

S_{11} process and temperature variations

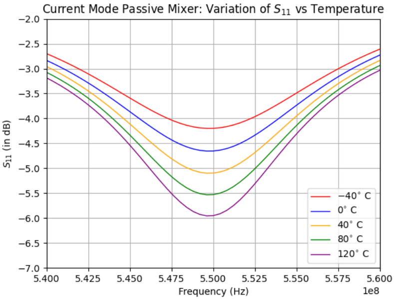


Figure 26: Temperature

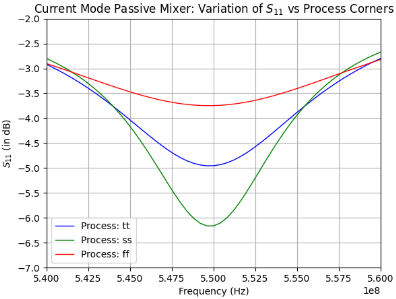


Figure 27: Process variations at 27°C

Gain process and temperature variations

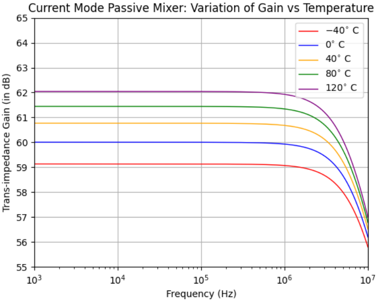


Figure 28: Temperature

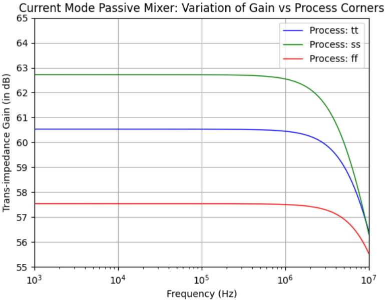
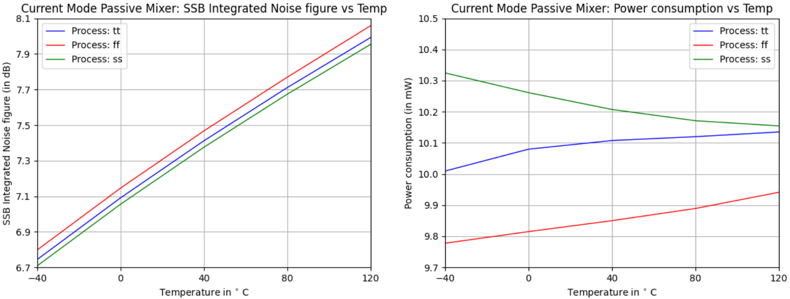


Figure 29: Process variations at 27°C

Current Mode Passive Mixer - Optimisation Results (cont.)



Conclusion

In this project,

- I have automated the schematic design of double-balanced fully differential **voltage** and **current mode** passive downconversion mixers
- Optimisation algorithm used - Gradient Descent
- Quadrature LO waveforms with 25% duty cycle are used to drive both mixers
- Specifications optimised are - input impedance matching S_{11}, conversion gain, integrated single sideband (SSB) noise figure, IIP_3 and power consumption
- Temperature and process variations are analysed post-optimisation using Python code

Further Improvements

- Expand Automatic RFIC synthesis for more mixer circuit topologies
- Automation for Layout design
- The local minimum achieved in gradient descent depends on the choice of initial circuit parameters in the netlist. Hence the **role of a circuit designer is very important** in converging to the optimum solution faster.

Thank You