README FILE

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Description :

This is a five-stage 32-bit RISC pipeline with a simplified instruction set. It has a hardwired control unit and a dual port register unit with 32 GPRs. The memory address is 24-bit wide (as it is the maximum size we can use in Logisim), and the data bit is 32-bit wide.

STEPS TO RUN THE PROGRAM IN LOGISIM

- Click the reset button or Ctrl+R to reset the circuit to its default configuration.
- First, we need to manually set the counter to 4 (which implies that stage 5 is complete), and we can start afresh from stage 1 for the implementation of instruction. The counter can be accessed by right clicking the control unit and viewing it.
- Then, we can access the memory by using the poke tool. We can load the instructions using an image (select the load image option). We can start the instruction from any start base address.
- Now using the poke tool, double click the fetch unit and set the PC to the address of the first instruction to be executed.
- Then, Ctrl+K is used to enable the clock trigger and start the circuit.
- Wait for the result computation until the Halt instruction is Executed. After the halt instruction, the stage counter stops and hence program execution is completed.
- We can view the result in the specific address of the RAM (this address depends on the program).