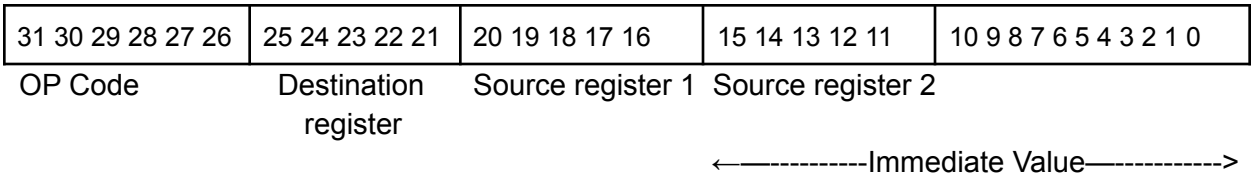
32-Bit RISC Processor Pipeline
Instruction Encoding Scheme

Encoding Scheme:



In the next page, we have explained the register file encoding and the 13 instruction encoding.

Register Encoding Table:

Registers	Decimal Encoding	Binary Encoding	Hexadecimal Encoding
R1	0	00000	0
R2	1	00001	1
R3	2	00010	2
R4	3	00011	3
R5	4	00100	4
R6	5	00101	5
R7	6	00110	6
R8	7	00111	7
R9	8	01000	8
R10	9	01001	9
R11	10	01010	A
R12	11	01011	B
R13	12	01100	C
R14	13	01101	D
R15	14	01110	E
R16	15	01111	F
R17	16	10000	10
R18	17	10001	11
R19	18	10010	12
R20	19	10011	13
R21	20	10100	14
R22	21	10101	15
R23	22	10110	16
R24	23	10111	17
R25	24	11000	18
R26	25	11001	19
R27	26	11010	1A
R28	27	11011	1B
R29	28	11100	1C
R30	29	11101	1D
R31	30	11110	1E

Instruction Encoding Table:

Instruction	Op-Code
MOV	XX0000
MVI	XX0001
ADD	XX0010
ADI	XX0011
SUB	XX0100
SUI	XX0101
AND	XX0110
ANI	XX0111
OR	XX1000
ORI	XX1001
LOAD	XX1010
STORE	XX1011
HLT	XX11XX

A=B+C-Immediate,X=10,Y=12,Z=12 and Immediate=16.

Example instructions :

Address	Assembly Code	Machine Code
000000	Load R1, X, R2	2801000A
000001	Load R3, Y, R2	2841000B
000002	ADD R1, R1, R3	01130000
000003	SUI R1, R1, #Immediate	91100010
000004	Store R1, Z, R2	6120000C
000005	HLT, Halts Instruction	C0000000