Counters

The diagram (Figure 1), shows a counter composed of J-K flip flops. Clock pulses are input at the leftmost flip flop. The output from this flip flop is connected to the clock input of the next. The J and K inputs are held at logic 1 so that the flip flops toggle on each clock pulse. However, the clock pulse rate seen by the second flip flop is only half the rate of that seen by the first. This happens because the clock pulse for the second comes from the output of the first. The same is true for the other flip flops, i.e., the clock pulse rate seen by each is only half that of its predecessor on the left. This models binary counting as shown in the table (Table 1). Remember however, that Q1 is the least significant bit (LSB) and Q4 the most significant bit (MSB).

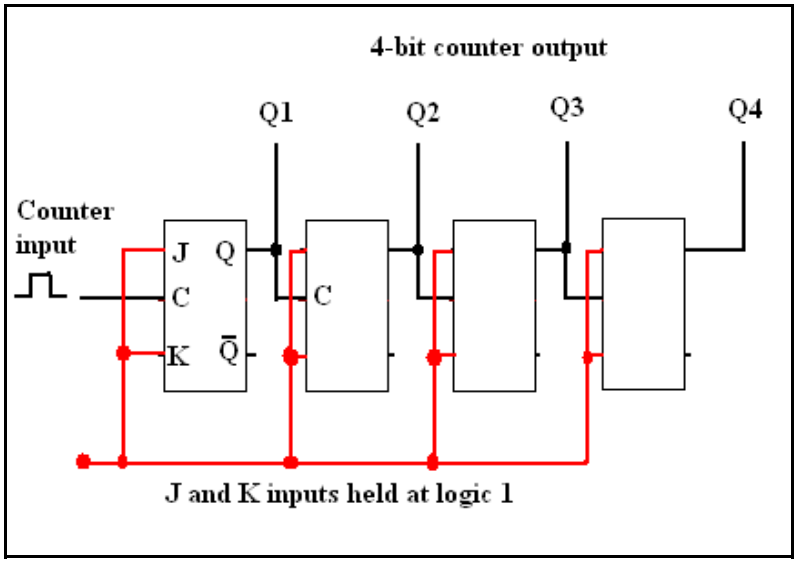

Figure 1. A 4-bit counter composed of J-K flip flops.

Clock Pulse	Q4	Q3	Q2	Q1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	1	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Table 1. Q1 toggles on every clock pulse, Q2 at half this rate etc.