Computer Architectures & Operating Systems

Lecture 3: Digital Logic & Truth Tables

Chips & Logic Gates

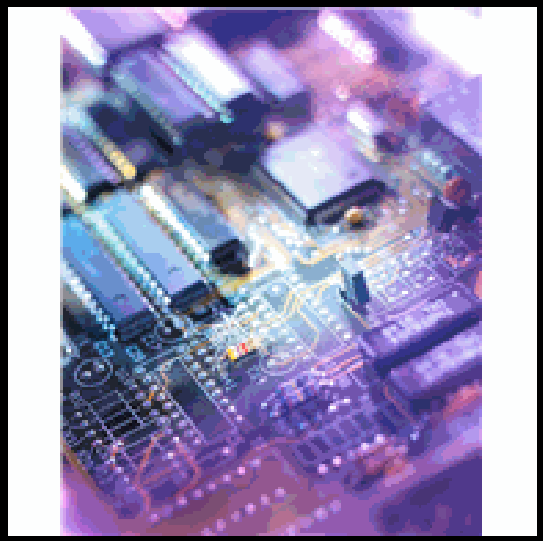


Figure 1: A circuit board populated with chips.

- Digital systems are built with electronic circuits.
- Logic typically represented by voltages, eg. 5V = 1 0V = 0.
- Large numbers of transistors, resistors and other components integrated onto chips.
- Design of chips is complex and specialised.
- Black box approach.
- Design building blocks are gates and chips rather than individual components.

Logic Gates

- A logic gate is a circuit with inputs and outputs that carries out logic operations such as AND, OR, NAND, NOR and NOT.
- Logic levels of inputs and outputs represented by voltages.
- Typically, 5V = Logic 1, 0V = Logic 0
- Voltage levels do not need to be absolute.
- Ceramic Metal Oxide Semiconductor (CMOS)
- CMOS devices (chips) $>$ 3.5V = 1, $<$ 1.5 = 0
- Transistor Transistor Logic (TTL)

Logic Gates

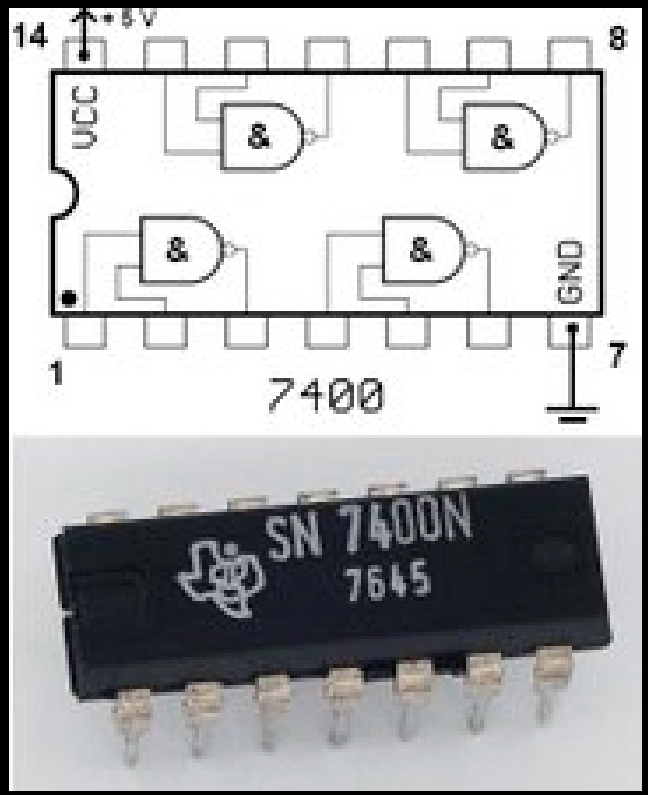


Figure 2: A TTL chip and pin-out diagram.

- The picture (Figure 2) shows a chip from Texas Instruments containing 4 NAND gates.
- The SN on the top of the chip indicates that the manufacturer is Texas Instruments.
- The number 7400 indicates that the chip is a TTL type with four AND gates.

Logic Operations: AND

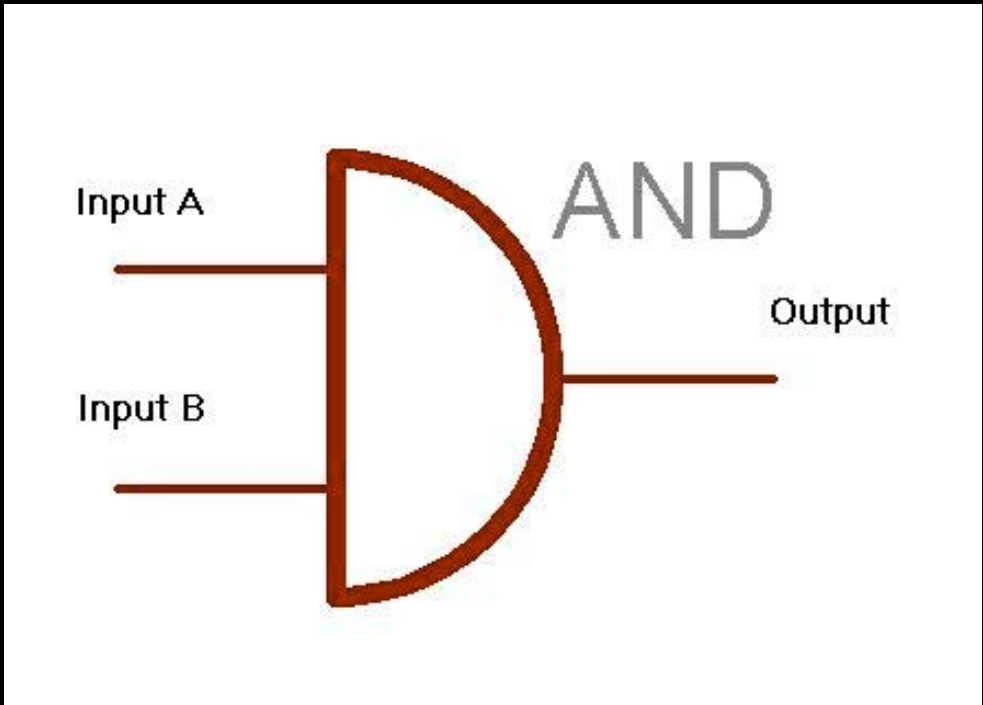


Figure 3: A two input AND gate.

- **AND**
- All inputs must be at logic 1 to get 1 at the output.
- Truth Table:

Input A	Input B	Output
0	0	0
1	0	0
0	1	0
1	1	1

Logic Operations: OR

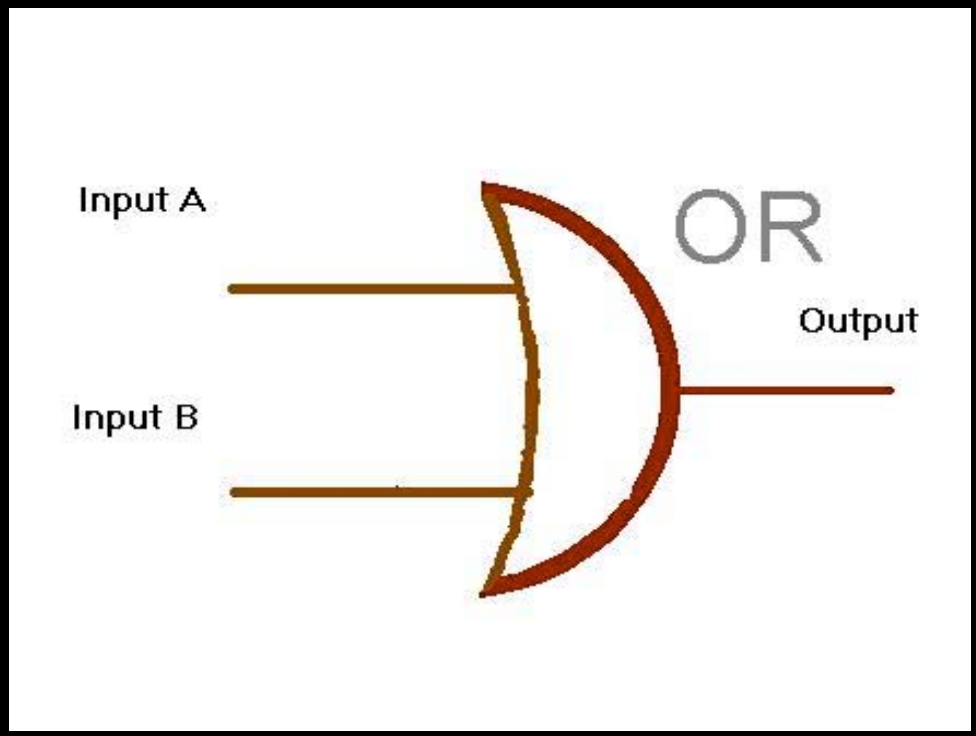


Figure 4: A two input OR gate.

- **OR**
- Output is 1 if either input is at 1.
- Truth Table:

Input A	Input B	Output
0	0	0
1	0	1
0	1	1
1	1	1

Logic Operations: NAND

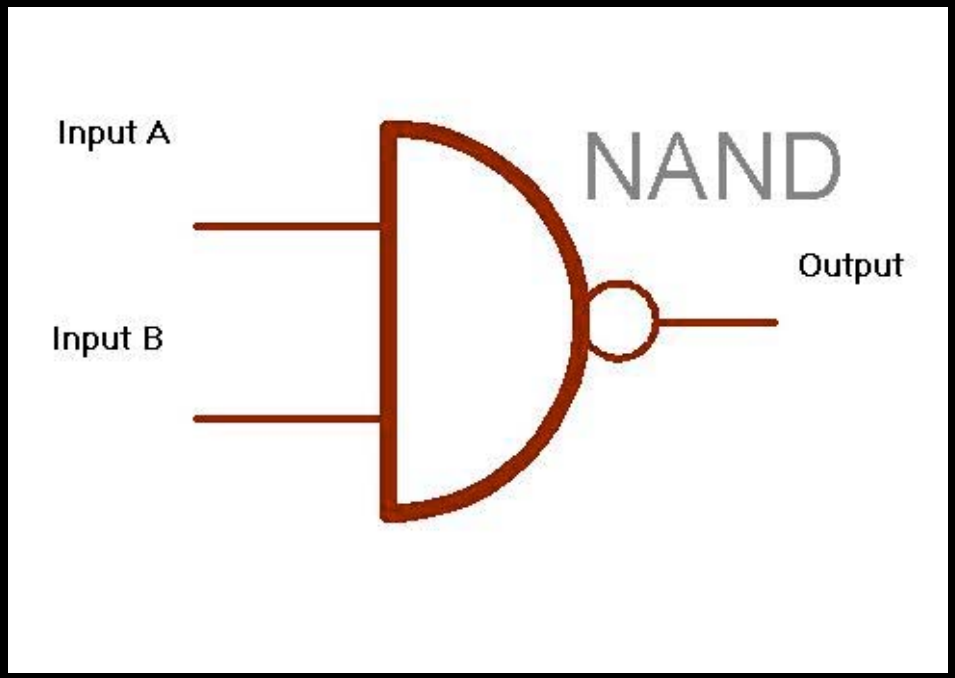


Figure 5: A two input NAND gate.

- **NAND**
- NOT AND
- Truth Table:

Input A	Input B	Output
0	0	1
1	0	1
0	1	1
1	1	0

Logic Operations: NOR

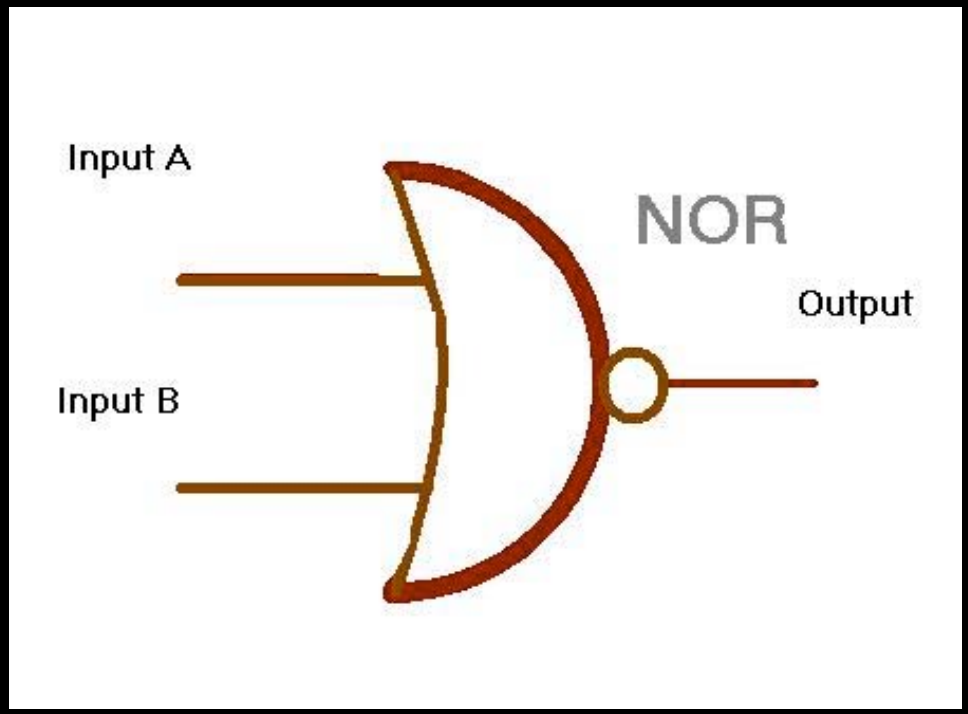


Figure 6: A two input NOR gate.

- **NOR**
- NOT OR
- Truth Table:

Input A	Input B	Output
0	0	1
1	0	0
0	1	0
1	1	0

Logic Operations: XOR

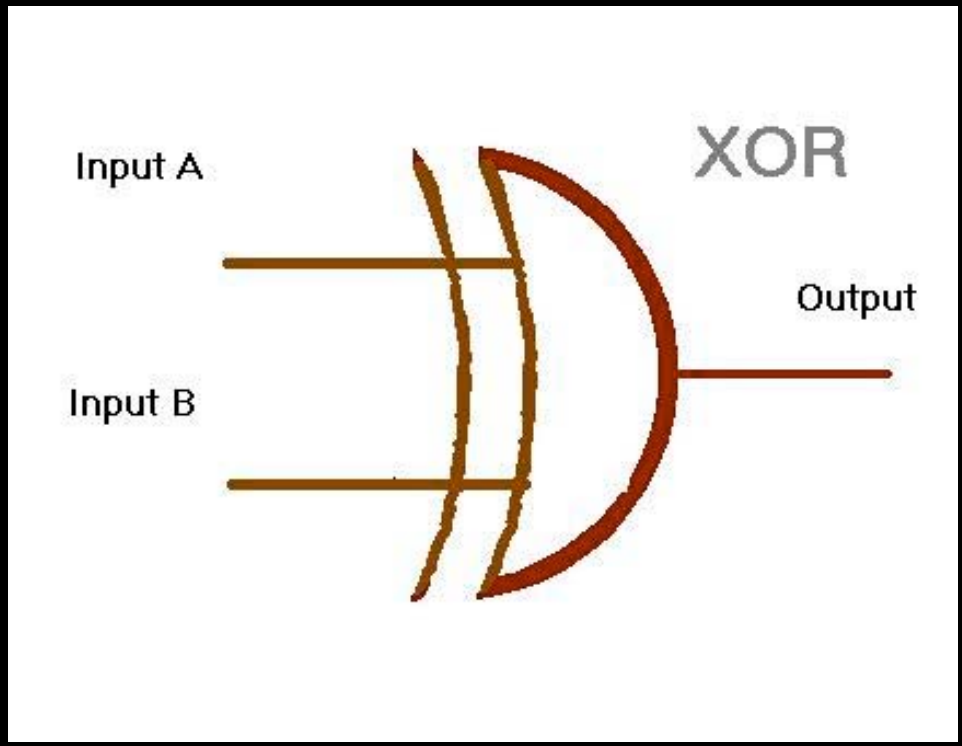
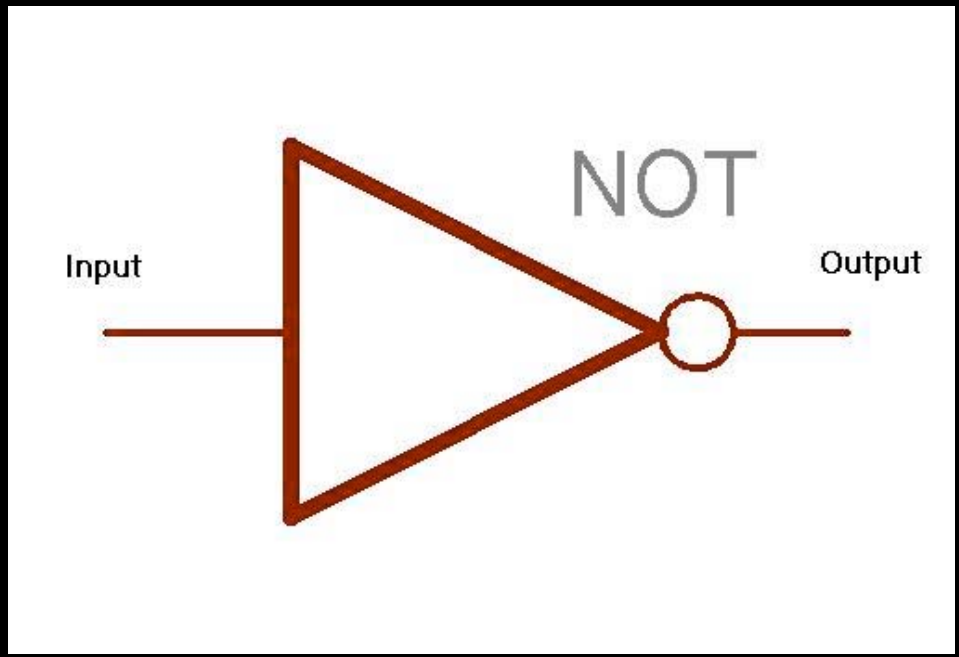


Figure 7: A XOR gate.

- **XOR (Exclusive OR)**
- To set the output to logic 1, either of the inputs must be at logic 1 but not both.
- Truth Table:

Input A	Input B	Output
0	0	0
1	0	1
0	1	1
1	1	0

Logic Operations: NOT



- **NOT**
- Inverter. Inverts the input.
- Truth Table:

Input	Output
0	1
1	0

Figure 8: A NOT gate.

Logic Operations: YES

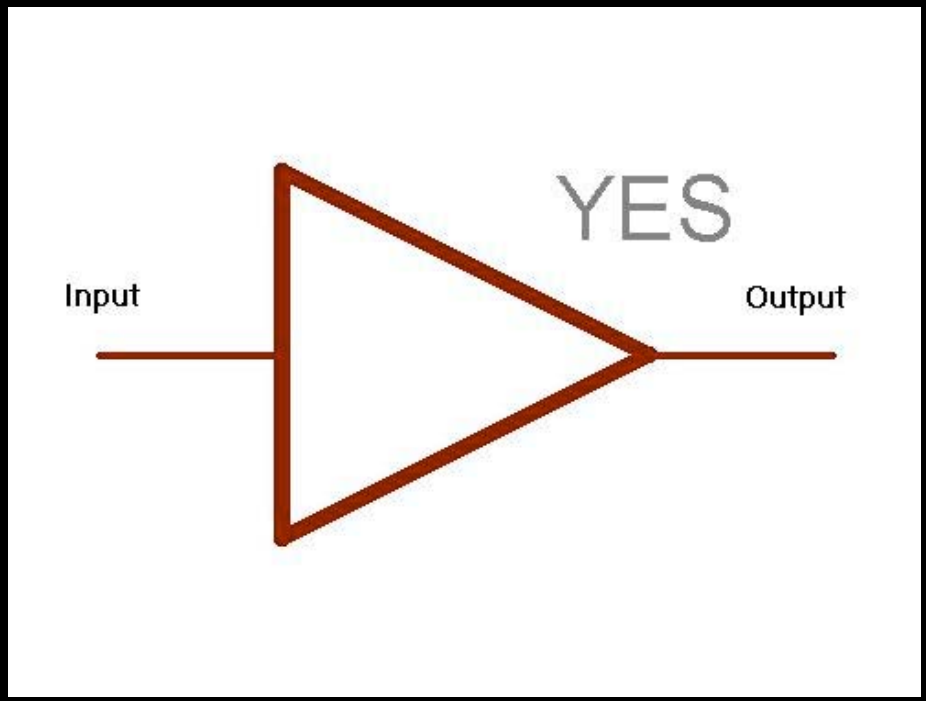


Figure 9: A YES gate.

- **YES**
- Buffer. Reproduces the input logic level as a clean logic signal.
- Truth Table:

Input	Output
1	1
0	0

Logic Operations: Problem 1

- **Problem 1:**

- Draw the truth table for the circuit shown in Figure 10.

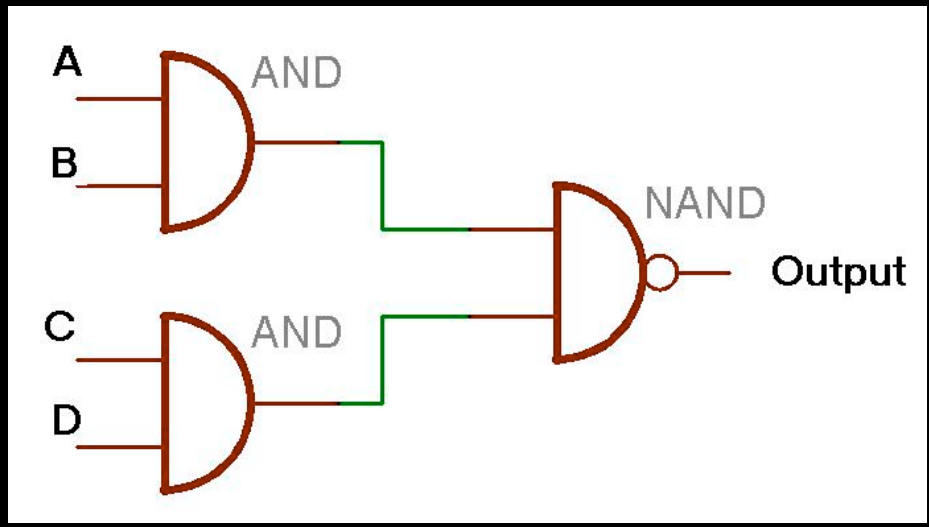


Figure 10: A four input gate circuit.

Logic Operations: Problem 2

- **Problem 2:**

- Draw the truth table for the circuit shown in Figure 11.

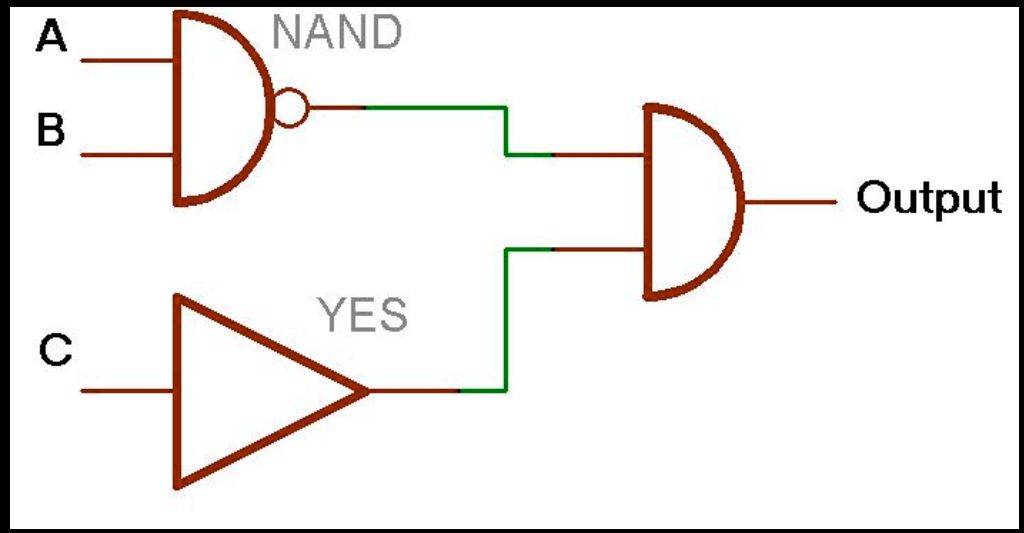


Figure 11: A three input gate circuit.

Logic Operations: Problem 3

- **Problem 3:**

- Draw the truth table for the circuit shown in Figure 12.

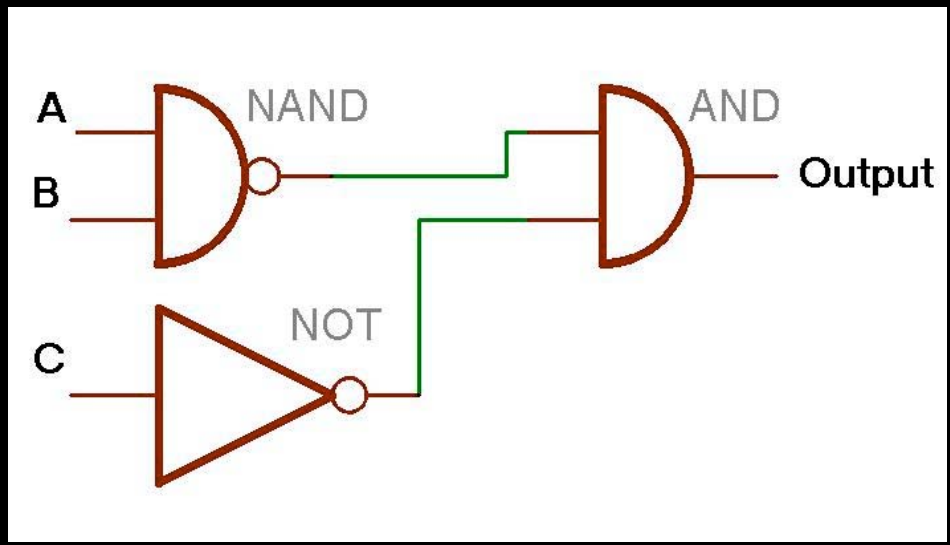


Figure 12: A three input gate circuit.

Logic Operations: Problem 4

- **Problem 4:**

- Draw the truth table for the circuit shown in Figure 13.

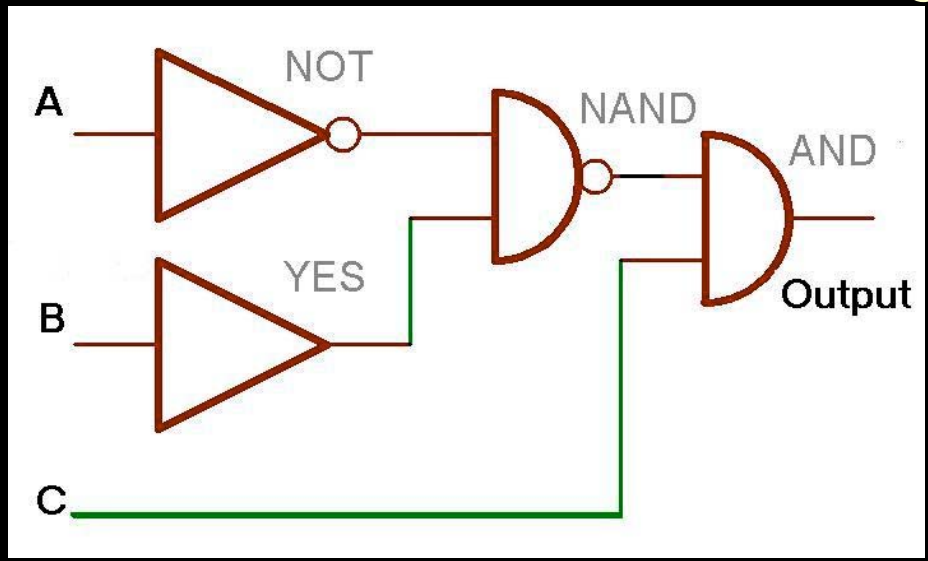


Figure 13: A three input gate circuit.

Logic Operations: Solution 1

- **Problem 1:**
- **Solution**

A	B	AB(out)	C	D	CD(out)	Output
0	0	0	0	0	0	1
0	0	0	0	1	0	1
0	0	0	1	0	0	1
0	0	0	1	1	1	1
0	1	0	0	0	0	1
0	1	0	0	1	0	1
0	1	0	1	0	0	1
0	1	0	1	1	1	1
1	0	0	0	0	0	1
1	0	0	0	1	0	1
1	0	0	1	0	0	1
1	0	0	1	1	1	1
1	1	1	0	0	0	1
1	1	1	0	1	0	1
1	1	1	1	0	0	1
1	1	1	1	1	1	0

Figure 10a: Truth table for the circuit in Figure 10.

Logic Operations: Solution 2

- **Problem 2:**
- **Solution**

A	B	AB(out)	C	C(out)	Output
0	0	1	0	0	0
0	0	1	1	1	1
1	0	1	0	0	0
1	0	1	1	1	1
0	1	1	0	0	0
0	1	1	1	1	1
1	1	0	0	0	0
1	1	0	1	1	0

Figure 11a: Truth table for the circuit in Figure 11.

Logic Operations: Solution 3

- **Problem 3:**
- **Solution**

A	B	AB(out)	C	C(out)	Output
0	0	1	0	1	1
0	0	1	1	0	0
1	0	1	0	1	1
1	0	1	1	0	0
0	1	1	0	1	1
0	1	1	1	0	0
1	1	0	0	1	0
1	1	0	1	0	0

Figure 12a: Truth table for the circuit in Figure 12.

Logic Operations: Solution 4

- **Problem 4:**
- **Solution**

A	A(out)	B	B(out)	Nand(out)	C	Output
0	1	0	0	1	0	0
0	1	0	0	1	1	1
0	1	1	1	0	0	0
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	0	1	1	1
1	0	1	1	1	0	0
1	0	1	1	1	1	1

Figure 13a: Truth table for the circuit in Figure 13.