4 Bit Latch Using D Flip Flops

Latch Definition

A *latch* is an electronic logic circuit that has two inputs and one output. One of the inputs is called the***SET*** *input;* the other is called the ***RESET*** *input.*

Latch circuits can be either active-high or active-low. The difference is determined by whether the operation of the latch circuit is triggered by HIGH or LOW signals on the inputs.

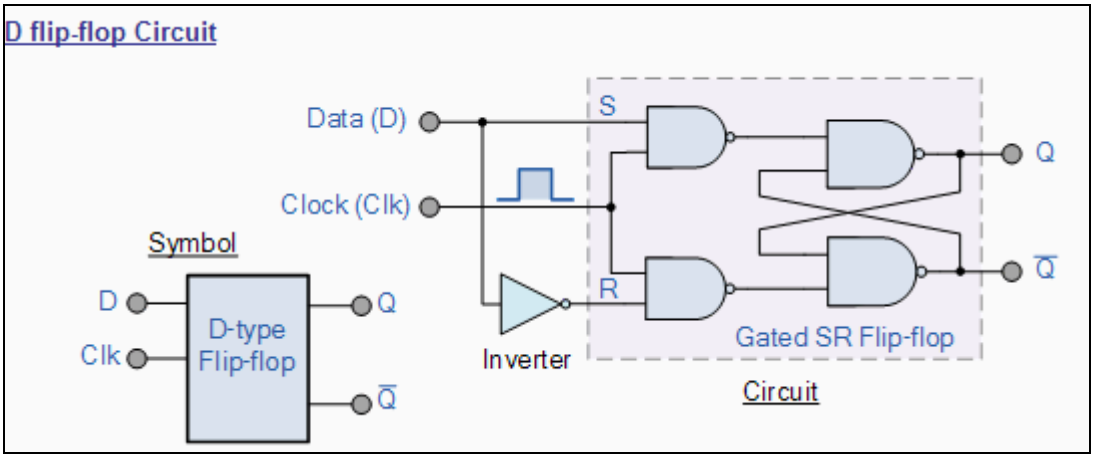
- **Active-high circuit:** Both inputs are normally tied to ground (LOW), and the latch is triggered by a momentary HIGH signal on either of the inputs.
- **Active-low circuit:** Both inputs are normally HIGH, and the latch is triggered by a momentary LOW signal on either input.

More Information:

http://www.dummies.com/how-to/content/electronics-basics-what-is-a-latch-circuit.html

D Flip Flop

D flip-flop Circuit

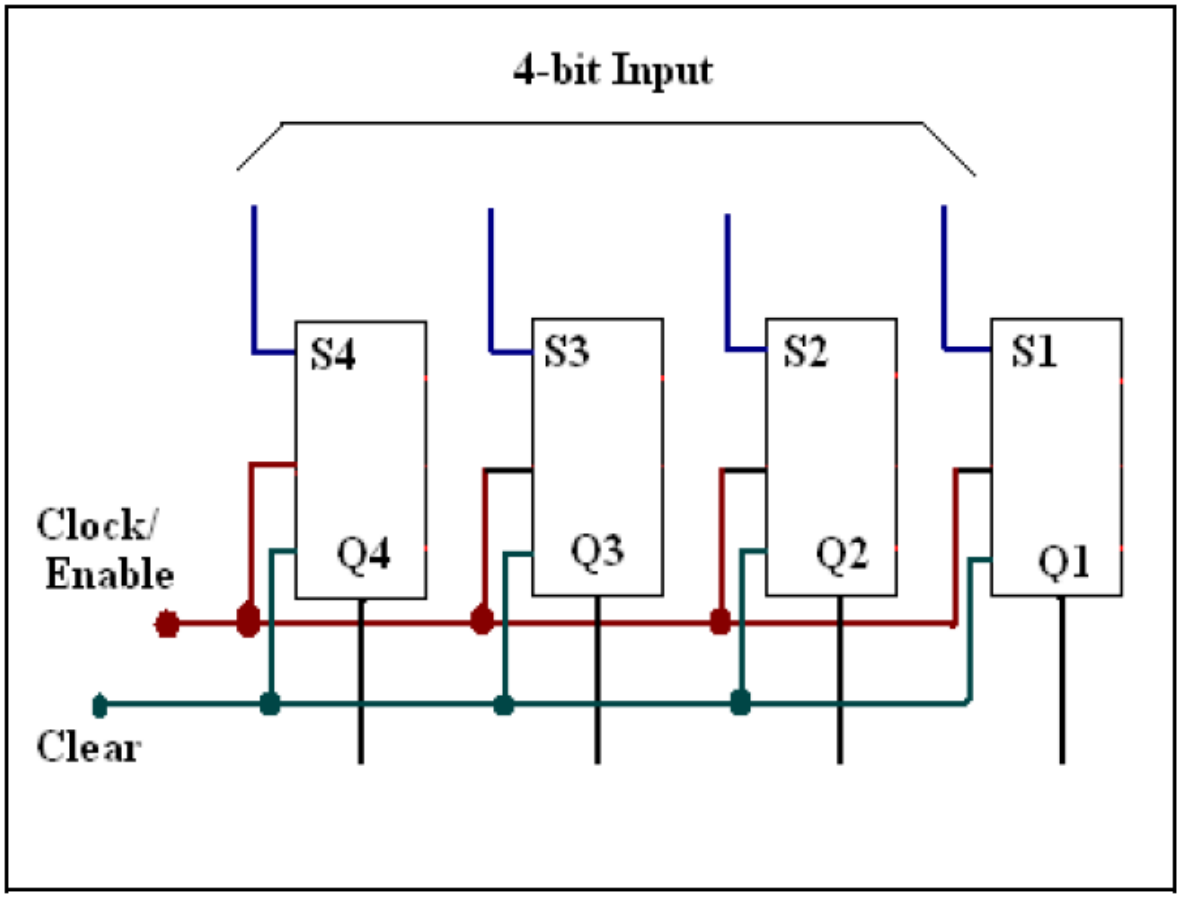


Truth Table for the D Flip-flop

Clk	D	Q	$\overline{Q}$	Description
↓ » 0	X	Q	$\overline{Q}$	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1

Note: ↓ and ↑ indicates direction of clock pulse as it is assumed D flip-flops are edge triggered

4 Bit Latch Circuit



4 Bit Latch Operation

- The clock inputs are connected in parallel.
- The data is placed on the four inputs.
- The data can only pass through to the Q outputs when the clock line goes high (logic 1).
- A clear line allows the latch to be reset.

CLK	D	Q
0	X	last state
1	0	0
1	1	1

CLK → low: D can change without effect on the output

CLK → high: Q is forced to equal the value of D

Ex: Create a 4 bit data memory with D-latches (D-FF).

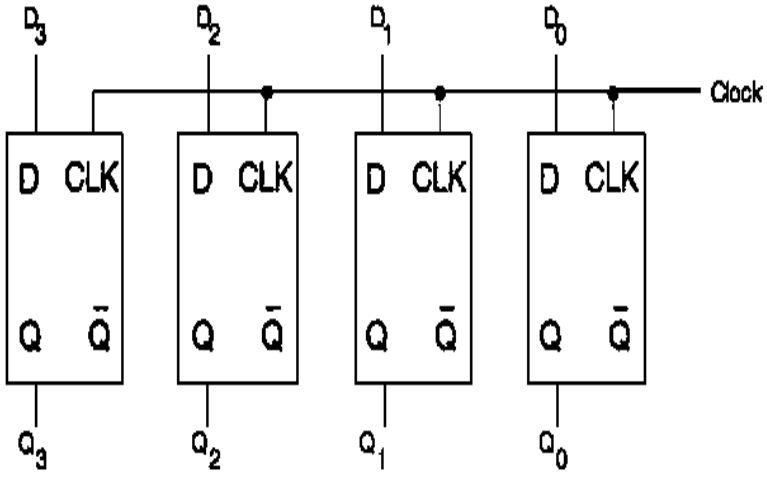


Fig. 7-9: Data storage with D-FF

In Fig. 7-9, when the clock goes high, input data is loaded into the Flip-Flops and appears at the output.

Suppose the data input is:

$D_3 D_2 D_1 D_0 = 1\ 0\ 1\ 0$

When the clock goes high this 4 bit word is loaded into the D-latches, resulting in an output of:

$Q_3 Q_2 Q_1 Q_0 = 1\ 0\ 1\ 0$