Adder Subtracter

The diagram (Figure 1), shows a 4 bit adder/subtracter. It consists of a 4 full adders with provision for inverting one set of inputs. Additionally, there is a carry-in to the LSB full adder when subtraction is performed. The subtract line is asserted (logic 1) to carry out subtraction and de-asserted (logic 0) for addition. Inversion is performed with the help of XOR gates.

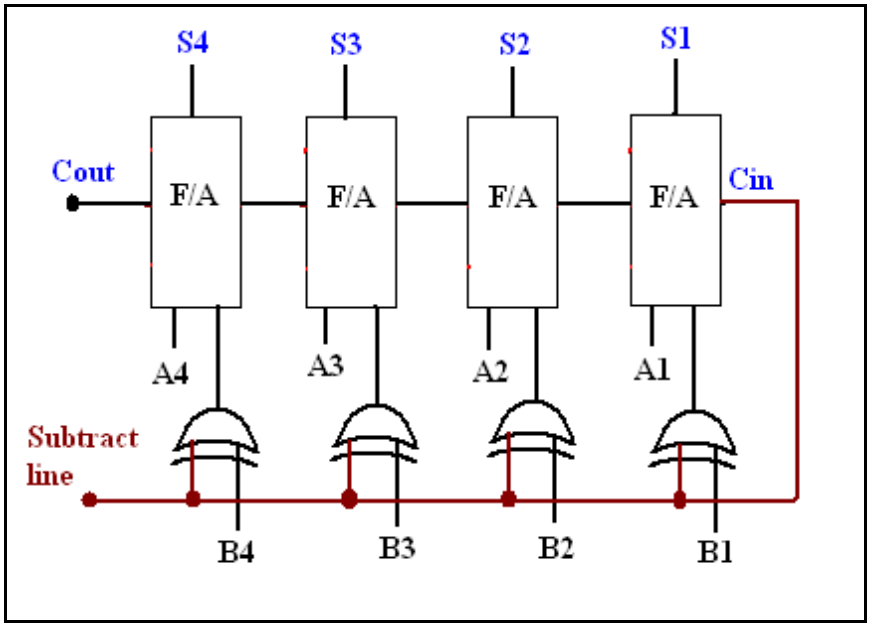

Figure 1. 4-bit Adder/subtracter

Ripple Carry Addition

The adder/subtracter shown in Figure 1 uses ripple carry to calculate carry bits. In the context of modern computing, where clocks are extremely fast and where the adder may be up to 128 bits wide, ripple carry would result in very poor performance. Each full adder would have to wait on a carry in from the right hand side. This process could take a long time if the carry ripples across 64 or even 128 adders.

To address this, carry look ahead (CLA) is used. CLA adds considerably more hardware. It implements the carry rules for sets of typically 4 bit sections. The carry rules are:

G: Carry generation occurs if both bits to be added are 1
P: Carry propagation occurs if either one or other bit is 1 and if there is a carry in

These are essentially AND/OR rules and require AND as well as OR gates to be added to the existing full adder architecture. The cost of this is considerable. However, the tradeoff is the much improved performance.