S-R Flip Flop

The S-R flip flop or latch (Figure 1), is a simple data storage circuit. This type of flip flop may be constructed using cross-coupled NOR gates. The flip flop is set by placing logic 1 on the Set (S) input. This causes the Q output to go high (logic 1). The S input may then be returned to logic 0. The Q output however, holds its state i.e., it stays at logic 1.

If the Reset (R) input is now asserted (logic 1), the flip flop is reset. This means that logic 0 now appears at Q and logic 1 appears at $\overline{Q}$. Note that returning an input to logic 0 has no effect on the outputs. The flip flop only responds to asserts (logic 1 inputs). The behaviour of the flip flop is further illustrated in Table 1.

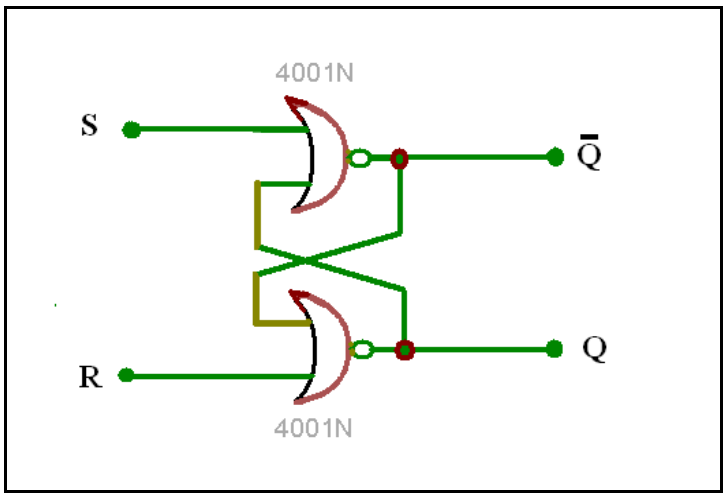

Figure 1. An S-R flip flop constructed from cross-coupled NOR gates

S	R	Q	$\overline{Q}$	Comment
1	0	1	0	Flip flop set
0	1	0	1	Flip flop reset
0	0	Q	$\overline{Q}$	Hold -Q states stored
1	1	0	0	Not used

Table 1. Truth table for the half adder