Half Adder

The diagram (Figure 1), shows a half adder built with AND and XOR gates. Remember that the AND gate outputs logic 1 only when both inputs are at logic 1. The XOR gate outputs logic 1 only when either one or the other inputs is at logic 1 but not both. The half adder has two outputs. This is because the addition of the binary bits at A and B will result in a sum but there may also be a carry. The truth table (Table 1) illustrates this well. It can be seen from the table that the carry is only generated when both inputs to be added are at logic 1. In this case (The last row of the truth table), the sum is zero with carry 1.

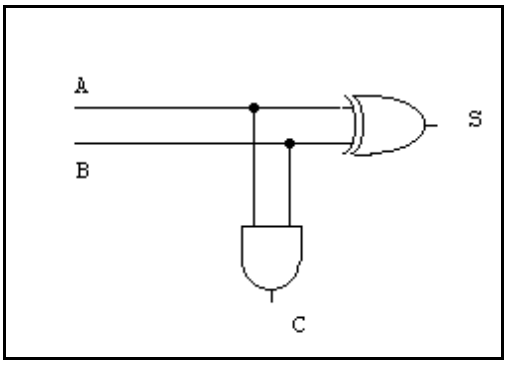

Figure 1. Half adder built with AND and XOR gates

A Binary digit input
B Binary digit input
S Sum
C Carry (out)

A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Table 1. Truth table for the half adder

Half Adder Limitation

Although the half adder correctly adds the two bits at A and B, it is lacking in one key respect: Although it has a carry out, there is no carry in. Therefore the half adder needs further refinement before it can be used for the addition of multibit binary numbers. The provision of a carry in results in the creation of a full adder. Full adders can then be connected together to perform 8-bit, 16-bit or 32 bit addition.