Shift Register

The diagram (Figure 1), shows a shift register composed of J-K flip flops. Data is input serially on the left hand side. The logic applied to the J input is inverted to be applied to the K input. All clock inputs are connected in parallel to a common clock line. When the clock goes high (logic 1), the first bit of serial data moves to Q1. The next time the clock goes high, this bit moves on to Q2 and the following serial bit appears on Q1.

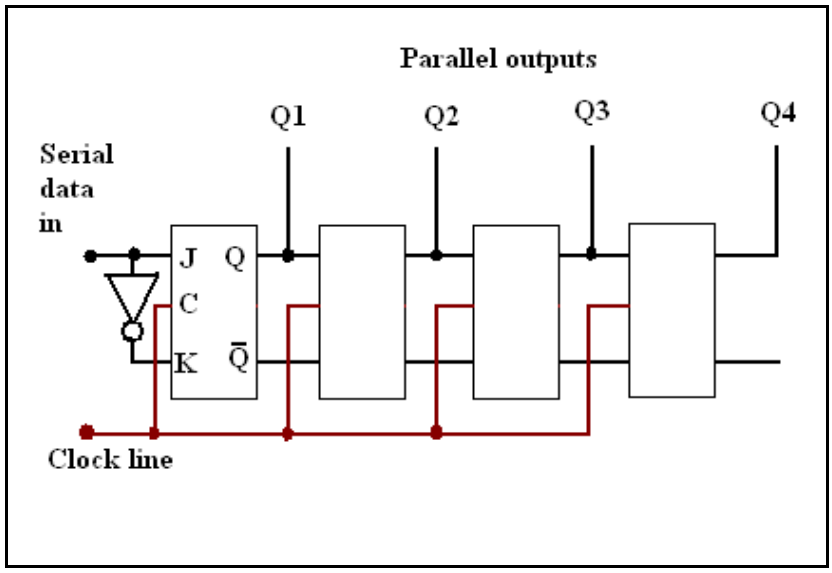

Figure 1. Shift register

The table (Table 1) illustrates how this happens if the data 1001 is applied to the serial input. Imagine at first that the Q outputs are all at zero logic. After the first clock pulse logic 1 appears on Q1. On clock pulse 2, this 1 bit moves to Q2 and a zero bit now comes in on Q1. The third clock pulse sees the leading 1 bit move to Q3, the zero on Q1 moves to Q2 and a new zero bit comes in on Q1. Finally, on clock pulse 4, the leading 1 bit moves to Q4. The zero bits move along to occupy Q3 and Q4 and a new 1 bit comes in on Q1. The serial data is now available in parallel on the Q outputs.

Clock Pulse	Q1	Q2	Q3	Q4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	1	0	0	1

Table 1. After 4 clock pulses, the serial data 1001 is present on the Q outputs.

Shift Register Applications

Shift registers can be used in the context of I/O operations to construct serial in parallel out (SIPO) data converters. They could also be used for arithmetic shift operations. For example, a single shift left multiplies by two, whereas a single shift right divides by two.