

**Griffith College Limerick**

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| **Student number:** | **2960992** | | |  | | |
| **Faculty:** | Computing Science | | | | | |
| **Course:** | BSc in Computing Science | | | Stage/Year: | 1 | |
| **Module:** | EffectiveLearning and Development | | | | | |
| **Study Mode:** | Full time | **🗸** |  | Part-time |  |  |
| **Lecturer Name:** | Bridget Murphy | | | | | |
| **Assignment Title:** | Assessment 1 | | | | | |
| **URL (IF Applicable)** |  | | | | | |
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| **Date due:** 29/11/2017 |  | | | **Date submitted: 29/11/2017** | | |
| **Academic Misconduct:**  *I understand that I will be subject to the penalties imposed for breaches of academic conduct as defined in the College’s Academic Misconduct Procedure (QA J6).*  **Signature: Sarah Narayamy Tavares Silva Date: 29/11/2017** | | | | | | |

## Please note: Students MUST retain a hard / soft copy of all assignments and must SIGN the Assignment Submission Sheet provided by the lecturer / member of Faculty as proof of submission.

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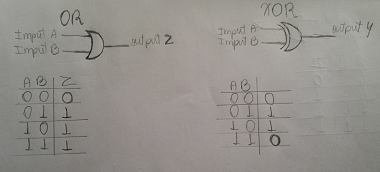
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# Distinguish between inclusive OR and exclusive OR. In support of your answer, draw the diagrams for two input OR and XOR gates. Show the truth table for each and explain how they differ.

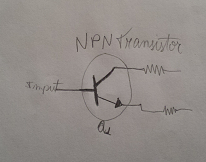
Answer:

As represented on the diagrams and truth tables below, when we have an OR operation between two inputs, the output will be 1 if either input is 1, including when both inputs are at 1. While when we have a XOR operation between two inputs, the output will be 1 when either input is 1, excluding when both inputs are 1.



# Draw the schematic symbol for a NPN bipolar junction transistor. Explain why the transistor was key to the proliferation of computers and computing devices. Outline one disadvantage of using bipolar junction type transistors in logic devices.

Answer:

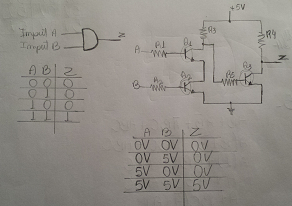


Before transistors, computers used Vacuum tubes, which turned on and off to represent zeros and ones. This technology was not efficient and was needed a lot of tubes, bulbs and heat to do basic math calculations. By the time, computers were slow and massive. Transistor, on the other hand, act as a switch, which means that if the transistor is on the current flows, but if the transistor is off the current stops. This turning on and off process can be in a velocity of 300 billion times per second.

One disadvantage of transistors is that they have low thermal stability, which means they can heat up in high temperatures, making them volatile.

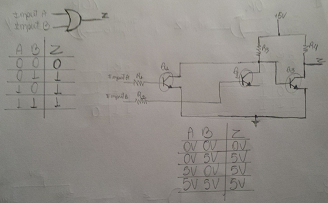
# Draw a diagram of a two input AND gate together with the corresponding truth table. With the help of a schematic diagram, show how AND might be implemented using discrete transistors.

Answer:



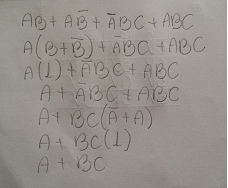
# Draw a diagram of a two input OR gate together with the corresponding truth table. With the help of a schematic diagram, show how OR might be implemented using discrete transistors.

Answer:



# Simplify, using the laws of Boolean algebra: AB + A + BC + ABC

Answer:



# Draw the combinational logic circuit to implement the Boolean expression:

# Y = ACF + AF + C

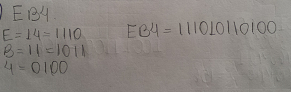
# Use Boolean algebra to simplify the expression and draw a diagram to show the simplified implementation.

Answer:

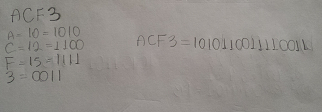
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# Convert to binary:

## EB4

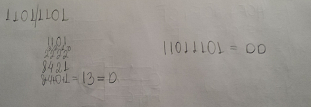


## ACF3

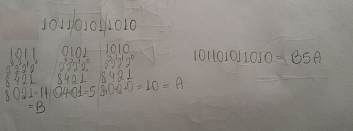


# Convert to Hexadecimal:

## 11011101

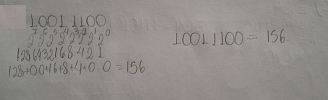


## 101101011010

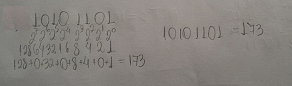


# Convert to decimal:

## 10011100



## 10101101



# Caching and pipelining are both methods of improving processor throughput. Explain how each of these approaches works. Is there any way that one of these impinges on the other?

Caching is a technology with the purpose to accelerate computers. Instructions and data are copied into cache when they are required. It can function in two ways; look-aside cache, which is connected to the memory bus so it can see main memory accesses, in this case, when something is required and it is already in cache, cache responds immediately, terminating the request. The second function is the look-through cache which a faster bus is used to connect to the processor in the arrangement. The cache is connected to main memory using the slower main memory bus.

Pipelining involves instruction level parallelism (ILP), which means that the microprocessor works with more than one instruction at the same time. The instructions are broken into down into separate parts with equal length. As soon as an instruction exists a block, the next instruction enters, so the block will be always busy. Pipelining has 4 stages: Fetch. Decode, Decode Operand fetch, Execute and Writeback.

Delays can occur due to memory operations. For example, a cache miss.