

**Griffith College Limerick**

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| **Student name:** | **ASSIGNMENT COVER SHEET**  **Sarah Narayamy Tavares Silva** | | | | | |
| **Student number:** | **2960992** | | |  | | |
| **Faculty:** | Computing Science | | | | | |
| **Course:** | BSc in Computing Science | | | Stage/Year: | 1 | |
| **Module:** | Computer Hardware | | | | | |
| **Study Mode:** | Full time | **🗸** |  | Part-time |  |  |
| **Lecturer Name:** | Bridget Murphy | | | | | |
| **Assignment Title:** | Assignment 02 | | | | | |
| **URL (IF Applicable)** |  | | | | | |
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| **Date due:** 28/03/2018 |  | | | **Date submitted: 28/03/2018** | | |
| **Academic Misconduct:**  *I understand that I will be subject to the penalties imposed for breaches of academic conduct as defined in the College’s Academic Misconduct Procedure (QA J6).*  **Signature: Sarah Narayamy Tavares Silva Date: 28/03/2018** | | | | | | |

## Please note: Students MUST retain a hard / soft copy of all assignments and must SIGN the Assignment Submission Sheet provided by the lecturer / member of Faculty as proof of submission.

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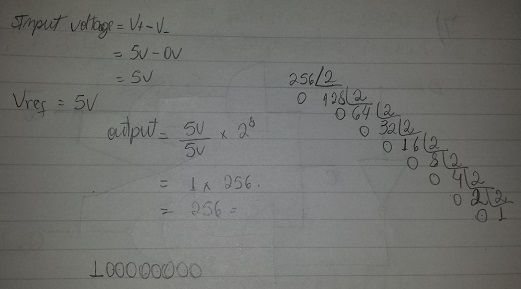
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# An ADC804 chip is connected to a sensor that outputs a voltage in the range 0V to 5V. The A-D reference voltage is the same as the supply voltage at 5V. Show how the resolution in Volts is calculated.

Answer:



# Outline two limitations of the sign and magnitude approach to the representation of signed integers

Answer:

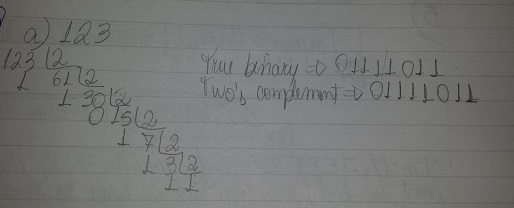
1- Addition and subtraction require a consideration of both the signs of the numbers and their relative magnitudes to carry out the required operation.

2- There are two representations of 0.

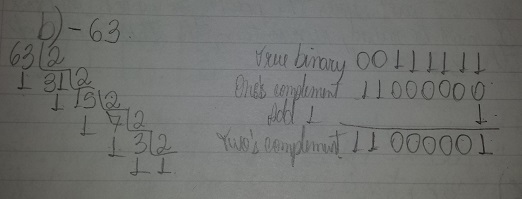
Because of these drawbacks, sign-magnitude representation is rarely used in implementing the integer portion of the ALU.

# Convert to 8-bit two’s complement:

## 123

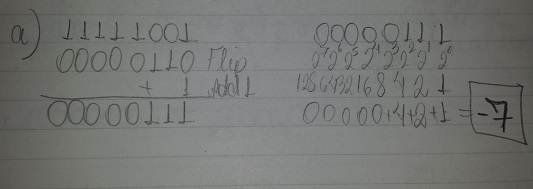


## -63

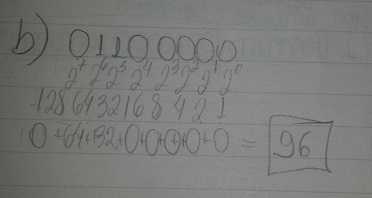


# Convert the following two’s complement numbers to decimal:

## 1111 1001

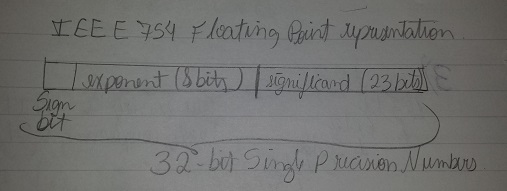


## 0110 0000



# With the help of a diagram, explain how the IEEE 754 approach represents single precision floating point numbers.

Answer:



In the IEEE 754 single precision, 32 bits, floating point standard; one sign bit is used to indicate if the analysed number is positive or negative. 23 bits are used to store the significant. The exponent part stores the power to which the base 2 must be raised, representing the other 8 bits of the 32 overall.

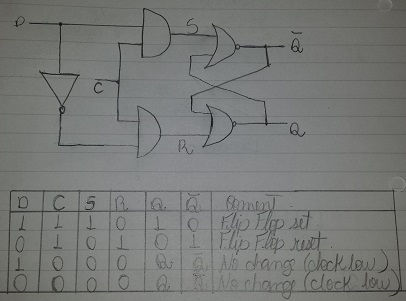
# Show how -36.125 is represented using the IEEE 754 approach

Answer:

|  |  |
| --- | --- |
| C:\Users\Sarah\Google Drive\Computer Hardware\6.jpg |  |

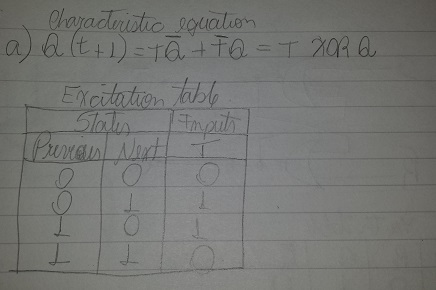
# With the help of a labelled diagram, show how the S-R flip flop can be gated with the addition of further logic gates to control the inputs to the flip flop.

Answer:

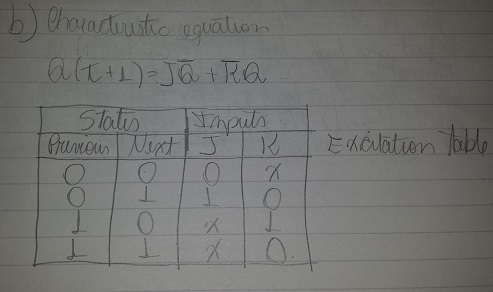


This type of flip flop is constructed by extending the S-R flip flop. The flip flop is gated with two AND gates which means that logic 1 inputs to the flip flop can only pass through when the C input is also at logic 1. The two inputs of the S-R flip flop are connected together using an inverter, which means that the inputs are reduced to one. Additionally, the S input is inverted to apply the complementary logic to the R input. The D flip flop will store either a 1 or a 0 applied to its input when the C (clock) input goes high.

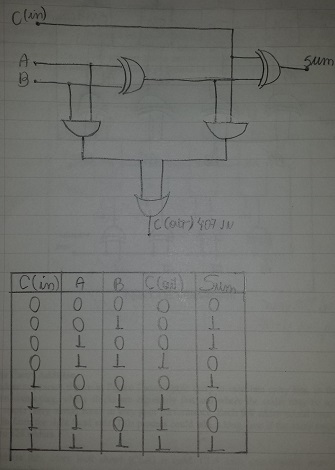
# (a) Write the characteristic equation and the excitation table for the T flip flop.



# (b) Write the characteristic equation and the excitation table for the J-K flip flop.

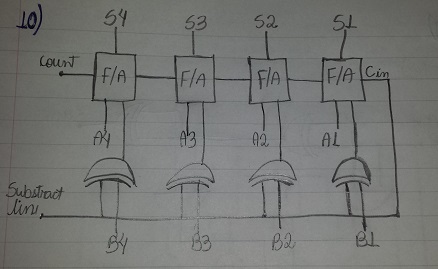


# With the help of a diagram and function table, explain how half adders can be combined to form a full adder.



This diagram shows a half adder built with AND and XOR gates, it has two outputs. This is because the addition of the binary bits at A and B will result in a sum but there may also be a carry. However, the half adder does not support a carry in. To remedy this, two half adders can be combined to form a full adder. The second half adder combines the sum output from the first with a carry in bit. An OR gate provide the carry out bit. The truth table shows the possible input s and the resulting outputs. The full adder can be used for the addition of multibit binary numbers. Full adders can be connected together to perform 8-bit, 16-bit or 32 bit addition.

10. With the help of a diagram, explain how a tow’s complement adder/subtracter can be created by combining a 4-bit full adder with a controlled inverter.



The 4-bit adder/subtracter consists of a 4 full adders with provision for inverting one set of inputs. Additionally, there is a carry-in to the LSB full adder when subtraction is performed. The subtract line is asserted (logic 1) to carry out subtraction and de-asserted (logic 0) for addition. Inversion is performed with the help of XOR gates.