

Addressing Modes

→ Indirect Addressing Mode

Mov A, 30h] → Mov R0, #30h
 Mov A, @R0

Syntax

Mov A, @Rp

Mov @Rp, A

Mov @Rp, #n

Mov @Rp, addr

Mov addr, @Rp

Mov addr, @R,

// ALP to copy the data from 70h ~~to R0 to R2~~ to R0 to R2

Mov 70h, #11h

Mov R0, 70h

Mov R1, 70h

Mov R2, 70h

Mov R3, 70h

Mov R4, 70h

// ALP to copy data from R0 to 30h to 33h

Mov R0, #30h

Mov R1, #31h

Mov 31h, @R0

Mov A, @R1

Mov @R1, 31h

Mov @R0, A

→ Direct Addressing Mode

Mov R_i, addrs

Mov A, addrs

Mov addrs, R_j

Mov addrs, #n

Mov addrs1, addrs2

Mov addrs, *

→ Immediate Addressing Mode

The operand is present in instruction

Mov A, #n

Mov R_i, #n

Mov DPTR, #nn

↳ 16 bit

→ Register Addressing Mode

Mov A, #30H

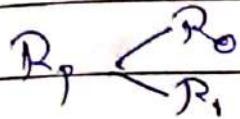
Mov R₀, A

Mov R₁, A

}

Mov R₂, *

Indirect Addressing Mode



Mov R₁, #40h

R₁ ← 40h

Mov A, #33h

A ← 33h

Mov @R₁, A

Mov A, 30h] → Mov R₀, #30h
Mov A, @R₀

Syntax

Mov A, @R_p

Mov @R_p, A

Mov @R_p, #n

Mov @R_p, addr

Mov addr, @R_p

Mov @R_p, @R_p

// Alp to copy data at 30h to R0 to R2

Mov 30h, #30h

Mov R0, 30h

Mov R1, 30h

Mov R2, 30h

Mov R3, 30h

// Alp to copy data from R0 to 30h to 33h

Mov 30h, R0

Mov 33h, R0

Mov 30h, R0

Mov 33h, R0

END

// Alp to load immediate value in register

Mov R1, #30h

Mov R0, #301h

TOD

// Alp using indirect addressing mode & exchange the
contents of 30h to 40h

direct → // Mov 31h, 20h

Mov 30h, 40h

Mov 40h, 31h

Indirect Addressing Mode $\rightarrow //$

Mov R₀, #30h

Mov R₁, #40h

Mov A, @R₀

Mov B, @R₁

Mov @R₀, B

Mov @R₁, A

DJ

Mov R₀, #30h

Mov A, @R₀

Mov @R₀, 40h

Mov 40h, A

END

\rightarrow Transfer 5 bytes of data from 30h to 40h onwards
using direct mode

Mov A, 30h

Mov 30h, 40h

Mov 40h, A

Mov A, 31h

!

Byte level → Logical Operations

AND

AND A, #n

AND A, Rn

AND A, add

AND A, @Rp

AND add, A

AND add, #n

n → Any value (Hexadecimal)

addr → Internal RAM Address

eg - MOV A, #54H

54H → 0101 0100

MOV R0, #32H

32H → 0011 0010 &

AND A, R0

0001 0000

A ← 10H

ORL

ORL A, #n

ORL A, Rn

ORL A, add

ORL A, @Rp

ORL add, A

ORL add, #n

→ eg - MOV A, #54H

0101 0100

MOV R1, #10H

0001 0010

ORL A, R0

0101 0110

A ← 5310

XOR : operations

XORL A, #n

XORL A, @Rp

XORL A, add

XORL add, A

XORL A, Rn

XORL add, #n

NOT operation

CPL A

clear operation

CLR A

→ HALP program that will Invert/Complement
bit of R₆ of bank0

Mov R₆, #10H

Mov A, R₆

CPL A

Mov R₆, A

END

XOR anything with FFH, we will get its complement

→ XRL 06H, #0FFH

→ ORB The contents of Port1 & Port2, put result into
0100H (Pictorial RAM)

Mov A, 90H

ORL A, 0100H

Mov DPTR, #0100H

Movx @DPTR, A

END

→ ALP to swap ~~high nibble of Ro & R~~^{Nibbles}, so that low nibble of Ro swaps with high nibble of R₁ & high nibble of R₀ swaps with low nibble of R₁

SWAP A

A → 32

SWAP 32

= 23

Mov R₀, #00H

Mov A, R₀

SWAP A, Mov R₀, A

Mov R₁, #23H

Mov A, R₁

SWAP A

XCH A, #00H

Mov R₁, A

END

O ↗

Mov R₀, #10H

Mov R₁, #20H

Mov A, R₀

SWAP A

XCH A, R₁

SWAP A

Mov R₀, A

END

→ Store most significant nibble of A in both
nibbles of R5.

Mov A, #10H

~~ANL~~ R5, A, #0F0H

Mov R5, A

SWAP A

ORL A, 00H

Mov R5, A

END

Arithmetic Operations

Increment operator (INC dest)

INC A	INC @R _p	INC add
INC R _s	INC D PTR X	

Decrement operator (DEC dest)

DEC A	DEC @R _p	DEC add
DEC R _s	DEC D PTR X	

Addition Instruction

ADD A, #n	ADDC A, #n
ADD A, R _s	ADDC A, R _s
ADD A, add	ADDC A, add
ADD A, @R _p	ADDC A, @R _p

// ALP to add bytes in RAM location 34h 435h & store result in R_s LSB in R₆ MSB

Mov A, 34h

Mov A, 35h

XOR R₆, R₆

ADD A, 35h

ADD A, 35h

Mov R_s, A

Mov R_s, A

CLR A

CLR A

ADDC A, #00h

RLC A

(00) Mov R₆, A

Mov R₆, A

END

11h	0001	0001
45h	0100	0101
	0101	0110
	56h	

T-#h	1111	0001
F5h	1111	0101
	11110	0110
	7 E 6h	

carry = 1

low byte = 66

high byte = 7

→ Add the bytes in register R₃ & R₄, put result in
RAM location 4Ah LSB, 4Bh MSB.

```

Mov R3, #10h
Mov R4, #11h
Mov A, R3
ADD A, R4
Mov 4Ah, A
CLR A
RLC A
Mov 4Bh, A
END

```

→ Subtraction

SUBB A, #0	SUBB A, @R _p
SUBB A, R ₃	
SUBB A, carry	

→ MULTIPLICATION

~~MOVUL A, B → MSByte~~

~~LSByte~~

→ Division

Div AB :- A/B

quotient → A

remainder → B

Subtract the no. 84h from RAM location 17h
if 0 → result in R₁LSB, R₁MSB

→ Subtract contents of R₁ from R₀, put back to R₁

2) MOV R₀, #10h

MOV R₁, #20h

~~MOV R₀, #10h~~

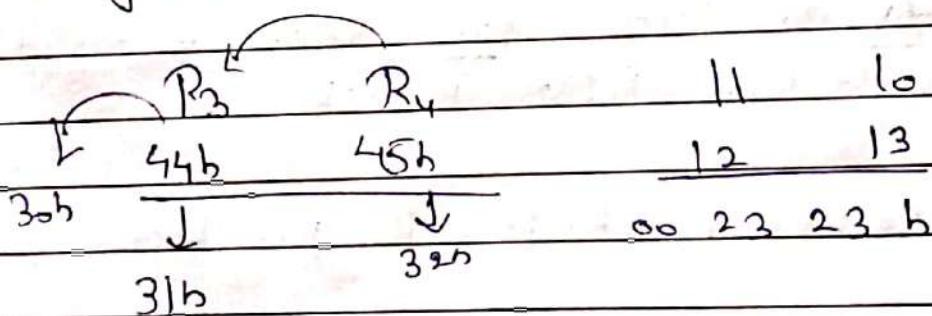
SUBR A, R₁

MOV R₁, A

$$\begin{array}{r}
 13h \\
 - 12h \\
 \hline
 1h
 \end{array}
 \quad
 \begin{array}{r}
 0001 \quad 0011 \\
 0001 \quad 0010 \\
 \hline
 0000 \quad 0001
 \end{array}$$

①
 MOV A, #17h
 SUBB A, #04h
 MOV R₂, A
 CLR A
 RLC A
 MOV R₄, A
 END

→ ALP to perform 16 bit Addition stored in R₃ & R₄
 with RAM location 44h & 45h. Put result in R₄ MSB, 31h
 Middle byte of 32h LSB.
 30h



MOV A, R₄
 ADDC A, R_{45h}

MOV 32h, A

MOV A, R₃

ADDC A, 44h

MOV 31h, A

CLR A

ADDC A, #00h

MOV 30h, A

END

→ Multiply data from 22h by gram location 15h, put result
in 19h LSB, 18h MSB

Mov A, 22h

Mov B, 15h

NWL AB

Mov 19h, A

Mov 18h, B

END 4

→ Square the contents of R5, result into R0 MSB

R1 LSB

Divide the data in RAM 3Eh by number 12h, put
quotient in R4, remainder R5

Mov A, R5 | Mov B, R5

Ator NWL A~~B~~

Mov R0, B

Mov R1, A

END 1

Mov A, 3Eh

Mov B, #12h

Div AB

Mov R4, d

Mov R5, B

END

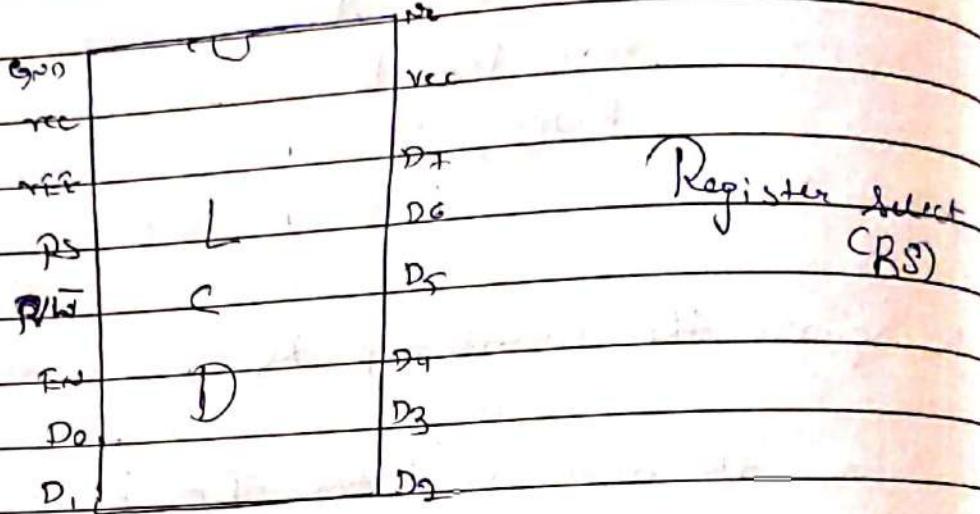
Lab - 5

14/2/2020

(Interfacing LCD with 8051)

16x2 LCD Module is very common type

→ 16 characters, 2 rows
pixel dimension is 5×7 or 5×8 dot



LCD	Signal Name	Port line
Pin No.		
1	GND	GND
2	V _{cc}	V _{cc}
3	V _{ref} (LCD contrast)	P ₉ (10 th pin)
4	RS Line	P _{2.7}
5	R/S Line	P _{2.5}
6	EN Line	P _{2.6}
7	Data D ₀	NC
8	Data D ₁	NC
9	Data D ₂	NC
10	Data D ₃	NC
11	Data D ₄	P _{2.0}
12	Data D ₅	P _{2.1}
13	Data D ₆	P _{2.2}
14	Data D ₇	P _{2.3}
15	V _{cc}	21V

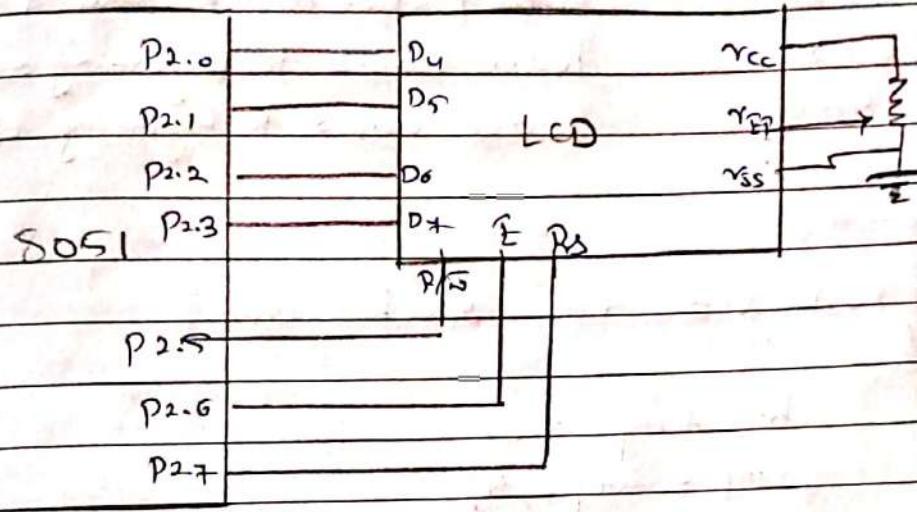
LCD Interfacing

P.S = 1 for sending command to LCD

P.S = 0 for sending data to LCD

R/W = 1 for reading from LCD

R/W = 0 for writing to LCD



→ EP - enable pin

4.7kΩ

Enable puller

→ LCD Commands

Command

0x01

0x02

0x04

0x06

0x07

0x09

Instructions

clear display screen

return home

decrement cursor (shift cursor left)

increment cursor (shift cursor right)

shift display left

Display off, cursor off

0x02

4 bit function set 2 lines 4 5x7 dots

0x28

Ponc

X

X

0x80

0x00

0x0F

Display ON, cursor n blinking

0x28

4 bit function set 2 lines 4 5x7 dots

0x80

Force cursor to beginning of 1st line

0x00

Force cursor to beginning of 2nd line

mid lcd cmd - wr (char cmd)

char temp = cmd;

temp = temp < , 4;

temp = temp | 0x40;

P2 = temp;

delay(450);

temp = temp + 0x0F;

P2 = temp;

delay(100);

temp = cmd;

temp = temp + 0x0F;

temp = temp | 0x40;

P2 = temp;

delay(450);

temp = temp + 0x0F;

P2 = temp;

delay(100);

void lcd_data_wr (char data)

```

    {
        char temp = data;
        temp = temp >> 4;
        temp = temp | 0x00;
        P2 = temp;
        delay (450);
        temp = temp & 0x8F;
        P2 = temp;
        delay (100);
        temp = data;
        temp = temp & 0x0F;
        temp = temp | 0x00;
        P2 = temp;
        delay (450);
        temp = temp & 0x8F;
        P2 = temp;
        delay (100);
    }

```

main()

```

    lcd_cnd_wr (0x06);
    lcd_cnd_wr (0x28);
    lcd_cnd_wr (0x0F);
    lcd_cnd_wr (0x01);
    lcd_cnd_wr (0x80);
    char str = "EscN";
    for (int i=0; i<strlen(str); i++)
        lcd_data_wr (str[i]);
}

```

Movec Syntax

Movec A, @pc + A
Movec A, @A + Dptr

|| ALP to copy contents of external code memory 0040H to IP register.

CLR A / Mov #00H
Mov Dptr, #0040H
Movec A, @Dptr + A
Mov CF A / Mov 0A8H, A
END

|| Copy the internal code byte at 0300H to external ^{RAM} memory 0300H.

CLR A
Mov Dptr, #0300H
Movec A, @Dptr + @x. // gets code byte
Movx @Dptr, A // written into ^{External RAM} RAM.
END.

|| ALP to copy program bytes 000H to 0102H to internal ^{External RAM from program} ROM to the location 20H to 28H

CLR A
Mov Dptr, #0000H
Movec A, @A + Dptr
Mov 090H, A
CLR A

Mov D PTR, #010H
 Movc A, @A+D PTR
 Mov 021H, A
 CLR A

Mov D PTR, #010H
 Movc A, @A+D PTR
 Mov 022H, A

Q3

Mov D PTR, #0100H

Mov A, #000H

Movc A, @A+D PTR

Mov 00H, A

Mov A, #01H

Movc A, @A+D PTR

Mov 21H, A

Mov A, #02H

Movc A, @A+D PTR

Mov 22H, A

PUSH & POP

push addn

pop addn

→ push 30H



increment after push data
Pop data + the decrement

Content of 30H will be

stored in top's location

→ pop 10H

top's data will be stored

in address location

of 10H.

Swap contents R₆ & R₇ using push & pop

```
push R6 (yy)  
push R7 (yy)  
pop R6 (yy)  
pop R7 (yy)  
END.
```

3/1/2020

|| Logical Instructions

Bit level logical Instructions

for	ANL C, #b	Mov c, b
ADD	ANL C, #b/b	Mov b, c
operation		

OR	ORL C, b	CPL C	complement
operation	ORL C/b	CPL b	

CLR C	reset	SETB b	sets the value to 1
CLR b			

e.g.: Write an Alp to clear bit 3 of RAM location 30H without affecting other bits

Mov 20H, 30H

CLR 03H // bit addressable

Mov 30H, 20H

END

SETB C } set the value to 1
SETB b }

// ALP to Move bit 6 of R₀ to bit 3 of Part a

Mov 26h, R₆

Mov C, 06H

Mov 83H, C

END

→ // Sequence of instructions to clear register R₃ of bank 1

CPL D3,

Mov R₃, #00H

SETB 0D0, 3h } selected the Bank 1
CLR 0D0, 4h }
Mov R₃, #00H

5/2/2020

Rotate Instructions

RR A

Rotate Right

RRC A

Rotate Right with carry

RLC A

RL A

Date: / /
Ex:- 80h

RL

1000 0000

0000 0000

~~00h~~ 0h

RR

1000 0000

0000 0000

40h

c⁼⁰ 1000 0000

(RLC)

1000010000

00h

(RRC) c⁼⁰

1000 0000

00100 0000

RLC \rightarrow will double the value (\times by 2)

RRC \rightarrow will half the value (\div by 2)

To move R0 & R, as 16 bit register & rotate \rightarrow place to left
bit 7 of R0 become bit 0 of R, & bit 7 of R, because
bit 0 of R0



Mov A, R0

RLC \rightarrow

Mov R0, A

Mov A, R,

RLC \rightarrow

Mov ~~A~~, R, A

CLR A

RLC A

ORL 00h, A

Mov ~~00h~~, R

Mov 00h, C

Mov R0, 20h

→ // ALP to rotate DPTR 1 place to the right
DPTR (16 bit)

Mov A, DPL (82h)

RRC A

Mov DPL, A

Mov A, DPH (83h)

RRC A

Mov DPH, A

Mov 20h, DP~~H~~L

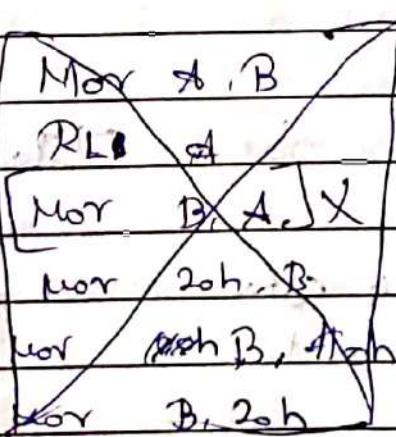
Mov 07h, C

Mov DP~~H~~, 20h

→ // ALP shifts B register content 1 place to the left &
bit on zero

0100 0010
 ^ P A

1000 0100



CLR C

Mov A, B

RLC A

Mov B, A

END

→ // ALP swaps every even numbered bit of R3 in bank 0 with every odd numbered bit to its left.

Mov A, R₃

RR A

ANL A, #55h

Mov 30h, A [odd bit → even bit → 30h]

Mov A, R₃

R₂ A (even bit → odd bit)

ANL A, #AAh

OPL A, 30h

Mov R₃, A

END

9/2/2020

10h 0001 0000

99h 0000 1001

109h 1010 1001

A 9

+ 1 Add 6 circuit

109

μ₀° should be within 00-99 → for B.Decimal

HALP to add R₃, R₄, store result in 30h & 31h.
(LSB) (MSB)

Numbers are in BCD format.

Mov A, R₃

ADD A, R₄

adjust spcc

DA → decimal

DA A

Mov 30h, A

CLD A

Addc A, #00h

Mov 31h, A

CLR A

RLC A

II ALP to add Numbers found in 30h, 31h, 32h, store result in R₃ (LSB) R₄ (Mbyte), R₅ (MSB)

Mov A, 30h	Mov A, 30h	Mov A, 30h
ADD A, 31h	Add A, 31h	Add A, 31h, Mov R ₃ , A
Mov R ₃ , A	Addc A, 32h	CLR A
CLD A	Mov R ₃ , A	RLC A
ADDC A, H00h	CLD A	Mov R ₃ (Corrig.)
Mov R ₄ , A	RLC A	ADDE
Mov A, 32h	Mov R ₄ , A	Mov A, 32h
ADD A, R ₂	END	ADDC R ₃ , R ₃
Mov R ₁ , A		Mov R ₃ , A (LSR)
Mov A, R ₄		CLD A
ADDC A, H00h		RLC A
Mov R ₄ , A		Adc R ₃ , A
END		Mov R ₅ , A
		END

→ 16 bit × 8 bit multiplication.

$$R_1, R_0 \rightarrow 16 \text{ bit No.}$$

$$R_2 \rightarrow 8 \text{ bit No.}$$

Store in 30h, 31h, 32h

10/2/2020

16 bit x 8 bit multiplication.

Mov A; R₀

Mov OF0h, R₁

MUL AB

Mov A3h, A → LSB.

Mov 31h, B

Mov A, R₀

Mov OF0h, R₁

MUL AB

[Mov 32h, B → HSB]

Mov

ADD A, 31h

Mov 31h, A → Middle byte

ABSCRMBCPRA CLR A

ADDA A, OF0h

ADDC A, OF0h // A + B + carry

Mov 32h, A // HSB

END.

? Subtract byte in the External Ram 02ch from the internal Ram 19h, put result into external memory location 0001 HSB

Mov A, 02ch

CLR C

SUBB A, 19h

Mov DPTR, #02ch

Movx A, @DPTR // AL

Mov DPTR, #0000

R₀

Mov @DPTR, A

Mov A, 19h

ENCL DPTR

SUBB A, R₀

Mov DPTR, #0000

Mov @DPTR, A

CLP \rightarrow

RLC \rightarrow

Inc Dptr

Mov @Dptr, A

END

Jump

Bit

JC radd

(Jump on carry)

JNC radd

(Jump on no carry)

JB b, radd

If b=1 then jump

JNB b, radd

If b=0, then jump

JBc b, radd

If b=0, then jump, but before going
it will clear the bit =0

Flags are not

affected by memory device

Affected.

Byte

CJNE A, radd, radd

Compare A with radd, if not equal, then go

CJNE A, #n, radd

Compare A with n, if not equal = Jump

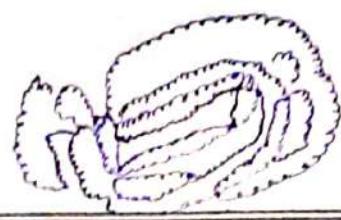
CJNE Rr, #n, radd

CJNE @Rp, A, radd

A > 30h, C=0

A < 30h, C=1

//Alg to put a random no° in R3 & increment it until
it equals a no° in b



Mov R₃, #11h

bK, INC R₃

CJNE R₃, #0E1h, blk

// ALP to put a random no. in R₃ & decrement it until it becomes
11h.

Mov R₃, #11h

bK DEC R₃

CJNE R₃, #0E1h, blk

// ALP to count no. of 1's in numbers in Register B, put the
Count in R₅

Mov R₅, #00h

Mov B, #50h

Mov A, B

blk; RLC A

JNC Next

INC R₅

Next DJNZ R₂, blk

END

// ALP Count no. of zeroes in R₃ & put in R₅

Mov R₅, #00h

Mov R₂, #8h

Mov A, R₃

blk, RLC A

JC Next

INC R₅

Next DJNZ R₂, blk

END

II ALP to exchange bank 0 content with bank 2.

II ALP to find biggest no. among R1 R2 R3 R4 & put it in R6

Bank 0

R0

R1

1

R2

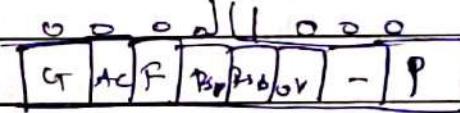
R3

One register to count the values
R0 - base address

Mov 0Dah, #0sh // select bank 1

Set bit 0Dah // 0Dah = address of PSW

clr 0Dah.4



Mov 0Dah, #0sh

bank 1

Mov R3, #3

PSW \rightarrow 0Dah

Mov R0, #0oh

Mov A, @R0

II ALG-6

R0 - 16

inc R0 // R0 - 01

R1 - 5

Mov 30h, @R0 // 30h - 5

R2 - 13

CJNR A, 30h, L1

R3 - 2

SJMP L2

L1: JNC L2

CJNR,

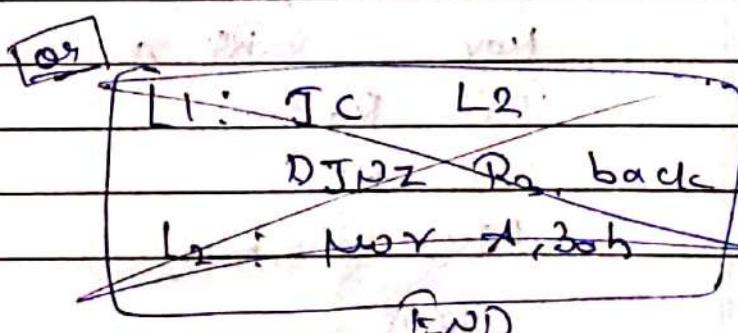
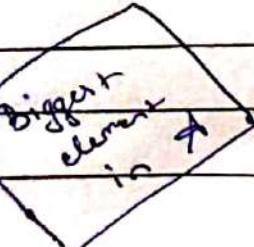
Mov A, 30h

b7=5 \therefore C=0

L2: DJNZ R3, back

get L2 \therefore C=1

END



// ALP to find smaller no. (among array)
of 20 element stored in memory location

not
needed

Mov 0Doh, H0h

Mov R₃, #13h (#19)

(20 elements) \Rightarrow 19 compare

Mov R₀, #40h

Mov A, @R₀

back Inc R₀

Mov 30h, @R₀

CJNP A, 30h; L1

SJMP L2

L1: JC L2

Mov A, 30h

L2: DJNZ R₃, back

END

L1: ~~JNC L2~~

L1: JNC L2

~~Mov 0Doh, H0h~~

L2: ~~Mov A, 30h~~

~~END~~

// exchange bank 0 content with bank 3

Mov 0Doh, #~~08h~~ //bank 1 (using bank 0 &
^{08h} ⁰⁰⁰¹¹⁰⁰⁰)

Mov R₀, #00h //bank 0 starting address (use diff bank)

Mov R₁, #10h //bank 2 starting address

Mov R₃, #08h // 8 iteration

back: Mov A, @R₀

Inc A, @R₁

Mov @R₀, A

Inc R₀

Inc R₁

DJNZ R₃, back

END

1) ALP to check whether No. in R5 is even or odd.
 if even store in FFh, else store 00h.

Mov A, R5
 Mov B, #02h
 Div A/B
~~JNC~~

A → quotient B → remainder

2) Mov A, R5
 RRC A // LSB is in Carry
 JC L1
 Mov P0, #FFh
 SJMP last (unconditional jump)
 L2: Mov P0, #00h
 last:
 END

↑
 SJMP → short
 LJMP → long
 AJMP → absolute