**Design of Low Power VLSI Architectures for Machine Learning Based Wearable Healthcare Devices**

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**Abstract**

According to the World Health Organization (WHO), cardiovascular diseases cause approximately 17.9 million fatalities yearly, which is estimated to be 31% of the global mortality rate. An electrocardiogram (ECG) is a biosignal that provides information on the patient’s heart’s electrical activity. ECG enables the diagnosis of various cardiac abnormalities, from acute coronary syndrome to cardiac arrhythmias. Therefore, ECG monitoring in daily life is necessary for early diagnosis of heart disease. With the increasing population and inadequate healthcare infrastructure, medical support has become paramount in today’s scenario. Due to fewer medical professionals available than required, it has become challenging to administer expert help to people living in urban and rural areas. Hardware and software developments have led to the development of machine learning-enabled wearable healthcare devices, such as smartwatches and chest patches, which can continuously monitor cardiac functioning easily. The wearable devices provide critical alerts for events that require prompt medical attention or hospitalization, making them highly efficient and practical. Further, these devices can continuously track vital health parameters and send this information to healthcare providers. This reduces the number of yearly visits to a medical professional.

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A conventional wearable device has three primary modules. The first module is the sensors and analog front, responsible for acquiring the ECG signals and converting them to digital samples. The second module consists of an ECG co-processor, incorporating a feature extraction block and a machine learning-based classifier responsible for ECG signal analysis and classification of cardiovascular diseases. The final module comprises data compression and transmitter blocks, which transmit ECG data and the classifier output to the cloud servers. In wearable devices, battery life is critical because most devices monitor ECG continuously. Further, these devices should be small and easy to use. Therefore, area and power-optimized algorithms and their VLSI architectures are required for continuous monitoring of ECG on wearable devices. Thus, we present optimized ECG signal processing algorithms and their low-power and resource-efficient VLSI architectures for cardiovascular disease detection, such as cardiac arrhythmia and myocardial infarction, for wearable devices.

Initially, an optimized ECG feature extraction algorithm and its low-power hardware implementation, which can extract all the critical features of ECG is proposed. Further, this design is integrated with different classifiers, employing neural networks and if-else-based methods to detect different types of cardiac arrhythmia and severity stages of Myocardial Infarction (MI). In this thesis, we propose three different VLSI architectures for classifying five types of arrhythmia beats, predicting ventricular arrhythmia and detecting severity stages of MI. Further, a low-power ECG data compression architecture, enabling the wearable healthcare device to compress a large amount of ECG data, is also developed. The proposed algorithms and their VLSI architectures for ECG signal processing operate at low power and require minimal hardware resources, making them suitable candidates for wearable healthcare devices.