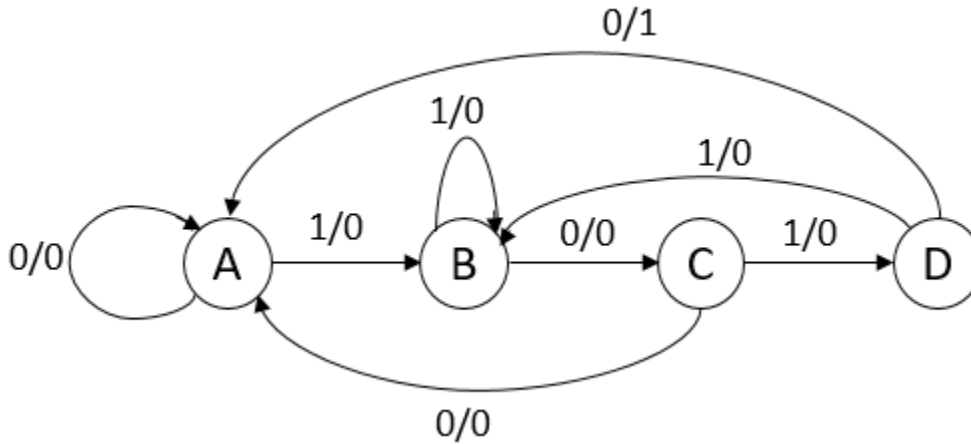


# SEQUENCE DETECTOR



## DESIGN:

```
module seq_detector_1010(input bit clk, rst_n, x, output z);
```

```
    parameter A = 4'h1;
```

```
    parameter B = 4'h2;
```

```
    parameter C = 4'h3;
```

```
    parameter D = 4'h4;
```

```
    bit [3:0] state, next_state;
```

```
    always @(posedge clk or negedge rst_n) begin
```

```
        if(!rst_n) begin
```

```
            state <= A;
```

```
        end
```

```
        else state <= next_state;
```

```
    end
```

```
    always @(state or x) begin
```

```
        case(state)
```

```

A: begin
    if(x == 0) next_state = A;
    else      next_state = B;
end
B: begin
    if(x == 0) next_state = C;
    else      next_state = B;
end
C: begin
    if(x == 0) next_state = A;
    else      next_state = D;
end
D: begin
    if(x == 0) next_state = A;
    else      next_state = B;
end
default: next_state = A;
endcase
end

assign z = (state == D) && (x == 0)? 1:0;
Endmodule

```

### **TESTBENCH:**

```

module TB;
    reg clk, rst_n, x;
    wire z;

```

```
seq_detector_1010 sd(clk, rst_n, x, z);
```

```
initial clk = 0;
```

```
always #2 clk = ~clk;
```

```
initial begin
```

```
    x = 0;
```

```
    #1 rst_n = 0;
```

```
    #2 rst_n = 1;
```

```
    #3 x = 1;
```

```
    #4 x = 1;
```

```
    #4 x = 0;
```

```
    #4 x = 1;
```

```
    #4 x = 0;
```

```
    #4 x = 1;
```

```
    #4 x = 0;
```

```
    #4 x = 1;
```

```
    #4 x = 1;
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```
    #4 x = 1;
```

```
    #4 x = 0;
```

```
    #4 x = 1;
```

```
    #4 x = 0;
```

```
    #4 x = 1;
```

```
    #4 x = 0;
```

```
    #10;
```

```
    $finish;
```

```
end
```

```
initial begin
    // Dump waves
    $dumpfile("dump.vcd");
    $dumpvars(0);
end
Endmodule
```

### **OUTPUT WAVEFORMS(SCREEN SHOTS):**

how to use X Bing Videos X iverilog - Se X Icarus Verilog X Sequence X mealy fsm - X Mealy Sequ X EDA Edit code - X

https://edaplayground.com

EDA playground Run Save New support email is support@edaplayground.com. Playgrounds Profile

EPWave

From: 0ns To: 72ns

Get Signals Radix 100%

0 10 20 30 40 50 60 70

clk

rst\_n

x

z

A[3:0]

B[3:0]

C[3:0]

D[3:0]

clk

next\_state[3:0]

rst\_n

state[3:0]

x

z

Note: To revert to EPWave opening in a new browser window, set that option on your user page.

19:18

04-03-2024