TRAFFIC LIGHT CONTROLLER

DESIGN:

MAIN MODULE:

```
`timescale 1ns/1ps
module main(
  output MR,
  output MY,
  output MG,
  output SR,
  output SY,
  output SG,
  input reset,
  input C,
  input Clk
  );
timer part 1 (TS, TL, ST, CIK);
fsm part2(MR, MY, MG, SR, SY, SG, ST, TS, TL, C, reset, Clk);
endmodule
```

TIMER MODULE:

```
'timescale 1ns/1ps
module timer(
  output TS,
  output TL,
  input ST,
  input Clk
  );
integer value;

assign TS (value>=4);
assign TL (value>=14);
```

```
always@(posedge ST or posedge Clk)
begin
if(ST=1)begin
value=0;
end
else begin
value=value+1;
end
end
endmodule
```

FSM MODULE:

```
'timescale 1ns/1ps
module fsm(
  output MR,
  output MY,
  output MG,
  output SR,
  output SY,
  output SG,
  output ST,
  input TS,
  input TL,
     input C,
  input reset,

  input Clk
  );
reg [6:1] state;
reg ST;
parameter mainroadgreen= 6'b001100;
parameter mainroadyellow=6'b010100;
```

```
parameter sideroadgreen= 6'b100001;
parameter sideroadyellow=6'b100010;
assign MR state[6];
assign MY = state[5];
assign MG=state[4];
assign SR state[3];
assign SY = state[2];
assign SG = state[1];
initial begin state mainroadgreen; ST = 0; end
always @(posedge Clk)
        begin
                if (reset)
                begin state mainroadgreen; ST = 1; end
                else
                begin
                        ST=0;
                                case (state)
                                mainroadgreen:
                                if (TL & C) begin state mainroadyellow; ST = 1; end
                                mainroadyellow:
                                if (TS) begin state = sideroadgreen; ST = 1; end
                                sideroadgreen:
                                if (TLC) begin state = sideroadyellow; ST = 1; end
                                sideroadyellow:
                                if (TS) begin state = mainroadgreen; ST = 1; end
                                endcase
                        end
        end
endmodule
```

TEST BENCH:

```
`timescale 1ns/1ps
module fsm_test;
        reg TS;     reg TL;      reg C; reg reset;      reg Clk;
        wire MR;  wire MY;   wire MG;    wire SR;   wire SY;   wire SG;
        wire ST;
        fsm uut (
        .MR(MR), .MY(MY), .MG(MG), .SR(SR), .SY(SY), .SG(SG), .ST(ST),
        .TS(TS), .TL(TL), .C(C),
        .reset(reset), .Clk(Clk)
        );
        initial begin
                TS=0;TL=0;C=0;reset = 1;
                Clk = 0;
                #100; TS=0;TL=1;C=1;reset=0;
                #100; TS-0;TL=0;C=0;reset-1;
                #100; TS-1;TL-1;C=0;reset=0;
                #100;
                end
                always
                begin
                #100
                Clk=~Clk;
                end
        endmodule
```

output waveforms: