

Logisim main of HALF ADDER

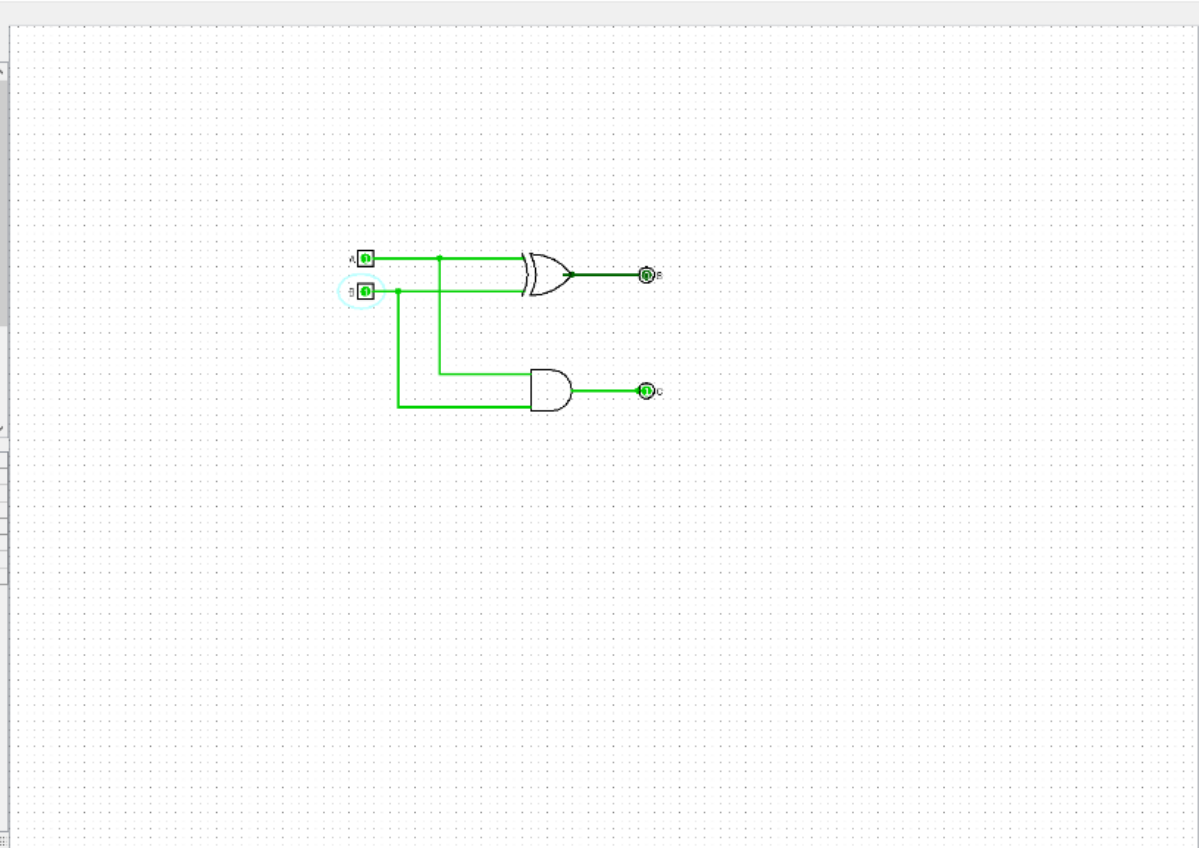
File Edit Project Simulate Window Help



HALF ADDER

- main
 - Wiring
 - Gates
 - NOT Gate
 - Buffer
 - AND Gate
 - OR Gate
 - NAND Gate
 - NOR Gate
 - XOR Gate
 - XNOR Gate
 - Odd Parity
 - Even Parity
 - Controlled Buffer
 - Controlled Inverter
 - Flowers
 - Arithmetic
 - D Flip-Flop
 - T Flip-Flop
 - J-K Flip-Flop
 - S-R Flip-Flop
 - Register
 - Counter
 - Shift Register
 - Random Generator
 - RAM

	Pin
Facing	East
Output?	No
Data Bits	1
Three-state?	No
Pull Behavior	Unchanged
Label	B
Label Location	West
Label Font	SansSerif Plain 12



100%