

Expt No: 01

Date:

LOGIC GATES

Aim:- To Verify the functionality of logic gates (NAND, NOR, NOT, AND, OR, XOR, XNOR).

Apparatus:- IC7400-1, IC7402-1, IC7404-1, IC7408-1, IC7432-1, IC7486-1, IC74266-1, Breadboard-1, Digital Multimeter-1, Regulated Power Supply (RPS)-1, (0-30V), LED's and connecting wires as per required.

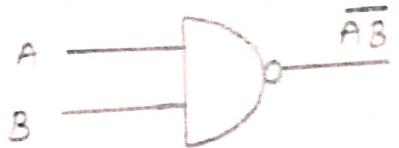
Theory:- In digital circuits, two discrete voltages are recognized as logic 1 and logic 0 known as high and low level logics respectively. A logic gate is a device that acts as a building block for digital circuits.

Procedure:-

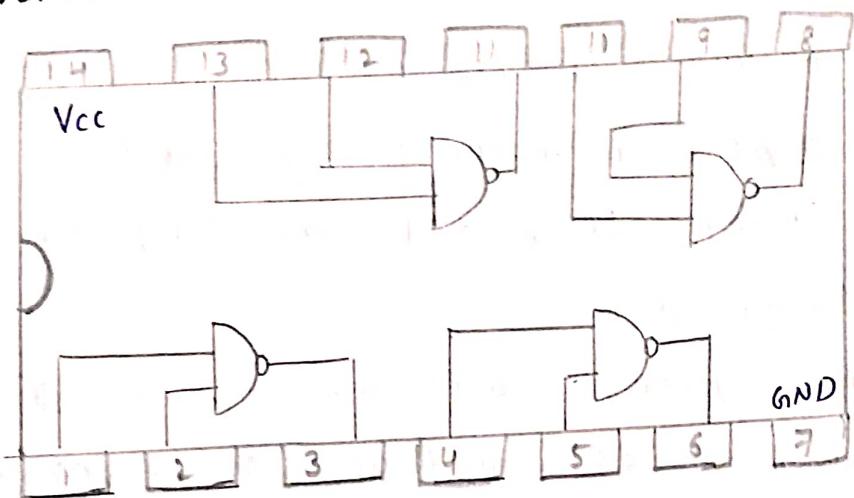
- 1) Check whether all the components are working properly or not.
- 2) Connect the circuit as per the circuit diagram.
- 3) Check all loose connections. If any, fix them.
- 4) Switch on the power supply.
- 5) Start giving all possible inputs from RPS to the circuit.
- 6) Notice down the corresponding output values for the given inputs.

NAND :-

Logic Symbol :-



Internal Architecture :-



Truth Table :-

A	B	\bar{AB}
0	0	1
0	1	1
1	0	1
1	1	0

Practical Values

Inputs		Outputs
A	B	\bar{AB}
OFF	OFF	ON
OFF	ON	ON
ON	OFF	ON
ON	ON	OFF

7) Compare the theoretical and practical values and conclude the functionality of the respective logic gate.

NAND GATE :-

The NAND gate is a logic gate whose functionality is output 0, if all inputs are 1, otherwise output is 1. The NAND gate is a AND gate followed by a bubble or a NOT gate. Its IC is 7400.

It contains 4 NAND gates and a Vcc pin for input voltage and another for ground.

It is one of the universal logic gates.

Pin :-

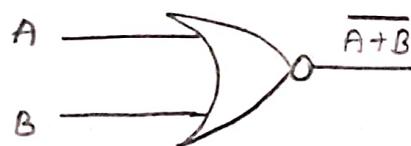
Input	Output
1, 2	3
4, 5	6
10, 9	8
13, 12	11

Vcc (14)

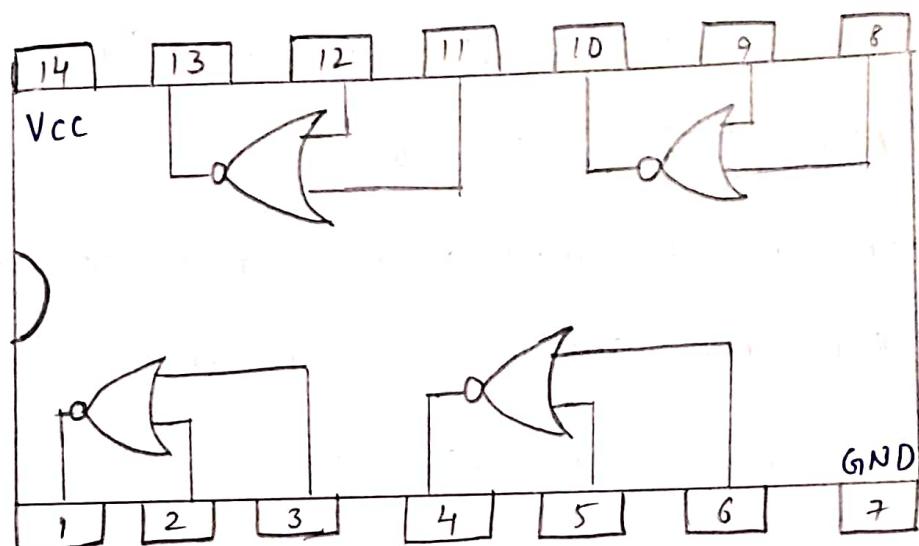
GND (7)

NOR

Logic Symbol :-



Internal Architecture :-



Truth Table:-

A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Practical values:-

Inputs		Output
A	B	$\overline{A+B}$
OFF	OFF	ON
OFF	ON	OFF
ON	OFF	OFF
ON	ON	OFF

NOR GATE :-

The NOR gate is a logic gate whose functionality is output '1' if all inputs are '1', otherwise output is '0'.

The NOR gate is an OR gate followed by a bubble or a NOT gate.

It's IC is 7402.

It contains 4 NOR gates and a Vcc pin for input voltage and another for ground.

It is one of the universal logic gates.

PINS :-

Input	Output
2, 3	1
5, 6	4
8, 9	10
11, 12	13

Vcc (14)

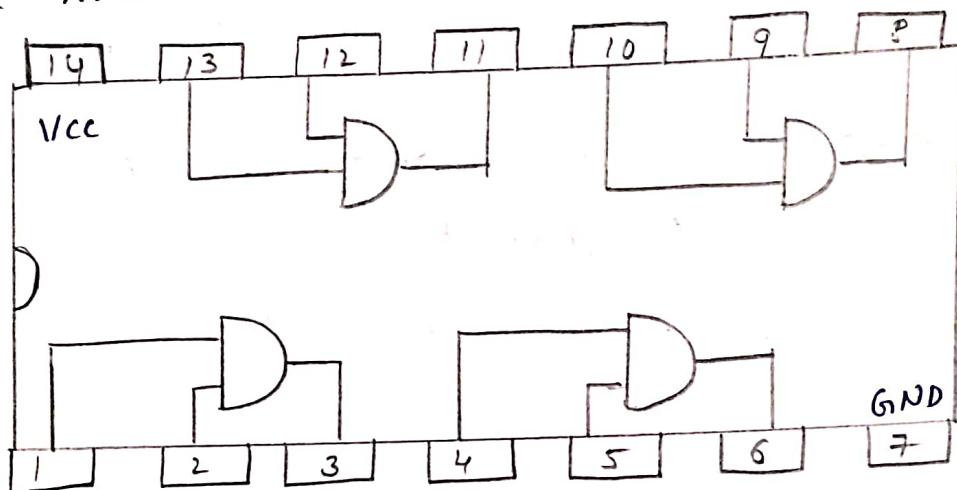
GND (7)

AND :-

Logic symbol :-



Internal Architecture :-



Truth Table :-

A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1

Practical values :-

Inputs		Output
A	B	\bar{AB}
OFF	OFF	OFF
OFF	ON	OFF
ON	OFF	OFF
ON	ON	ON

AND gate:-

The AND gate is a logic gate whose functionality is output $\neq 1$, if all inputs are 1 , Otherwise output is 0 .

It's IC is 7408.

It is a 2-input AND gate

It contains 4 AND gates and one for Vcc pin for input voltage and another for ground.

Pins :-

14 - Vcc

7 - GND

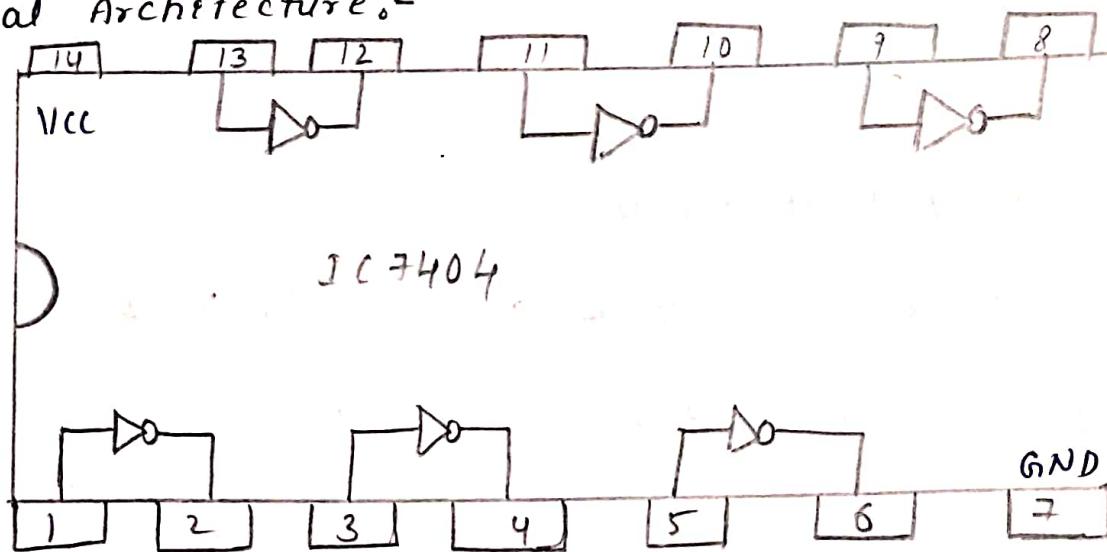
Input	Output
1,2	3
4,5	6
12,13	11
9,10	8

NOT gate:-

Logic Symbols:-



Internal Architecture:-



Truth Table:-

A	\bar{A}
0	1
1	0

Practical values:-

Input	Output
A	NOT A
OFF	ON
ON	OFF

NOT gate:-

The NOT gate negates the values of data or signal in its input. If the input is 0 then the output is 1. If the input is 1, then the output is '0'. It is also known as Inverter.

It's IC is 7404. It contains 6 not gates and a pin for input voltage Vcc and another pin for ground.

Pins:-

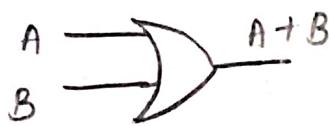
Inputs	Outputs
1	2
3	4
5	6
9	8
11	10
13	12

14 - Vcc

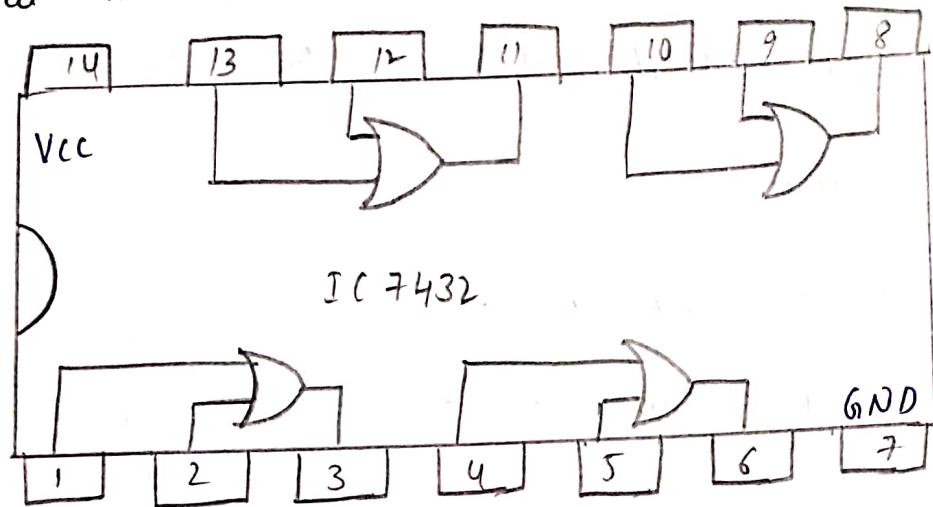
7 - GND

OR :-

Logic Symbol :-



Internal Architecture :-



Practical values :-

Truth Table :-

A	B	$A + B$
0	0	0
0	1	1
1	0	1
1	1	1

Inputs		Output
A	B	$A + B$
OFF	OFF	OFF
OFF	ON	ON
ON	OFF	ON
ON	ON	ON

OR gate :-

The OR gate is a logic gate whose functionality is such that its output is '0', if all inputs are '0', otherwise the output is '1'. Its IC no is 7432.

It is a 2-input OR gate.

It contains 4 OR gates and Vcc pin for input voltage and another for ground.

Pins :-

Inputs	Outputs
1, 2	3
4, 5	6
12, 13	11
9, 10	8

14 - Vcc

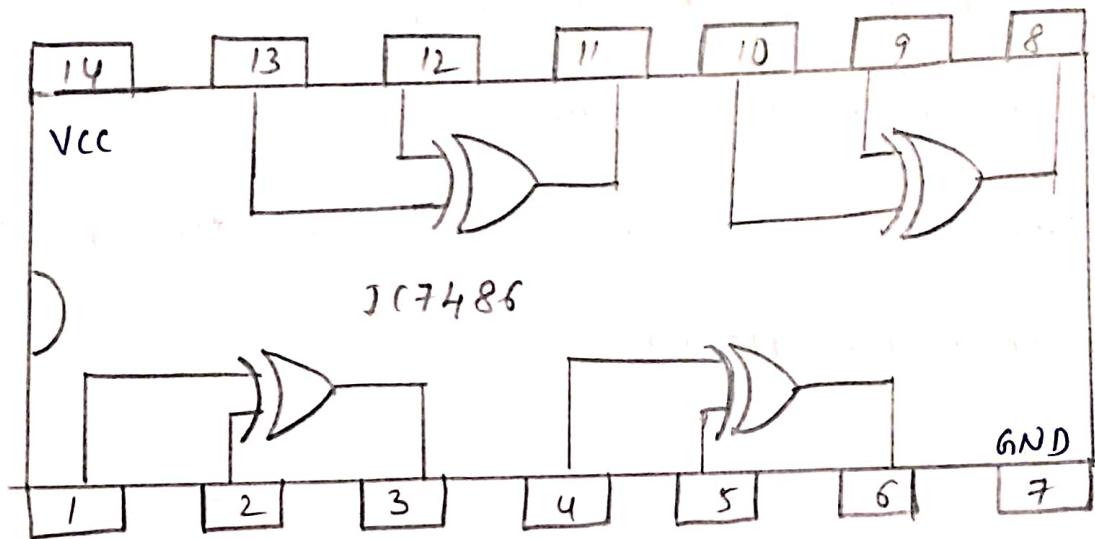
7 - GND

XOR :-

Logic symbol:-



Internal Architecture:-



Truth Table:-

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Practical Values:-

Inputs		Output
A	B	$A \oplus B$
OFF	OFF	OFF
OFF	ON	ON
ON	OFF	ON
ON	ON	OFF

XOR gate :-

'XOR' is an abbreviation for 'Exclusive OR'. The simplest XOR gate is a two-input digital circuit that outputs a logical "1" if the two inputs values differ. i.e., its output is a logical '1', if either of its inputs are 1, but not at the same time (exclusively).

It contains 4 XOR gates in a single IC7486.

Prns :-

Inputs Outputs

1, 2 3

4, 5 6

9, 10 8

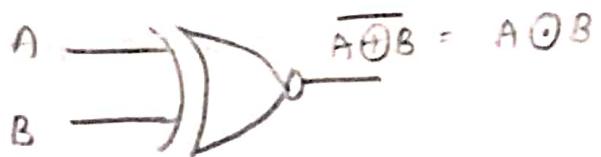
12, 13 11

14 - Vcc

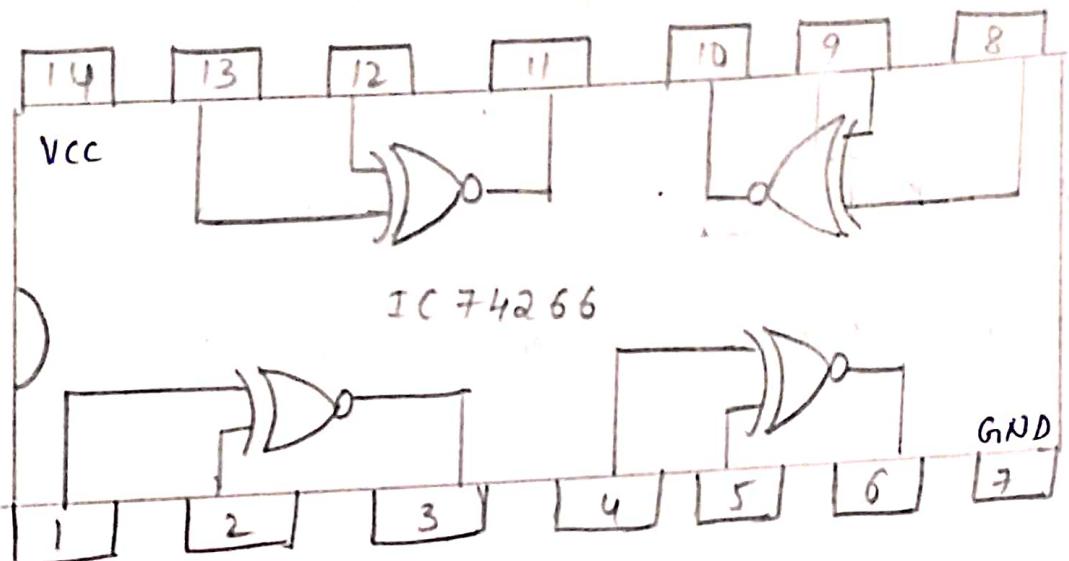
7 - GND

~~NOR :-~~

Logic Symbol :-



Internal Architecture :-



Practical values :-

Truth Table

A	B	$A \odot B$
0	0	1
0	1	0
1	0	0
1	1	1

Inputs		Output
A	B	$\overline{A \oplus B}$
OFF	OFF	ON
OFF	ON	OFF
ON	OFF	OFF
ON	ON	ON

XNOR gate :-

The XNOR (Exclusive NOR) is a combination XOR gate followed by an inverter.
Its output is '1' if the both the inputs are the same and '0' otherwise.

Sometimes referred it as an Equivalence gate, the gate's output requires both inputs to be the same to produce a high output.

There are 4 XNOR gates on a single IC 74266.

PinS :-

Inputs	Outputs
1, 2	3
5, 6	4
8, 9	10
12, 13	11

Vcc - 74

GND - 7

Precautions:-

- 1) We have to wear shoes before coming to Lab.
- 2) Handle the IC's and RPS with utmost care.
- 3) Make sure that all components are connected properly.
- 4) Avoid loose connections, if any then fix them before conducting the experiment.

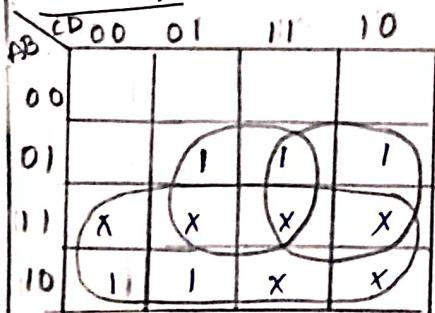
Result:-

thus designed and verified the functionality of logic gates with theoretical values.

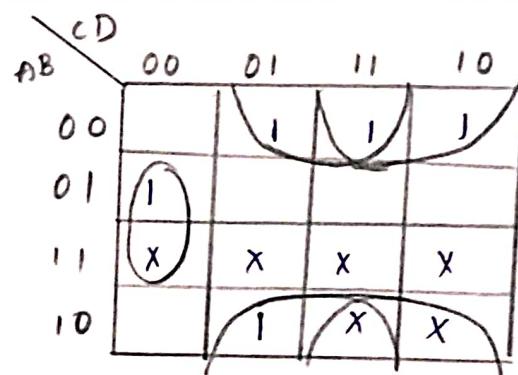
Truth table of BCD to Excess-3 Converter :-

BCD				Excess-3				
A	B	C	D	W	X	Y	Z	
0	0	0	0	0	0	1	1	
0	0	0	1	0	1	0	0	
0	0	1	0	0	1	0	1	
0	0	1	1	0	1	1	0	
0	1	0	0	0	1	1	1	
0	1	0	1	1	0	0	0	
0	1	1	0	1	0	0	1	
0	1	1	1	1	0	1	0	
1	0	0	0	1	0	1	1	
1	0	0	1	1	1	0	0	
1	0	1	0	x	x	x	x	
1	0	1	1	x	x	x	x	
1	1	0	0	x	x	x	x	
1	1	0	1	x	x	x	x	
1	1	1	0	x	x	x	x	
1	1	1	1	x	x	x	x	

K-maps :-



$$W = A + BC + BD$$



$$X = B'C + B'D + BC'D'$$

EXP NO: 2

Date:

BCD to Excess-3 Converter

Aim:- To design and verify the functionality of BCD to Excess-3 converter circuit.

Apparatus:- IC7400-2, Regulated Power Supply (RPS) - $\frac{10-30V}{-1}$, Breadboard-1, Connecting wires (as per required), IC7404-1, IC7410-1.

Theory:-

BCD : Binary Coded Decimal in which every digit is individual converted into binary format.

$$\text{Ex: } (985)_{10} = (1001\ 1000\ 0101)_{BCD}$$
$$= (1100\ 1011\ 1000)_{Ex-3}$$

⇒ For converting BCD having four bits (A,B,C,D) into Excess-3 having four bits (w,x,y,z) we need to construct the truth table.

⇒ After the truth table is constructed find the Boolean expression for the output bits i.e., (w,x,y,z) by using k-map.

⇒ Then we get

$$w = A + BD + BC = A + B(C + D)$$

$$x = \bar{B}C + \bar{B}D + B\bar{C}\bar{D}$$

$$= \bar{B}(C + D) + B(C\bar{C} + \bar{D})$$

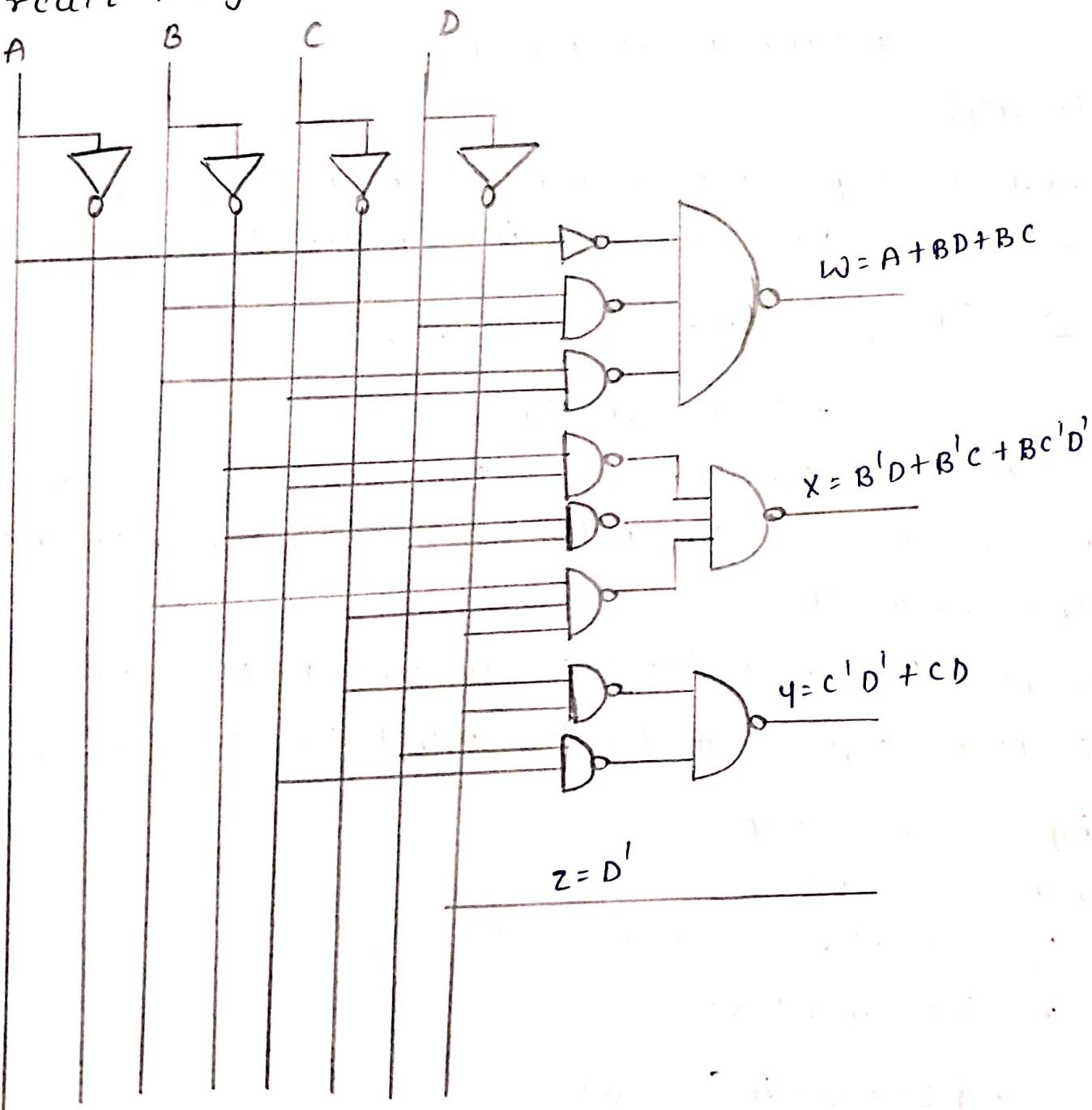
	CD	00	01	11	10
AB	00	1			
	01	1	1		
	11	X	X	X	X
	10	1	X	X	X

$$y = CD + C'D'$$

AB	CD	00	01	11	10
	00	1			1
	01	1			1
	11	X	X	X	X
	10	1		X	X

$$z = D'$$

* Circuit diagram of BCD to Excess-3 Converter -



$$y = CD + \bar{C}\bar{D} = CD + (\bar{C} + D)$$

$$z = \bar{D}$$

Now let's construct the circuit using the above inputs and outputs using NAND gates.

Procedure:-

- 1) Check whether all components are working properly or not.
- 2) Connect the circuit as per circuit diagram and avoid loose connections.
- 3) Start giving all possible input from RPS to the circuit.
- 4) Record corresponding output values for all the input from LED.
- 5) Verify the outputs with theoretical readings.

Precautions:-

- 1) We should wear shoes before coming to lab.
- 2) Handle the IC's and RPS with utmost care.
- 3) Make sure that all components are connected properly.
- 4) Avoid loose connections, if any then fix them before conducting the experiment.

Result:-

thus designed and verified the functionality of BCD to Excess-3 Converter.

Practical Readings:-

BCD

Excess - 3

A	B	C	D	W	X	Y	Z
OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
OFF	OFF	OFF	ON	OFF	ON	OFF	OFF
OFF	OFF	ON	OFF	OFF	ON	OFF	ON
OFF	OFF	ON	ON	OFF	ON	ON	OFF
OFF	ON	OFF	OFF	OFF	ON	ON	ON
OFF	ON	OFF	ON	ON	OFF	OFF	OFF
OFF	ON	ON	OFF	ON	OFF	OFF	ON
OFF	ON	ON	ON	ON	OFF	ON	OFF
OFF	OFF	OFF	OFF	ON	OFF	ON	ON
ON	OFF	OFF	ON	ON	ON	OFF	OFF
ON	OFF	ON	OFF	X	X	X	X
ON	OFF	ON	ON	X	X	X	X
ON	ON	OFF	OFF	X	X	X	X
ON	ON	OFF	ON	X	X	X	X
ON	ON	ON	OFF	X	X	X	X
ON	ON	ON	ON	X	X	X	X

Truth table for a 2-bit magnitude Comparator :-

Inputs				Outputs		
A_1	A_0	B_1	B_0	$A > B$	$A = B$	$A < B$
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

EXP NO: 3

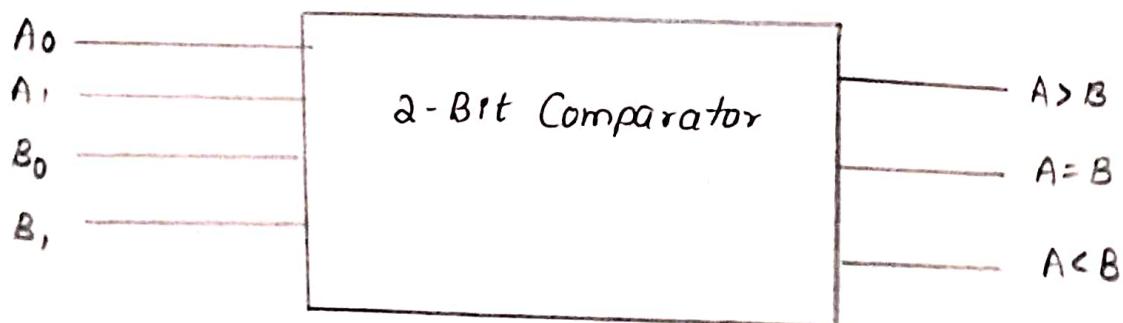
Date:

Magnitude Comparator

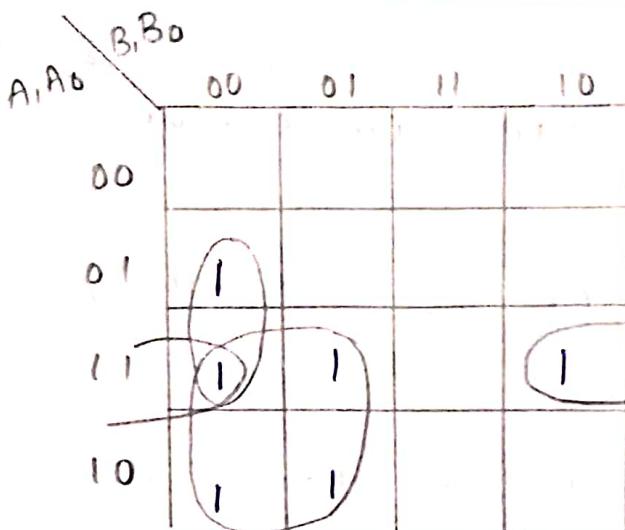
Aim:- To design and verify the functionality of magnitude comparator using theoretical values.

Apparatus :- IC7400-1, RPS (0-30V) - 1, Digital Multimeter - 1, connecting wires (as per required), Breadboard - 1.

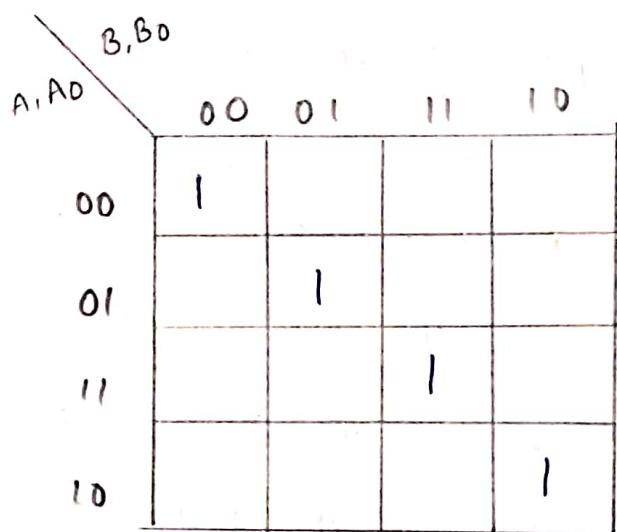
Theory :- A magnitude digital comparator is a combinational circuit that compares two digital or binary numbers in order to find out whether one binary number is equals, less than, or greater than the other number. We logically design a circuit for which we will have two inputs one for A and the other for B and have three output terminals, one for $A > B$ condition, one for $A = B$ condition, and one for $A < B$ condition.



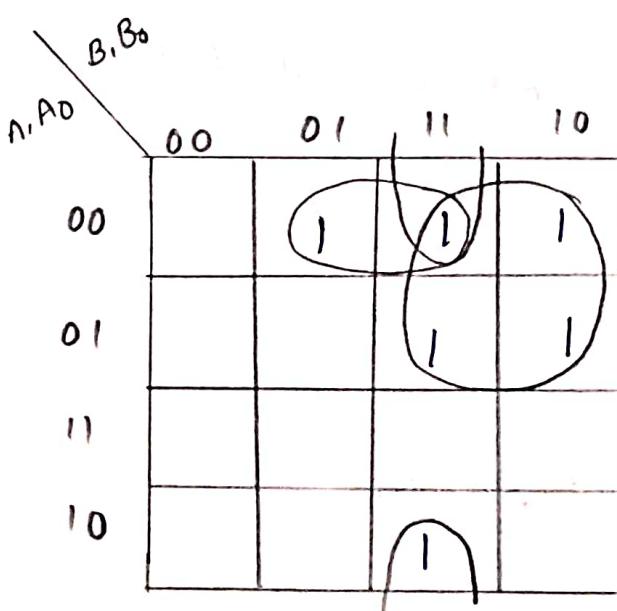
k-maps



$$A > B = A_1 B_1' + A_0 B_1' B_0' + A_1 A_0 B_0'$$



$$A = B = \overline{A_1 \oplus B_1} \cdot \overline{A_0 \oplus B_0}$$



$$A < B = A_1' B_1 + A_1' A_0' B_0 + A_0' B_1 B_0$$

A 2-bit magnitude comparator used to compare two binary numbers each of two bits is called a 2-bit Magnitude Comparator. It consists of four inputs and three outputs to generate less than, equal to, and greater than between two binary numbers.

From the k-maps logical expressions for each output can be expressed as follows.

$$\begin{aligned} A > B &= A_1 B_1' + A_0 B_1' B_0' + A_1 A_0 B_0' \\ &= A_1 B_1' + A_0 B_0' (B_1' + A_1) \\ &= A_1 B_1' + A_0 B_0' (\overline{A_1 \oplus B_1}) \end{aligned}$$

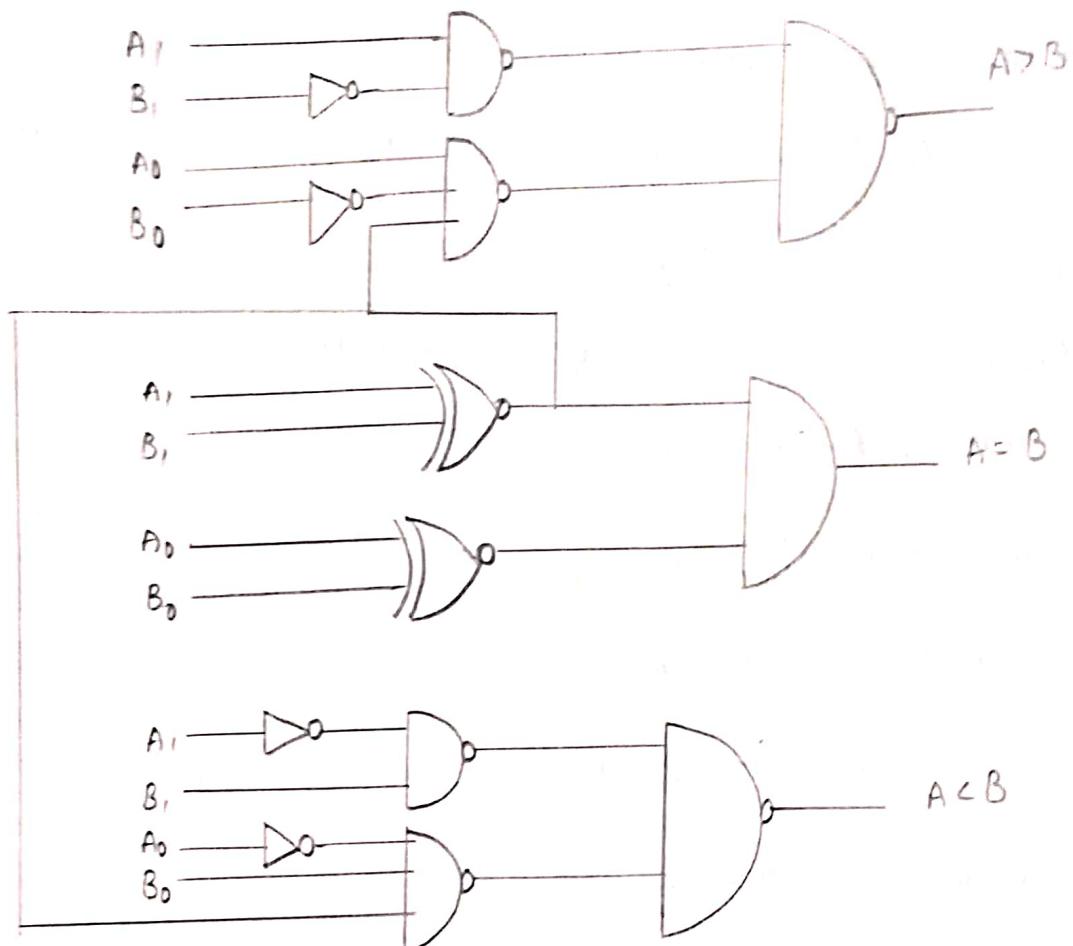
$$\begin{aligned} A = B &= A_1' A_0' B_1' B_0' + A_1' A_0 B_1' B_0 + A_1 A_0 B_1 B_0 + A_1 A_0' B_1 B_0' \\ &= A_1' B_1' (A_0' B_0' + A_0 B_0) + A_1 B_1 (A_0 B_0 + A_0' B_0') \\ &= (A_1' B_1' + A_1 B_1) (A_0' B_0' + A_0 B_0) \\ &= (A_1 \ominus B_1) \cdot (A_0 \ominus B_0) \end{aligned}$$

$$\begin{aligned} A < B &= A_1' B_1 + A_1' A_0' B_0 + A_1' B_1 B_0 \\ &= A_1' B_1 + A_0' B_0 (\overline{A_1 \oplus B_1}) \end{aligned}$$

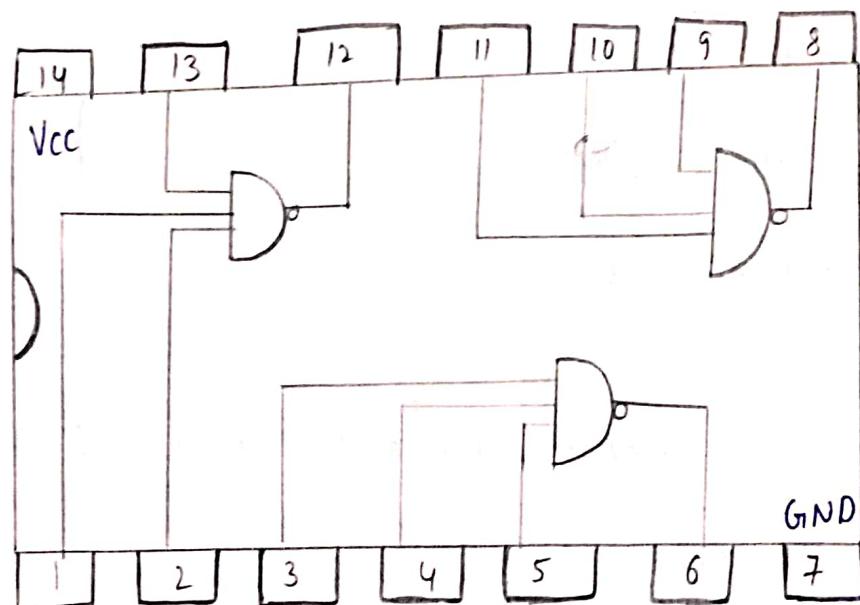
Procedure :-

- 1) Firstly check whether all the components are working properly or not.
- 2) Construct the circuit as per the above Boolean expressions, without any loose connections.

circuit diagram of 2-bit magnitude Comparator:-



Internal Architecture of 3 input NAND gate (IC7410):-



- 3) Try all combinations of inputs to A₀A₁, B₀B₁, from RPS with or and sr record the corresponding outputs.
- 4) Compare the experimental and theoretical values & calculate the functionality of circuit.
- 5) Give various combinations of inputs and verify the truth table.

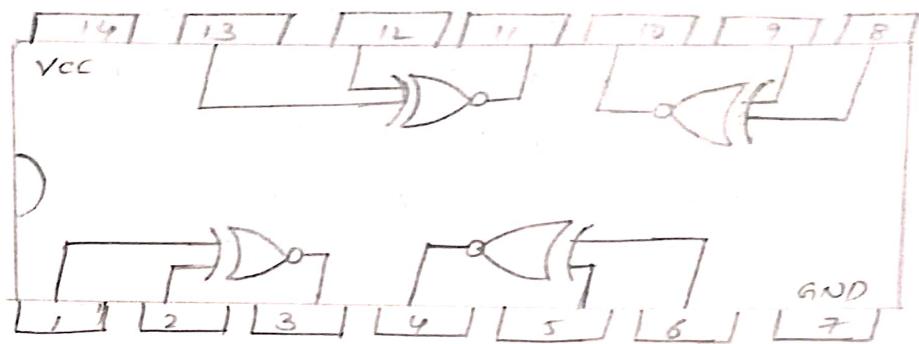
Applications:-

1. Comparators are used in central processing units (CPUs)
2. and microcontrollers (MCUs)
3. Used in password verification and biometric applications.
4. Comparators are also used for process controllers and for servo motor control.

Precautions:-

- ⇒ Check if any loose connections, then fix the connections properly.
- ⇒ All the connections should made neat and tight.
- ⇒ Never touch live and knacked wires.

Internal Architecture of a 2 input XNOR Gate (74266) :-



Practical Readings :-

Input				Output		
A,	A ₀	B,	B ₀	A>B	A = B	A < B
OFF	OFF	OFF	OFF	OFF	ON	OFF
OFF	OFF	OFF	ON	OFF	OFF	ON
OFF	OFF	ON	OFF	OFF	OFF	ON
OFF	OFF	ON	ON	OFF	OFF	ON
OFF	ON	OFF	OFF	ON	OFF	OFF
OFF	ON	OFF	ON	OFF	ON	OFF
OFF	ON	ON	OFF	OFF	OFF	ON
OFF	ON	ON	ON	OFF	OFF	ON
ON	OFF	OFF	OFF	ON	OFF	OFF
ON	OFF	OFF	ON	ON	OFF	OFF
ON	OFF	ON	OFF	OFF	ON	OFF
ON	OFF	ON	ON	OFF	OFF	ON
ON	ON	OFF	OFF	ON	OFF	OFF
ON	ON	ON	OFF	ON	OFF	OFF
ON	ON	ON	ON	OFF	ON	OFF

Result:-

thus designed and verified the functionality
of 2-bit magnitude comparator.

Truth Table for Full Adder

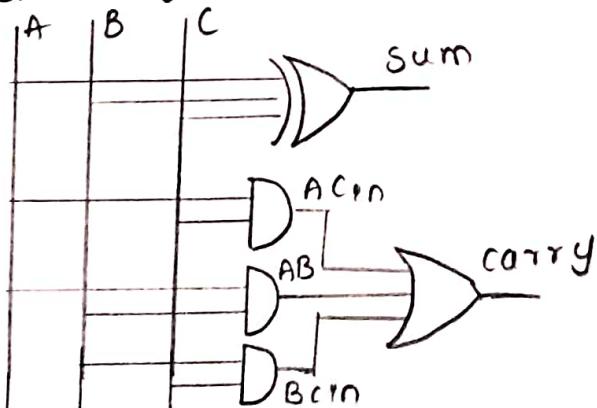
Input			Output	
A	B	C _{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-maps :-

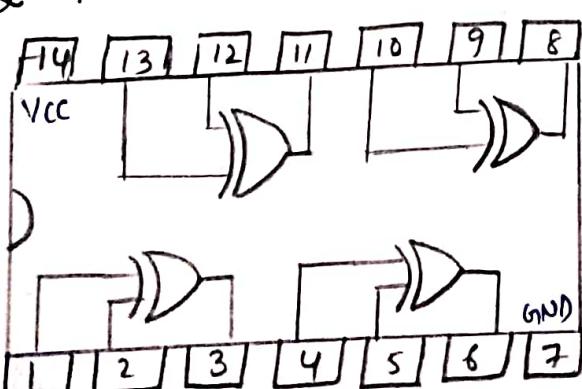
		BC _{in}	00	01	11	10
		A	0			
			0	1		
0	0	0				
1	1	1	1	1	0	1

$$S = A \oplus B \oplus C_{in}$$

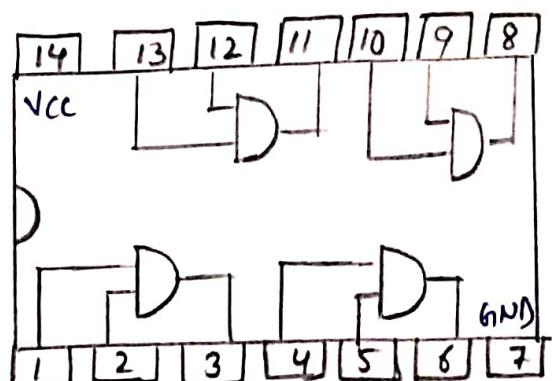
circuit diagram :-



2 input XOR gate



2 input AND gate



EXP NO: 04

Date:

Full Adder & Full Subtractor

Aim:- To design and verify the functionality of full Adder and Full Subtractor.

Apparatus:- Regulated Power Supply (RPS)-1, Breadboard -1, connecting wires (as per required), IC 7408-1, IC 7408-2, IC 7404 -1, IC 7432 -1.

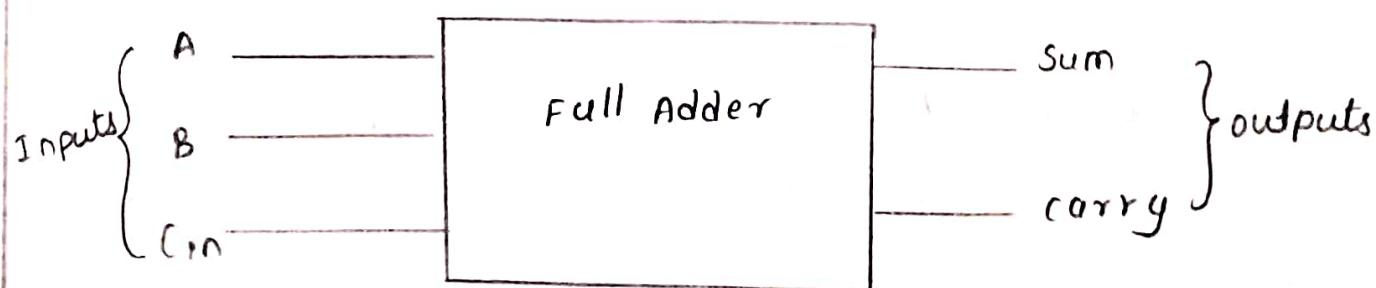
Theory:-

Full Adder:-

The adder that adds three inputs and produces two outputs. The first two inputs are A and B, and the third input is carry input C_{in} . The output carry is designed as (C_{out}) and normal output as sum (S).

$$Sum = A \oplus B \oplus C_{in}$$

$$Carry = AC_{in} + AB + BC_{in}$$



Truth Table of Full Subtractor :-

Inputs			Outputs	
A	B	B_0	Diff	B_1
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

K-maps :-

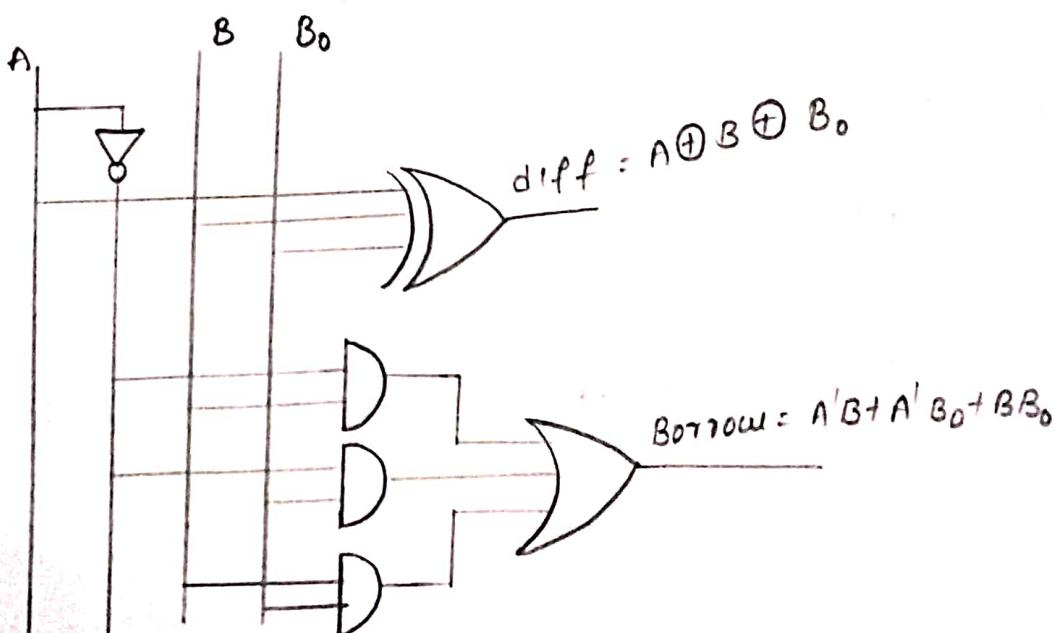
		BB ₀	00	01	11	10
		A	0	1		
		B	0	1		
0						
1			1	1		

		BB ₀	00	01	11	10
		A	0	1	1	1
		B	0		1	
0						
1						

$$B_1 = A'B + A'B_0 + BB_0$$

$$\text{Diff} = A \oplus B \oplus B_0$$

Circuit diagram of Full Subtractor :-

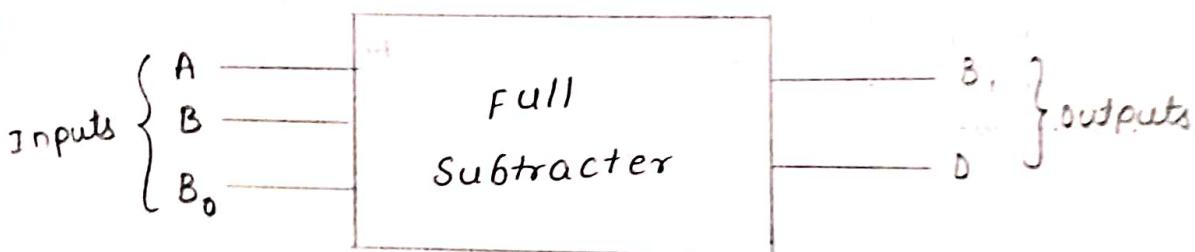


Full Subtractor:-

A combinational circuit that performs subtraction of two bits taking into the account of borrow of previous bit. The circuit has three inputs A, B and B_0 and two outputs D and B_1 . D represents the difference and B_1 represents the borrow output.

$$\text{Diff} = A \oplus B \oplus B_0$$

$$\text{Borrow } (B_1) = A'B + A'B_0 + BB_0$$



Procedure:-

1. Connect the circuit as per the logical expressions of full adder and full subtractor.
2. Start giving all the possible combination of inputs.
3. Supply the power to the circuit through RPS.
4. Record the corresponding output values of all the inputs of respective circuits.
5. Compare the practical values to the theoretical values.

Practical Readings :-

Full Adder :-

Input			Output	
A	B	C _{in}	Sum	Carry
OFF	OFF	OFF	OFF	OFF
OFF	OFF	ON	ON	OFF
OFF	ON	OFF	ON	OFF
OFF	ON	ON	OFF	ON
ON	OFF	OFF	ON	OFF
ON	OFF	ON	OFF	ON
ON	ON	OFF	OFF	ON
ON	ON	ON	ON	ON

Full Subtractor :-

Input			Output	
A	B	B ₀	Diff	Borrow
OFF	OFF	OFF	OFF	OFF
OFF	OFF	ON	ON	ON
OFF	ON	OFF	ON	ON
OFF	ON	ON	OFF	ON
ON	OFF	OFF	ON	OFF
ON	OFF	ON	OFF	OFF
ON	ON	OFF	OFF	OFF
ON	ON	ON	ON	ON

Precautions:-

- 1) Check whether all the components are working properly or not.
- 2) Make sure that all the connections are fixed without any loose connections.
- 3) Handle the components with utmost care.

Result:-

thus designed and verified the functionality of full adder and full subtractor.

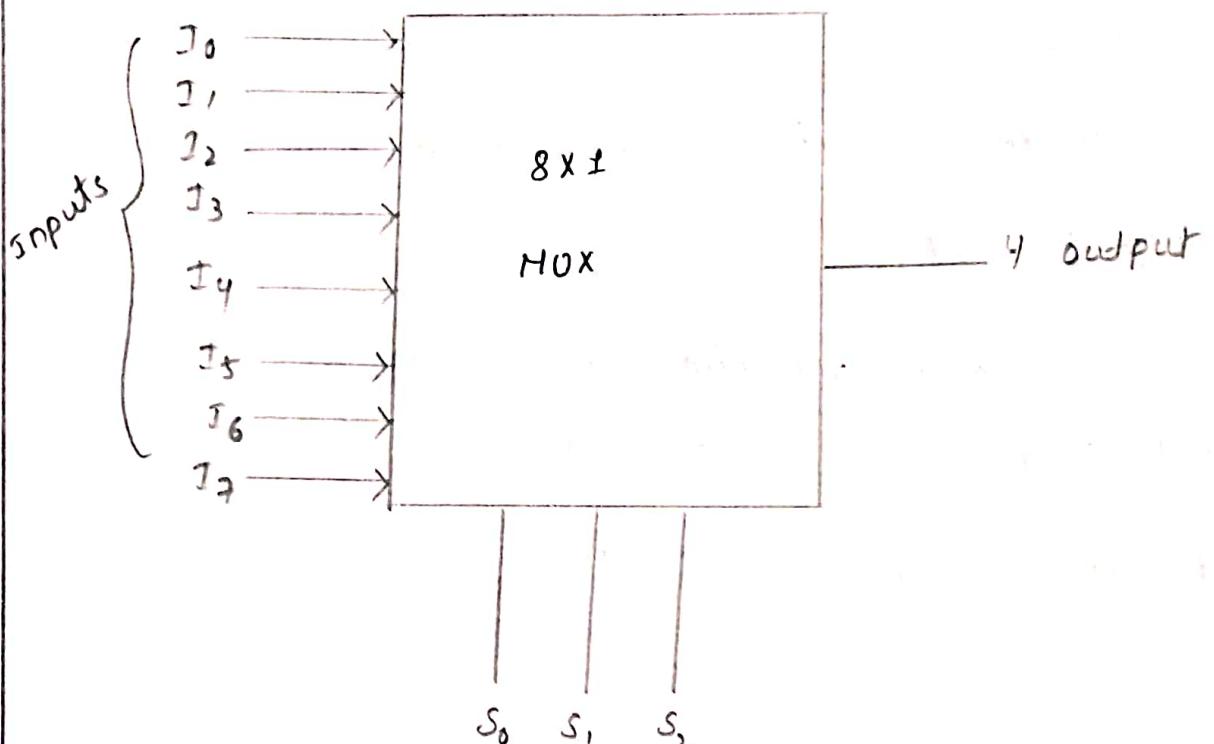


Fig: 8x1 Multiplexer

Truth table for 8x1 Multiplexer:-

Inputs			Output
S_2	S_1	S_0	I_4
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

EXP NO: 5a

Date:

8x1 MULTIPLEXER

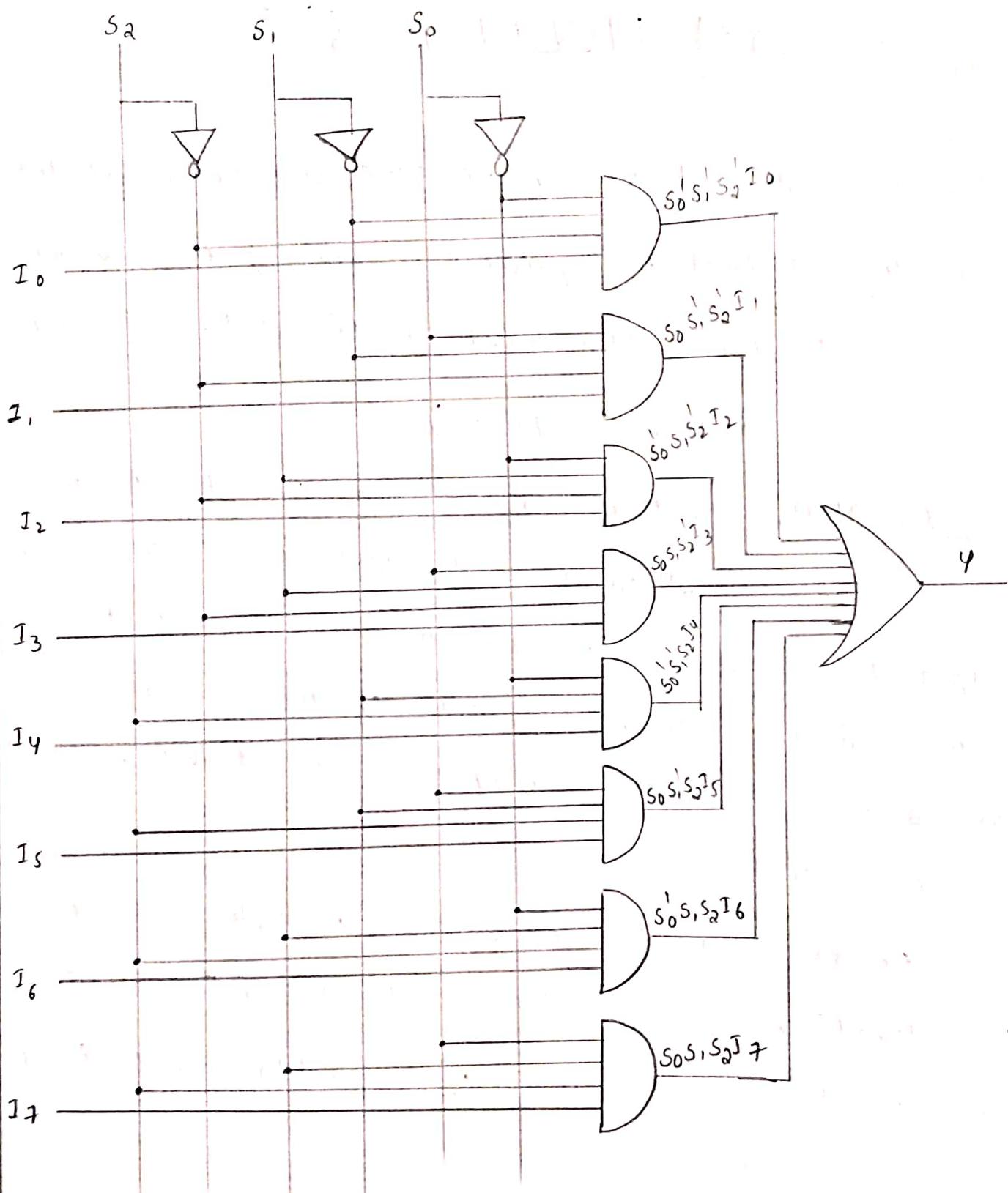
Aim: To design and verify the functionality of 8x1 MUX.

Apparatus:- IC 7421 - 1, Regulated Power Supply (RPS) - (0-30V) - 1, Digital Multimeter - 1, Breadboard - 1, Connecting wires (as per required).

Theory :- Multiplexer is a combinational circuit which takes n inputs and selects one of them for output. In the process it uses ' n ' selection lines. For each combination of binary values of the selection lines, for each a corresponding input is selected to be processed for the output.

An 8x1 MUX is nothing but a multiplexer with $8 = 2^3$ inputs, 3 selection lines and one output. Let the inputs be $I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7$ and its output be Y . Selection lines are S_0, S_1, S_2 .

$$Y = S_0' S_1' S_2' I_0 + S_0 S_1' S_2' I_1 + S_2' S_0 S_1 I_2 + S_2 S_0' S_1 I_3 + S_2 S_1' S_0 I_4 + S_2 S_1 S_0 I_5 + S_2 S_1 S_0' I_6 + S_2 S_1 S_0 I_7$$

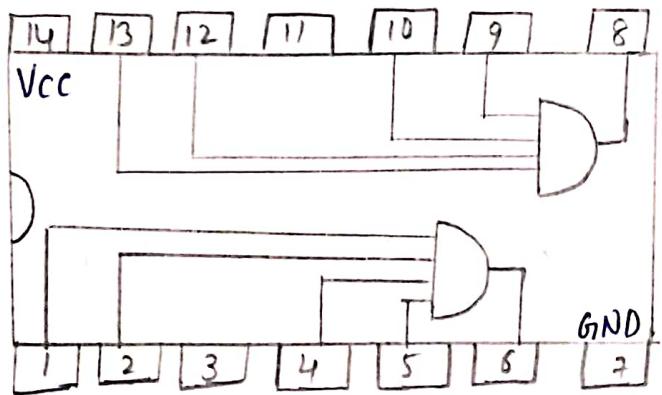


Circuit diagram of 8x1 Multiplexer

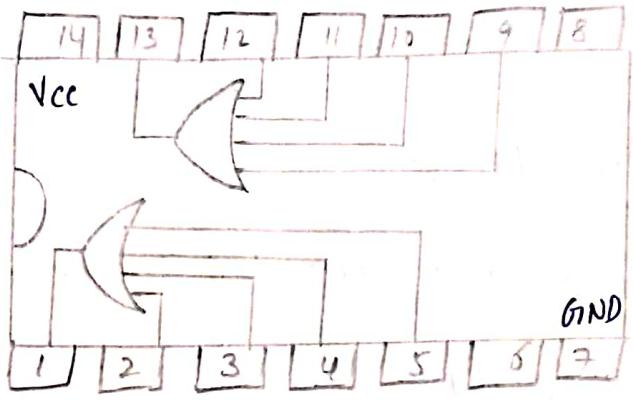
Procedure:-

- 1) check all the loose connections if any and fix them properly.
- 2) Connect the circuit as per the logical expressions.
- 3) Construct the truth table for 8x1 MUX for various inputs.
- 4) Try all combinations of inputs to s_0 , s_1 , and s_2 from RPS and read corresponding outputs using multiplexer.
- 5) Compare the theoretical and experimental values and concludes the functionality of the multiplexer.

4 Input AND gate (IC7421)



4 Input OR gate (40728)



Practical values for the 8x1 MUX :-

Inputs			Output
S _a	S ₁	S ₀	Y
OFF	OFF	OFF	I ₀
OFF	OFF	ON	I ₁
OFF	ON	OFF	I ₂
OFF	ON	ON	I ₃
ON	OFF	OFF	I ₄
ON	OFF	ON	I ₅
ON	ON	OFF	I ₆
ON	ON	ON	I ₇

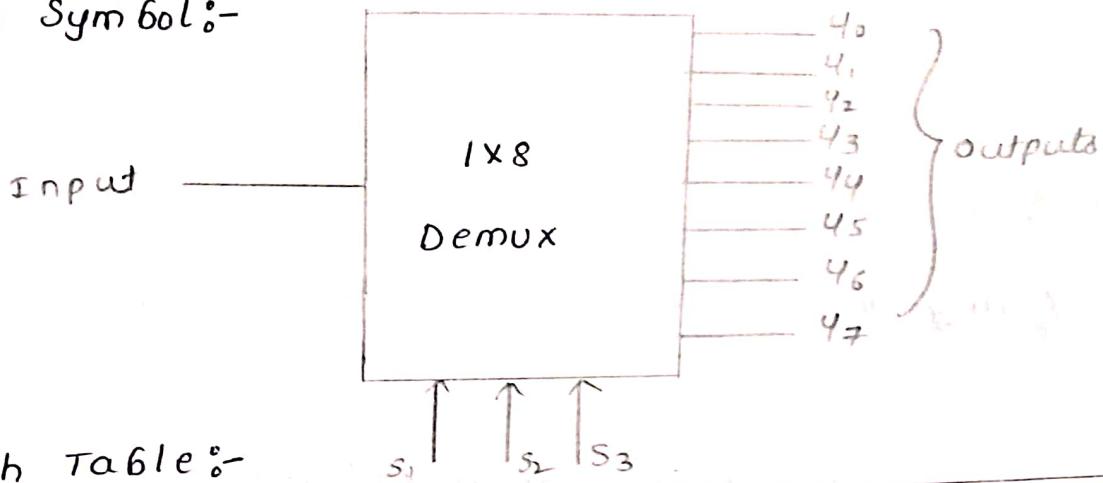
Precautions:-

- 1) check if any loose connections , then fix them properly.
- 2) All connections should be neat and tight.
- 3) Never touch live and naked wires.

Result:-

thus designed and verified the functionality
of 8x1 Multiplexer.

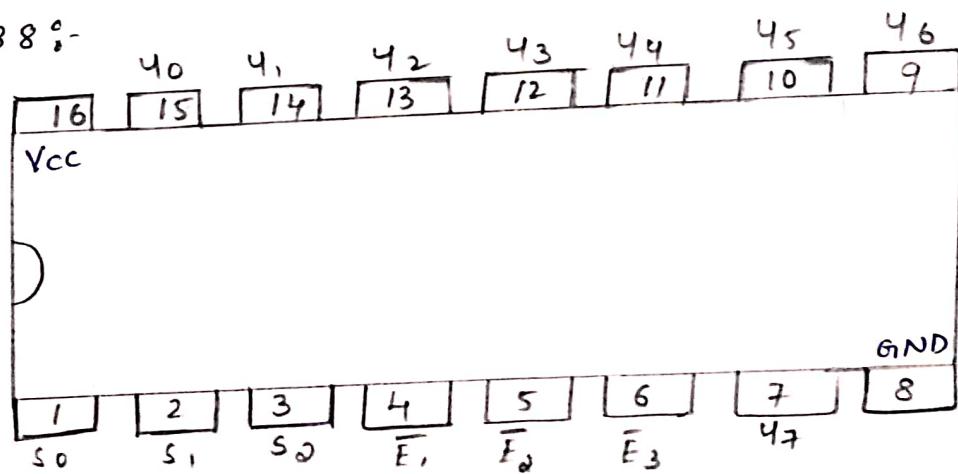
Logic Symbol:-



Truth Table:-

Input			Output							
\$s_0\$	\$s_1\$	\$s_2\$	\$y_0\$	\$y_1\$	\$y_2\$	\$y_3\$	\$y_4\$	\$y_5\$	\$y_6\$	\$y_7\$
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

IC 74138:-



Experiment No: 5b

Date:

1x8 DEMULTIPLEXER

Aim:- To design and verify the functionality of 1x8

Demultiplexer using theoretical values.

Apparatus:- IC 74138-1, RPS (5V) -1, Digital multimeter -1,

Bread board-1, Connecting wires (as per required).

Theory:- Demultiplexer is a combinational circuit which

takes one input and connects to one of the outputs using 'n' selection lines.

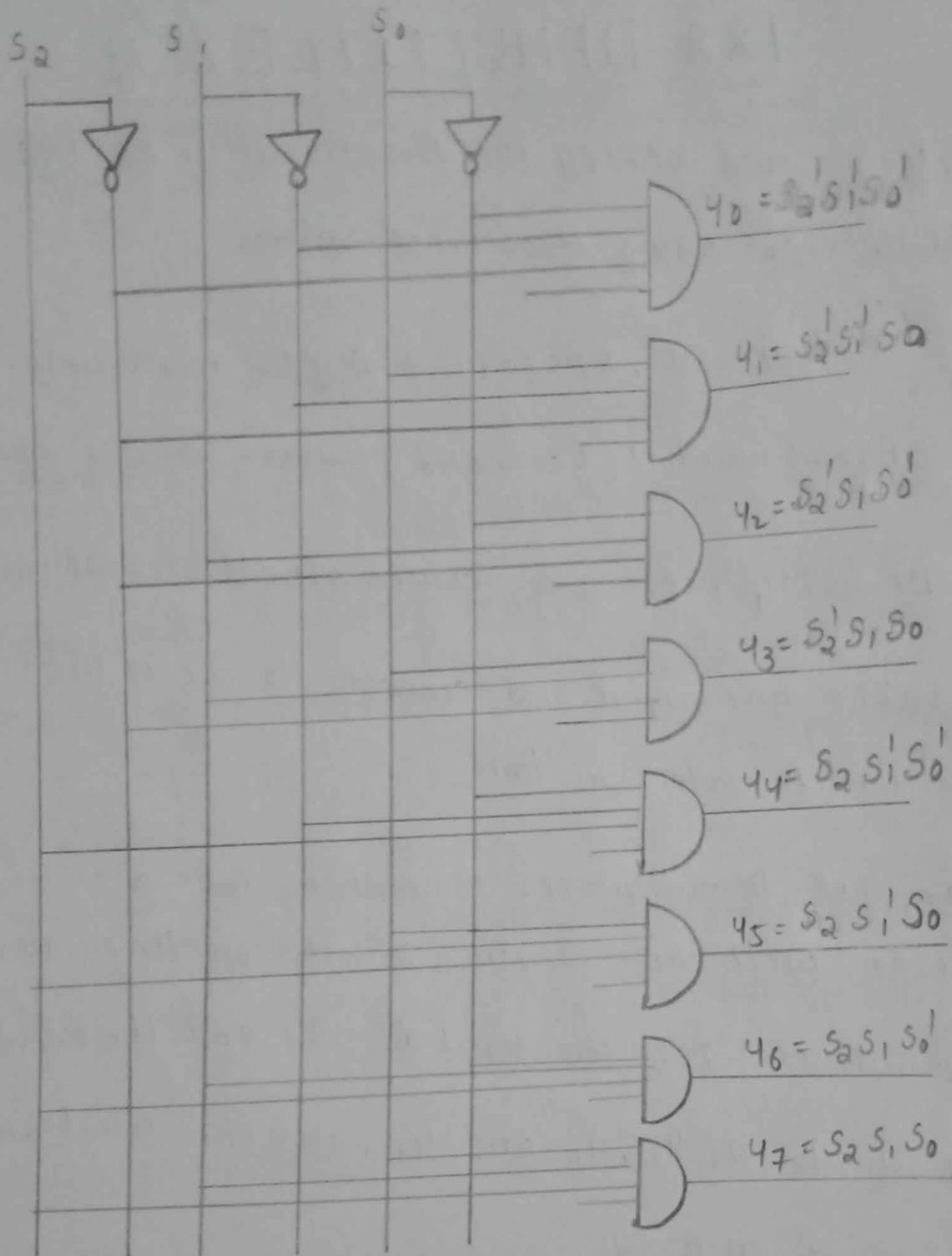
An 1x8 Demultiplexer is nothing but a demultiplexer with one input, 3 selection lines and $2^3 (8)$ outputs. Let the input be I_n and the outputs be $y_0, y_1, y_2, y_3, y_4, y_5, y_6$ and y_7 , and the selection lines be S_0, S_1 and S_2 .

Procedure:-

1) Check all the connections properly and fix them

properly, if any loose connections.

2) Connect the circuit as per the logical expressions.



Circuit diagram of 1×8 Demultiplexer

- 3) Construct the truth table for 1×8 demultiplexer for inputs.
- 4) Try all combinations of inputs to S_0, S_1, S_2 from RPS and record read corresponding outputs using MUX.
- 5) Compare the theoretical values with the practical values.

Precautions:-

- 1) Check whether all the components are working properly or not.
- 2) Make sure that all the connections are fixed without any loose connections.
- 3) Handle the components with utmost care.
- 4) Don't touch the live or naked wires.

Practical Values:-

Result:-

Thus designed and verified the functionality of
1x8 demultiplexer.

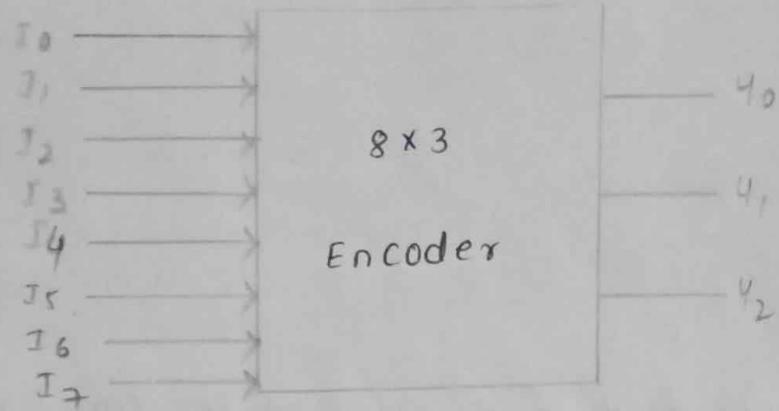


Fig: 8x3 Encoder

Truth table for 8x3 Encoder :-

inputs								outputs		
I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Y_2	Y_1	Y_0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

EXP NO: 6a

Date:

8x3 Encoder

Aim:- To design and verify the functionality of 8x3 Encoder using theoretical values.

Apparatus :- IC7404-1, 3C74H-3, Regulated Power Supply (0-30V)-1, Digital Multimeter-1, Breadboard-1, connecting wires, IC4072-2.

Theory:- An encoder is a combinational circuit which accepts one of 2^n inputs and encodes it from decimal to binary and results the n-bit binary digits. In 8x3 Encoder, the input is chosen from $2^3=8$ inputs and 3 bits as output.

Let the inputs be $I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7$ and outputs be Y_0, Y_1, Y_2 .

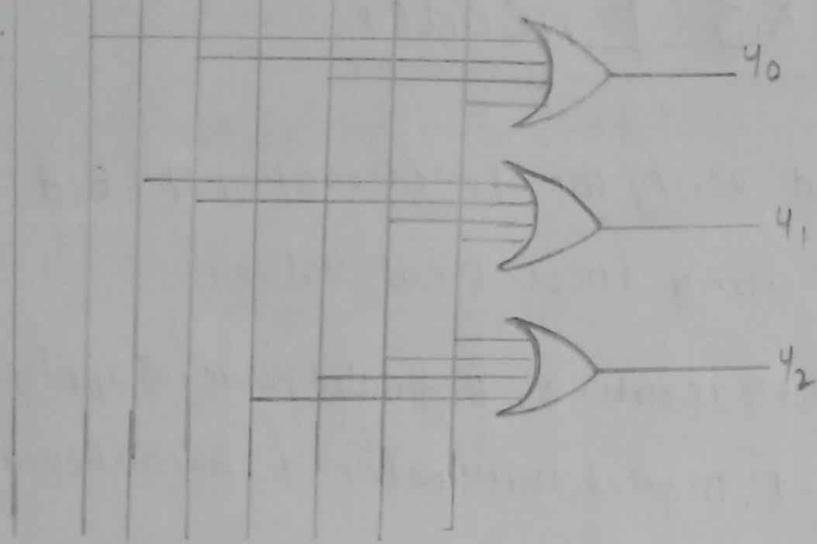
From truth table,

$$Y_0 = I_1 + I_3 + I_5 + I_7$$

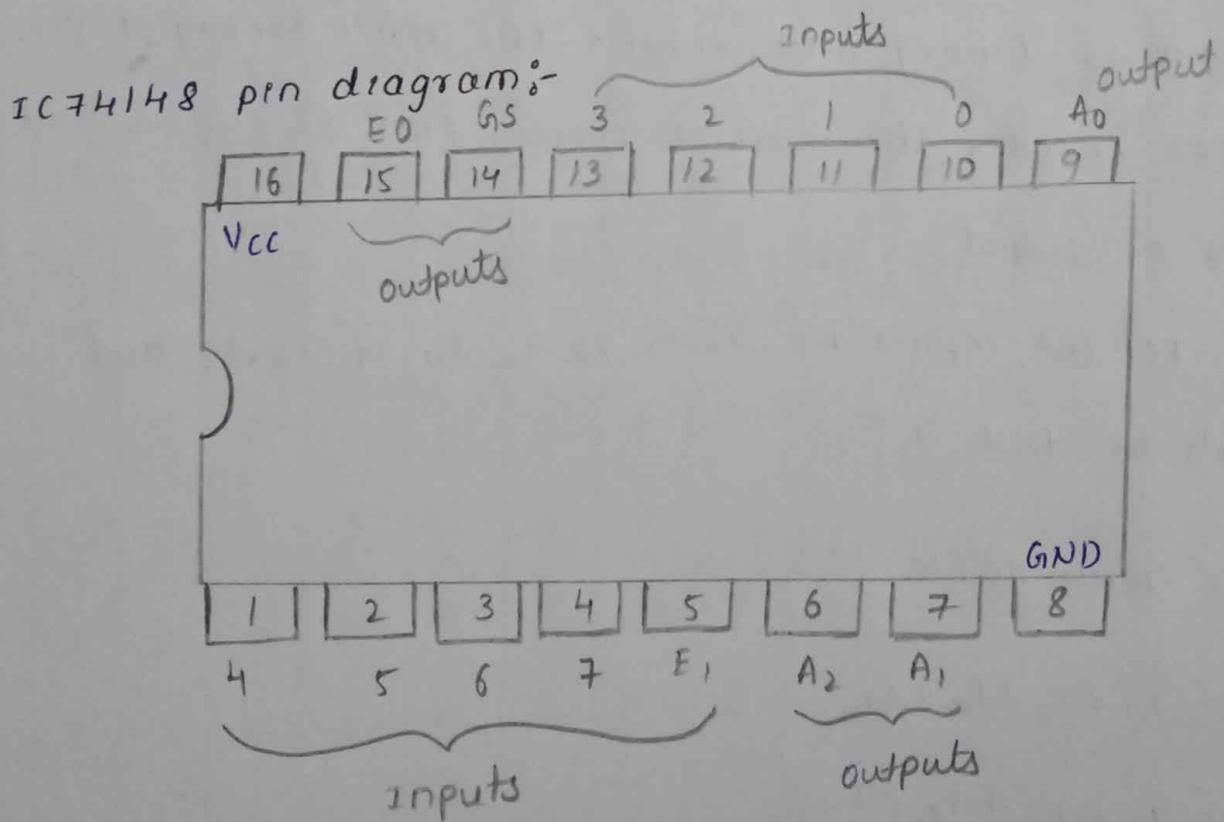
$$Y_1 = I_2 + I_3 + I_6 + I_7$$

$$Y_2 = I_4 + I_5 + I_6 + I_7$$

$I_0 \ I_1 \ I_2 \ I_3 \ I_4 \ I_5 \ I_6 \ I_7$



Circuit diagram of 8x3 Encoder



Procedure :-

- 1) check if any components are working properly or not.
- 2) check if any loose connections and fix them.
- 3) Connect the circuit as per the circuit diagram.
- 4) Construct the truthtable using 8x3 Encoder for various inputs.
- 5) Try all combinations of inputs to $I_7, I_6, I_5, I_4, I_3, I_2, I_1$, and I_0 from RPS ranging from 0V to 5V, and read corresponding outputs using multimeter.
- 6) Compare the theoretical and experimental values and conclude the functionality of 8x3 Encoder.

Precautions :-

- 1) Make sure that all the components which are connected are connected properly or not.
- 2) Avoid if any loose connections.

Practical values of 8x3 Encoders:-

Inputs								Outputs		
I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	q_2	q_1	q_0
ON	OFF	OFF	OFF							
OFF	ON	OFF	OFF	ON						
OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	ON
OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	OFF
OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON

Result:-

thus designed and verified the functionality of
8x3 Encoder.

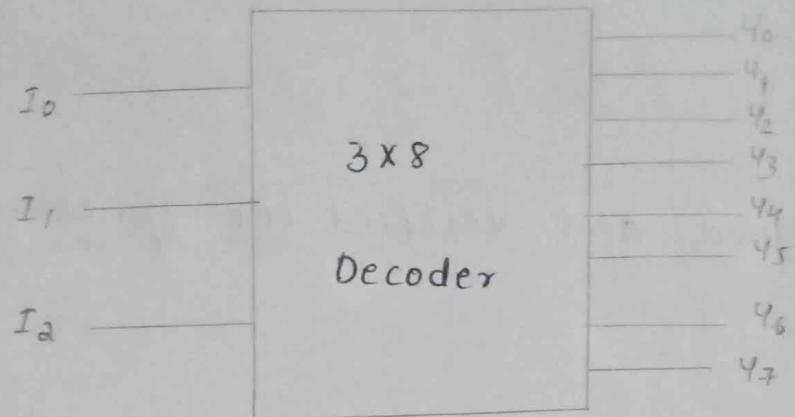


Fig: 3x8 Decoder

Truth Table for 3x8 Decoder:-

Inputs			Outputs							
I_2	I_1	I_0	4_7	4_6	4_5	4_4	4_3	4_2	4_1	4_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Experiment No:- 6b

Date

3x8 Decoder

Aim:- To design and verify the functionality of 3x8 Decoder using theoretical values.

Apparatus:- IC7404-1, I47411-3, RPS (0-30V)-1, Digital Multimeter -1, Breadboard -1, Connecting wires (as per required).

Theory:- A Decoder is a combinational circuit which takes n inputs and produces an output among 2^n possible outputs. It decodes the given n -bit binary number and produces its equivalent decimal code output. In 3x8 decoder, let the inputs be I_2, I_1, I_0 and outputs be $Y_0, Y_1, Y_2, Y_3, Y_4, Y_5, Y_6$ and Y_7 . From the truth

table we get,

$$Y_0 = I_2' I_1' I_0'$$

$$Y_1 = I_2' I_1 I_0'$$

$$Y_2 = I_2' I_1' I_0$$

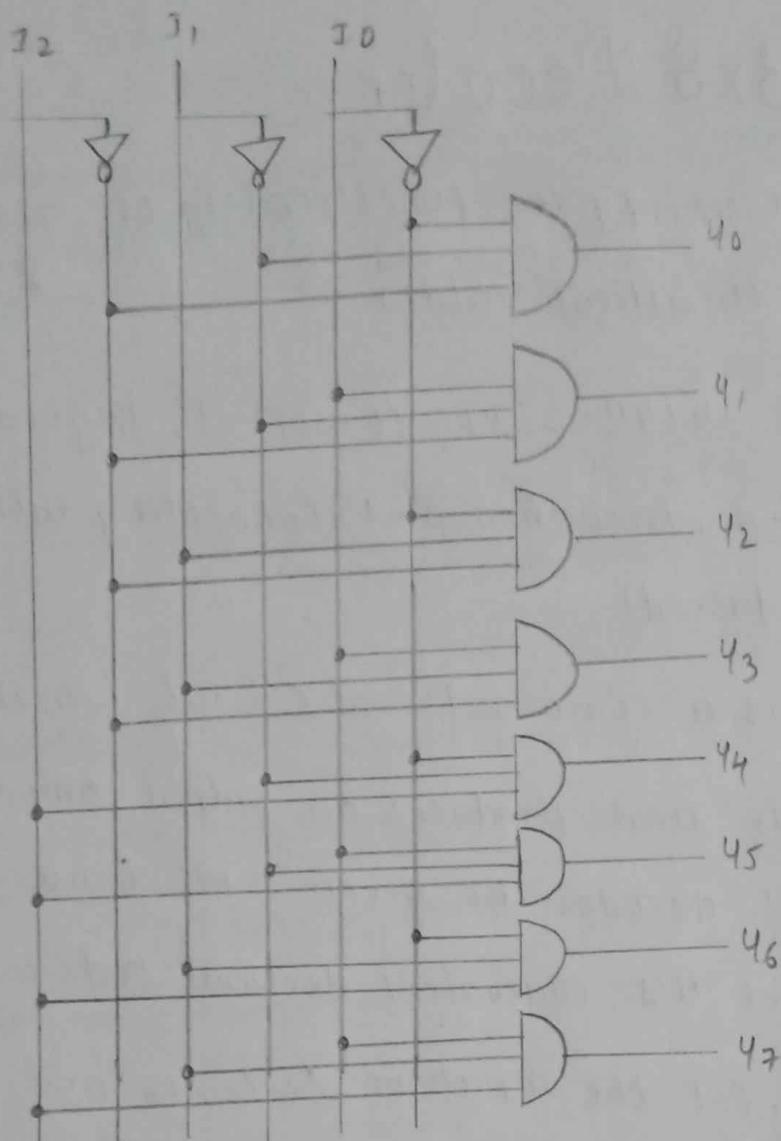
$$Y_3 = I_2' I_1 I_0$$

$$Y_4 = I_2 I_1' I_0$$

$$Y_5 = I_2 I_1 I_0'$$

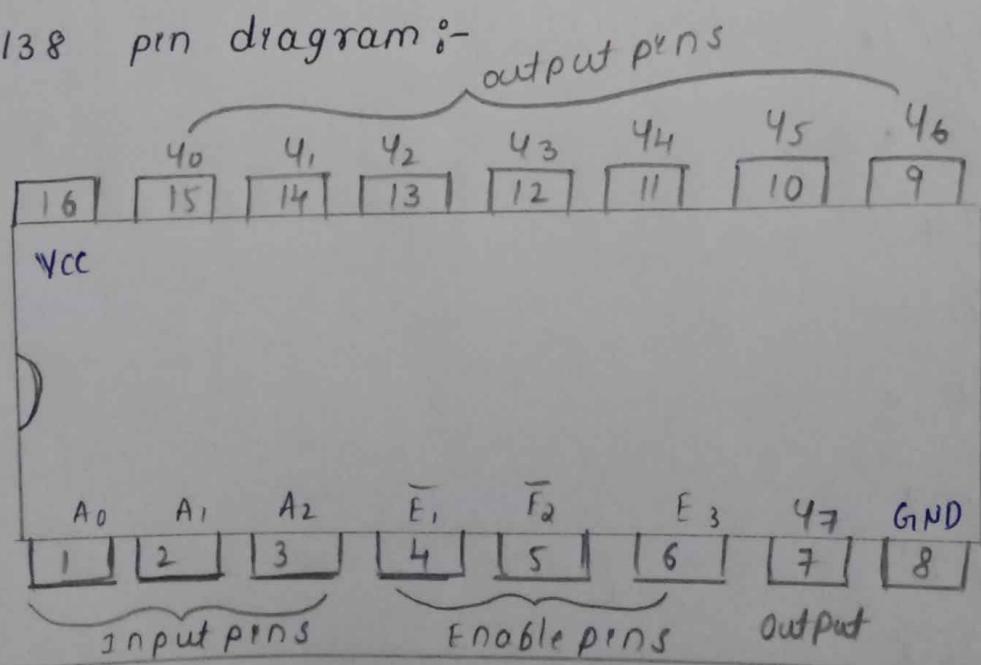
$$Y_6 = I_2 I_1' I_0$$

$$Y_7 = I_2 I_1 I_0$$



circuit diagram of 3x8 Decoder

IC 74138 pin diagram :-



Procedure:-

- 1) check if any loose connections and fix them properly.
- 2) Connect the circuit as per the circuit diagram.
- 3) Construct the truth table for 3x8 Decoder for various inputs.
- 4) Try all combinations of inputs to I_2, I_1, I_0 and from RPS read corresponding outputs using multimeter.
- 5) Compare the theoretical and practical reading and conclude the functionality of 3x8 Decoder.

Precautions:-

- 1) Avoid loose connections.
- 2) Make sure that all the components which are connected are connected properly or not.

Practical values for 3x8 Decoder:-

Inputs			Outputs							
I_2	I_1	I_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
ON	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
ON	ON	ON	ON	OFF						

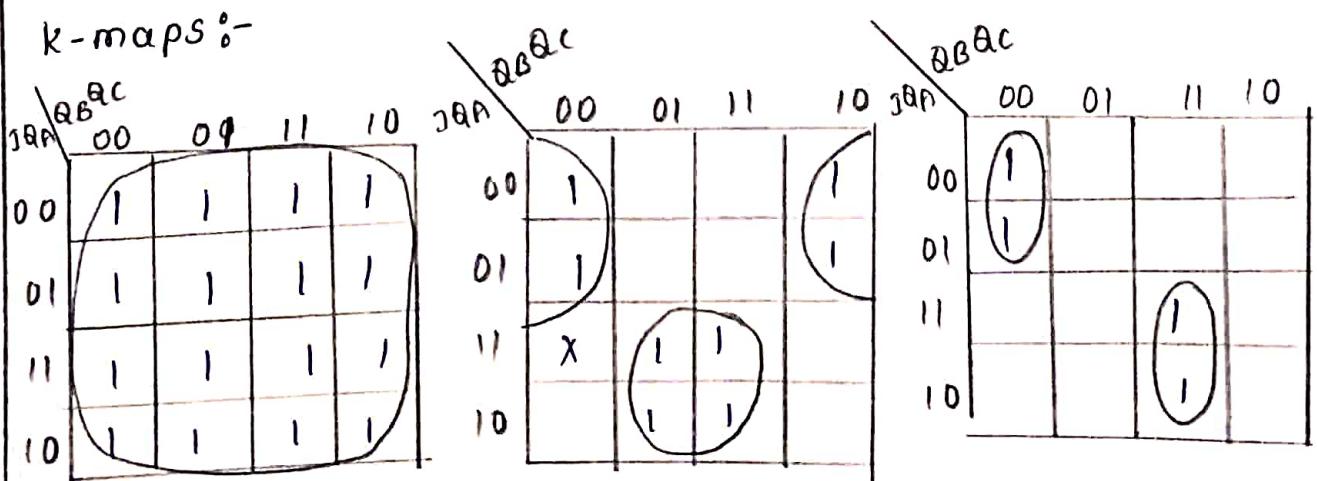
Results-

thus designed and verified the functionality
of 3x8 Decoder.

Truth Table :-

control Input (x)	Q_{A-1}	Q_{B-1}	Q_{C-1}	Q_A	Q_B	Q_C	T_A	T_B	T_C
0	0	0	0	1	1	1	1	1	1
0	0	0	1	0	0	0	0	0	1
0	0	1	0	0	0	1	0	1	1
0	0	1	1	0	1	0	0	0	1
0	1	0	0	0	1	1	1	1	1
0	1	0	1	1	0	0	0	0	1
0	1	1	0	1	0	1	0	0	1
0	1	1	1	1	1	0	0	0	1
1	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	0	1
1	0	1	0	0	1	1	0	0	1
1	0	1	1	1	0	0	1	1	1
1	1	0	0	1	0	1	0	0	1
1	1	0	1	1	1	0	0	1	1
1	1	1	0	1	1	0	0	1	1
1	1	1	1	0	1	1	0	0	1
1	1	1	1	1	0	0	1	1	1

K-maps :-



$$T_C = 1$$

$$T_B = I Q_C + I' Q_C'$$

$$T_A = I Q_B Q_C + I' Q_B' Q_C'$$

EXP NO:07

UP / Down Counter

Date:

Aim:- To design and verify the functionality of up / down counter by using theoretical values.

Apparatus:- IC 7400 - 2, IC 7410 - 1, RPS (0-30V) - 1, Digital Multimeter - 1, Bread board - 1, connecting wires (as per required), IC 7476 (T-Flipflops) - 2.

Theory:- An up / down counter is a sequential synchronous counter that can be either count in increasing order / decreasing order.

For a 3-bit up / down counter, it takes a mode control input which decides the working functionality. e.g., M=0 is up and M=1 is down counter. For synchronous counters, we generally use a kind of T-Flipflop. For 3-bits, we need 3 T-Flipflops.

Here the outputs for the flipflops are Q_A, Q_B, Q_C and the inputs for the flipflops are T_A, T_B, T_C.

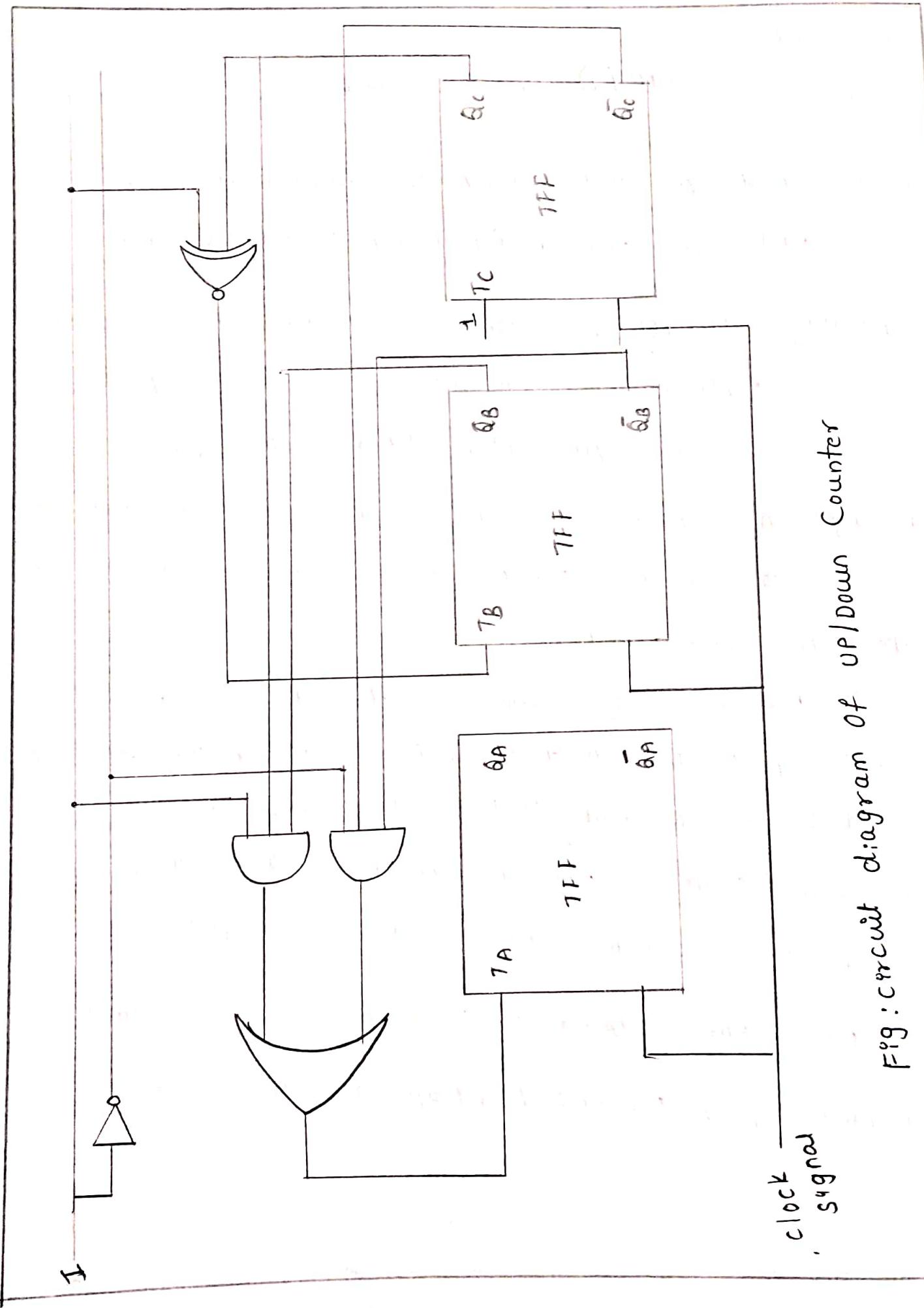


Fig : circuit diagram of Up/Down Counter

clock
signal

$$T_A = x'B'C' + xBC$$

$$T_B = xc + x'C'$$

$$T_C = 1$$

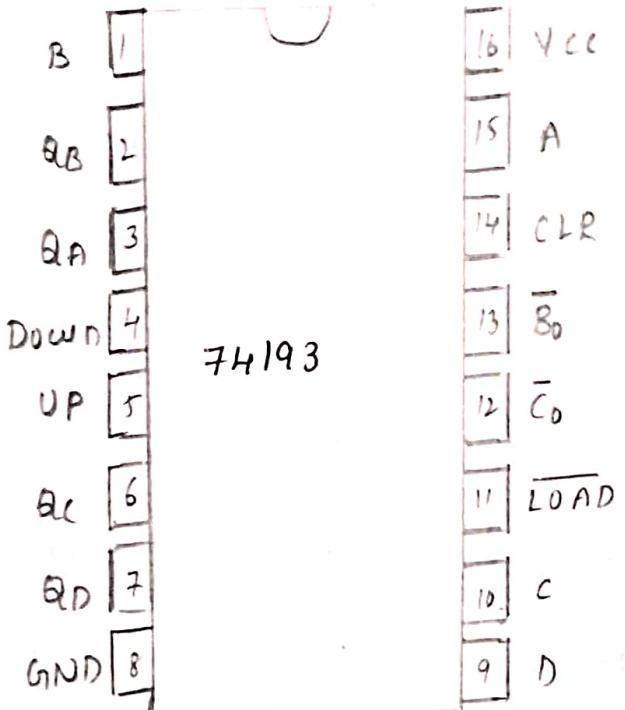
Procedure:-

- 1) check if any loose connections and fix them properly.
- a) Connect the circuit as per the circuit diagram.
- 3) Start giving all possible inputs from RNS to the circuit and read corresponding outputs.
- 4) Construct the truth table for up/down counters for various inputs.
- 5) Compare the theoretical and practical values and conclude the functionality of up/Down counter.

Precautions:-

- 1) Avoid loose connections
- 2) Make sure that all connections are connected properly or not.

IC 74193 :-



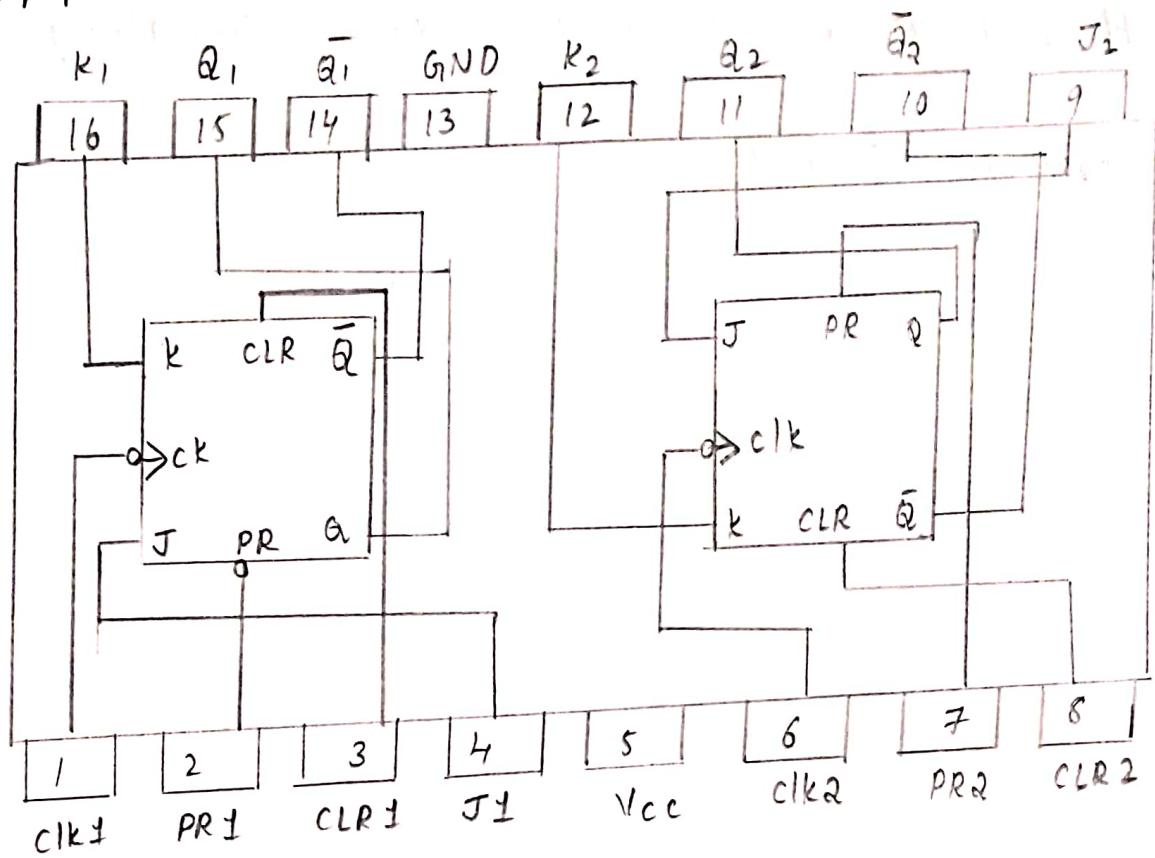
Practical values :-

X	QA-1	QB-1	QC-1	QA	QB	QC	TA	TB	TC
OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON
OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON
OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON
OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON
OFF	ON	OFF	OFF	OFF	ON	ON	ON	ON	ON
OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON
OFF	ON	ON	OFF	ON	OFF	ON	OFF	ON	ON
OFF	ON	ON	ON	ON	ON	OFF	OFF	OFF	ON
ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON
ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON
ON	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON
ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	ON
ON	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
ON	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON
ON	ON	ON	OFF	ON	ON	ON	OFF	OFF	ON
ON	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON

Result:-

Thus designed and verified the functionality
of UP/Down Counter.

1 flip flop IC - 7476



Truth Table :-

Left shift

clk	Q ₃	Q ₂	Q ₁	Q ₀
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	1	0	1
4	1	0	1	1

rightshift

clk	Q ₃	Q ₂	Q ₁	Q ₀
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	0	1	1	0
4	1	0	1	1

Practical values :-

Left shift

clk	Q ₃	Q ₂	Q ₁	Q ₀
0	OFF	OFF	OFF	OFF
1	OFF	OFF	OFF	ON
2	OFF	OFF	ON	OFF
3	OFF	ON	OFF	ON
4	ON	OFF	ON	ON

Rightshift

clk	Q ₃	Q ₂	Q ₁	Q ₀
0	OFF	OFF	OFF	OFF
1	ON	OFF	OFF	OFF
2	ON	ON	OFF	OFF
3	OFF	ON	ON	OFF
4	ON	OFF	ON	ON

EXP NO: 08

Date:

Universal Shift Register

Aim:- To design and verify the functionality of Universal shift register.

Apparatus:- IC 7400 - 4, Regulated Power Supply (RPS) (0-30V) - 1,
IC 7474 (D Flipflop) - 2, Digital Multimeter - 1,
Bread Board - 1, Connecting wires.

Theory:- A shift Register is a device which uses flipflops to store a sequence of bits of data and shifts the data among the flipflops. The shifting direction can be left to right or from right to left. A combination of both uni and bidirectional shift registers is called a "Universal shift Register". It has parallel load provision. An n bit shift register requires n no. of flipflops.

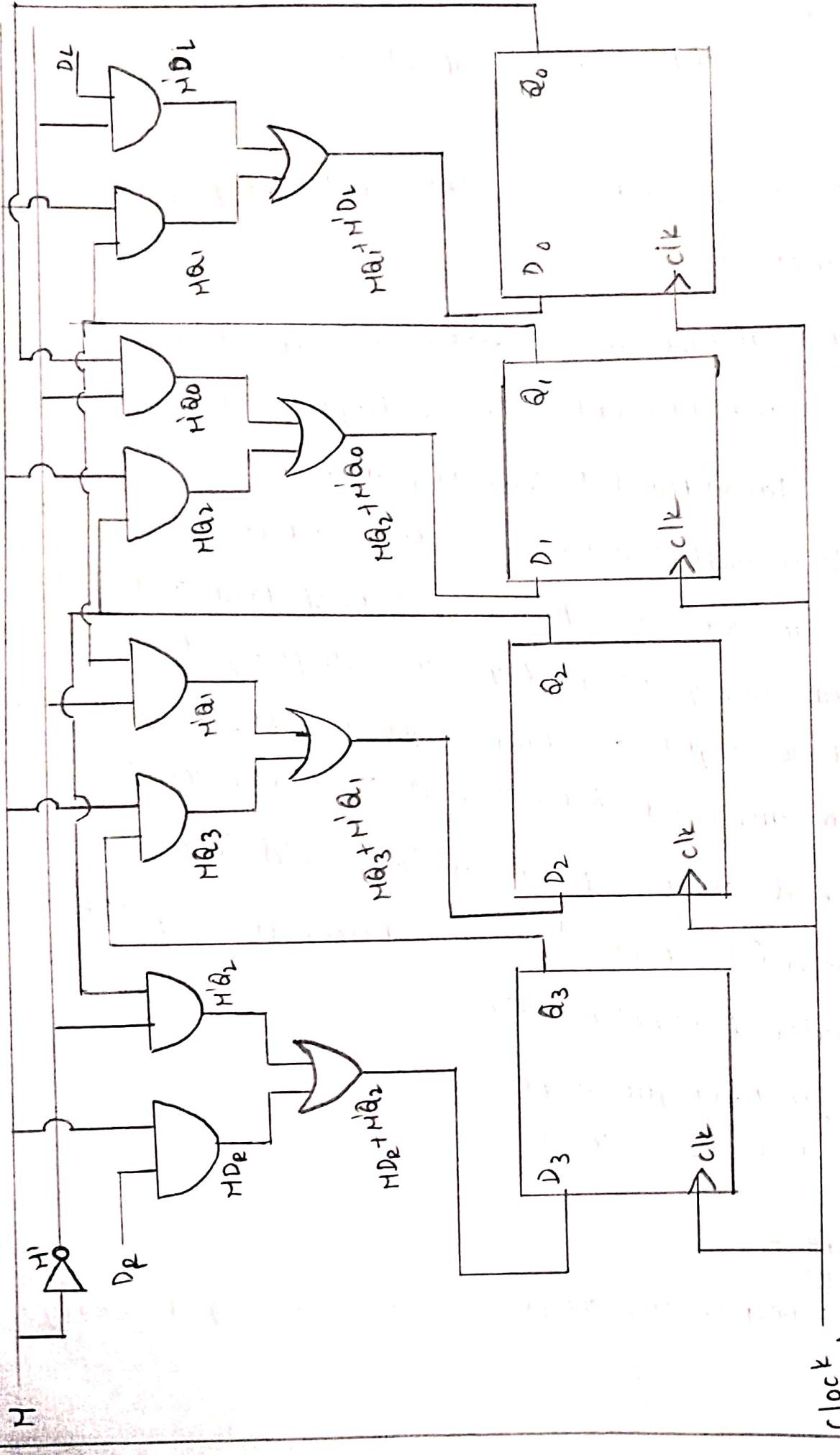
We consider D-Flipflops. Here,

Mode, $H=1 \rightarrow$ Right shift

$H=0 \rightarrow$ Left shift

Procedure:-

- 1) check whether the components are working properly or not.



Circuit Diagram of Universal Shift Register

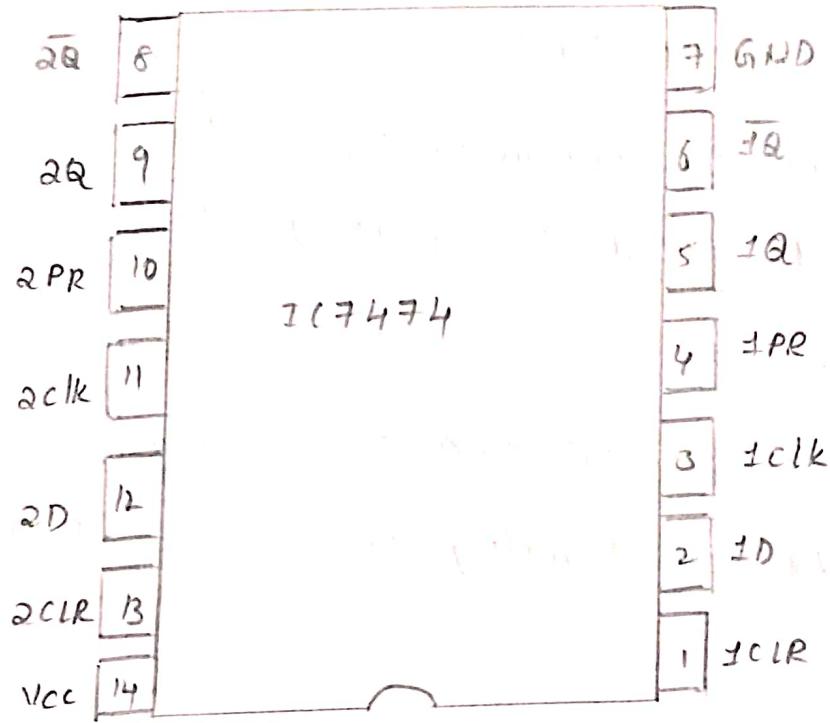
clock
signals

- 2) Connect the circuit as per the circuit diagram.
- 3) Construct the truth table for the universal shift register for various inputs.
- 4) Try all the combination of inputs from RPS to the circuit and record corresponding output values using multimeter.
- 5) Compare theoretical and experimental values and conclude the functionality of universal shift register.

Precautions :-

- 1) Make sure that all connections are connected properly or not.
- 2) Avoid if any loose connections and fix them tightly.

IC 7474 Dual D-Flipflop IC



Result:-

thus designed and verified the functionality of universal shift registers.

Truth Table for Modulo-10 Counter :-

Q_{A-1}	Q_{B-1}	Q_{C-1}	Q_{D-1}	Q_A	Q_B	Q_C	Q_D	T_A	T_B	T_C	T_D
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1
1	0	1	0	x	x	x	x	x	x	x	x
1	0	1	1	x	x	x	x	x	x	x	x
1	1	0	0	x	x	x	x	x	x	x	x
1	1	0	1	x	x	x	x	x	x	x	x
1	1	1	0	x	x	x	x	x	x	x	x
1	1	1	1	x	x	x	x	x	x	x	x

K-maps :-

		CD	00	01	11	10
AB	00					
01	00					
	01					
11	00	x	x	x	x	
	11	x	x	x	x	
10	00					
	10	1	x	x	x	

		CD	00	01	11	10
AB	00					
01	00					
	01					
11	00					
	11	x	x	x	x	
10	00					
	10	x	x	x	x	

$$T_A = AD + BCD$$

$$T_B = CD$$

EXP NO: 09

Date:

Modulo N-Counter

Aim :- To design and verify the functionality of Modulo N-Counter.

Apparatus :- IC 7408-1, IC 7432-1, Regulated Power Supply (0-30V)-1, Digital Multimeter-1, Breadboard-1, connecting wires (as per required), IC 7476 (7-flipflops)-2.

Theory :- The number of different output states a counter can produce is called the modulo counter. The modulus of a counter is given as 2^n where n = A number of flipflops for $n=3$, it can count maximum of $2^3=8$ counting states and would be called a Mod-8 counter. For $n=4$, it requires $n=4$ flipflops. $n=4$ counts $2^4=16$ counting states, it is called Mod-16 counter.

$$N=10 \Rightarrow 4 \text{ bits} \rightarrow 0-15$$

0-9 (We need to count)

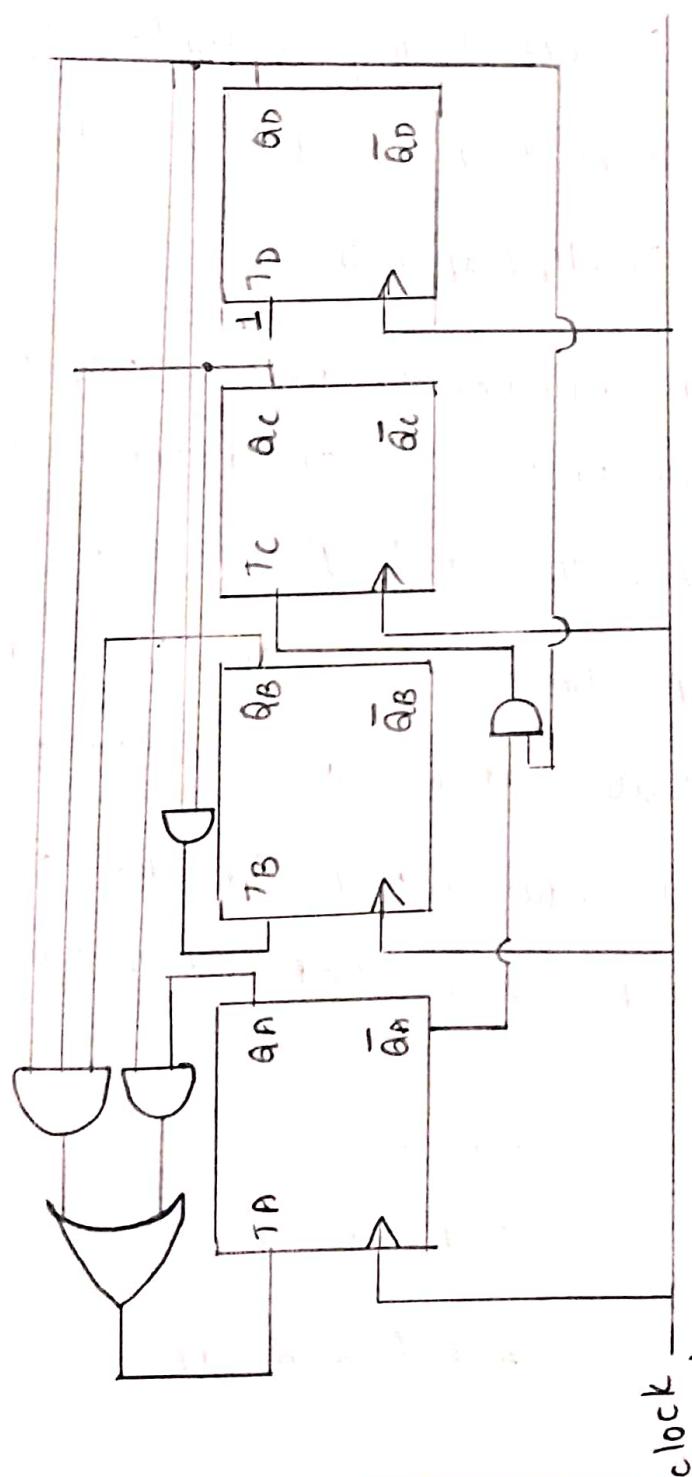
A-F (no need)

	CD	00	01	11	10
AB	00	1 1			
	01	1 1			
	11	X X	X X		
	10		X X		

$$T_C = A'D$$

	CD	00	01	11	10
AB	00	1 1 1 1			
	01	1 1 1 1			
	11	X X X X			
	10	1 1 X X			

$$T_D = 1$$



Circuit diagram of Modulo-10 Counter
clock signal

Procedure:-

- 1) Check whether the components are working properly or not.
- 2) Connect the circuit as per the circuit diagram.
- 3) Construct the truth table of Modulo-10 counter for various inputs.
- 4) Try all the combination of inputs using RPS ranging from 0V to 5V and read the values using Multimeter.
- 5) Compare the theoretical and experimental values of and conclude the functionality of Modulo-10 Counter.

IC 7490 (MOD-10 Counter) :-

clk A	NC	QA	QD	GND	QB	QC
14	13	12	11	10	9	8
1	2	3	4	5	6	7
clk B	R ₁	R ₂	NC	VCC	R ₃	R ₄

R - Reset

Q - output

Precautions:-

- 1) Avoid if any loose connections and fix them properly.
- 2) Make sure that all the connections are connected properly or not.
- 3) Don't touch the live and knocked wires.

Result:-

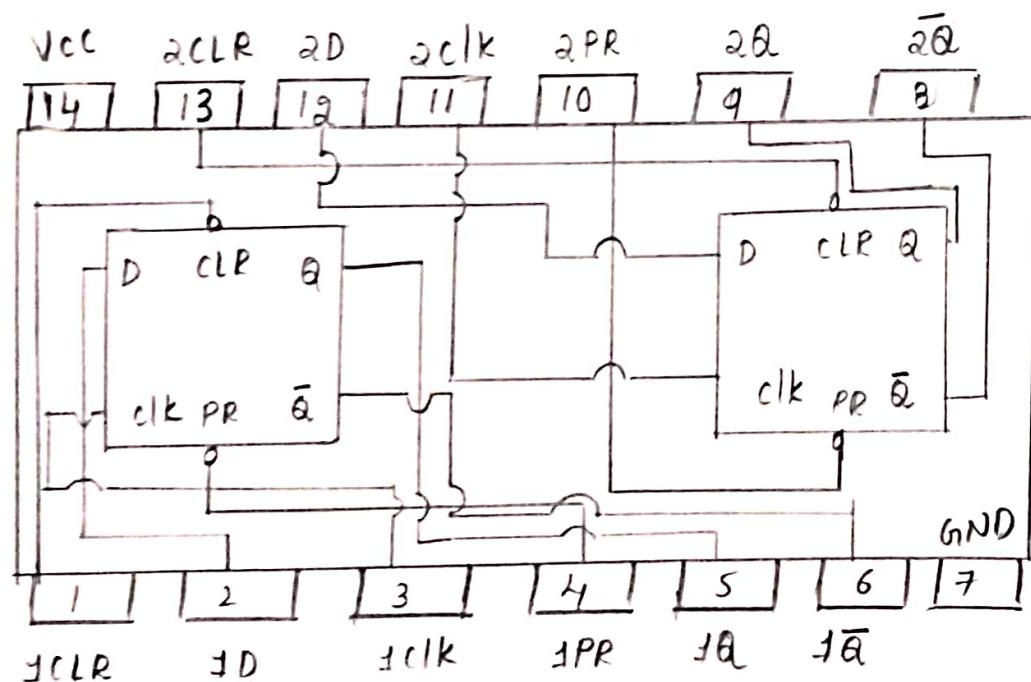
Thus designed and verified the functionality of Modulo - 10 counter.

Practical Values :-

Truth Table for Ring Counter :-

clock	Q_0	Q_1	Q_2	Q_3
0	1	0	0	0
1	0	1	0	0
a	0	0	1	0
3	0	0	0	1

IC 7474 (D-Flipflop) :-



EXP NO: 10

Date:

Ring Counter

Aim :- To design and verify the functionality of Ring counter using theoretical values.

Apparatus :- IC7474 (D-Flipflops)-2, RPS (0-30V) -1,
Digital Multimeter -1, Breadboard -1, Connecting wires (as per required).

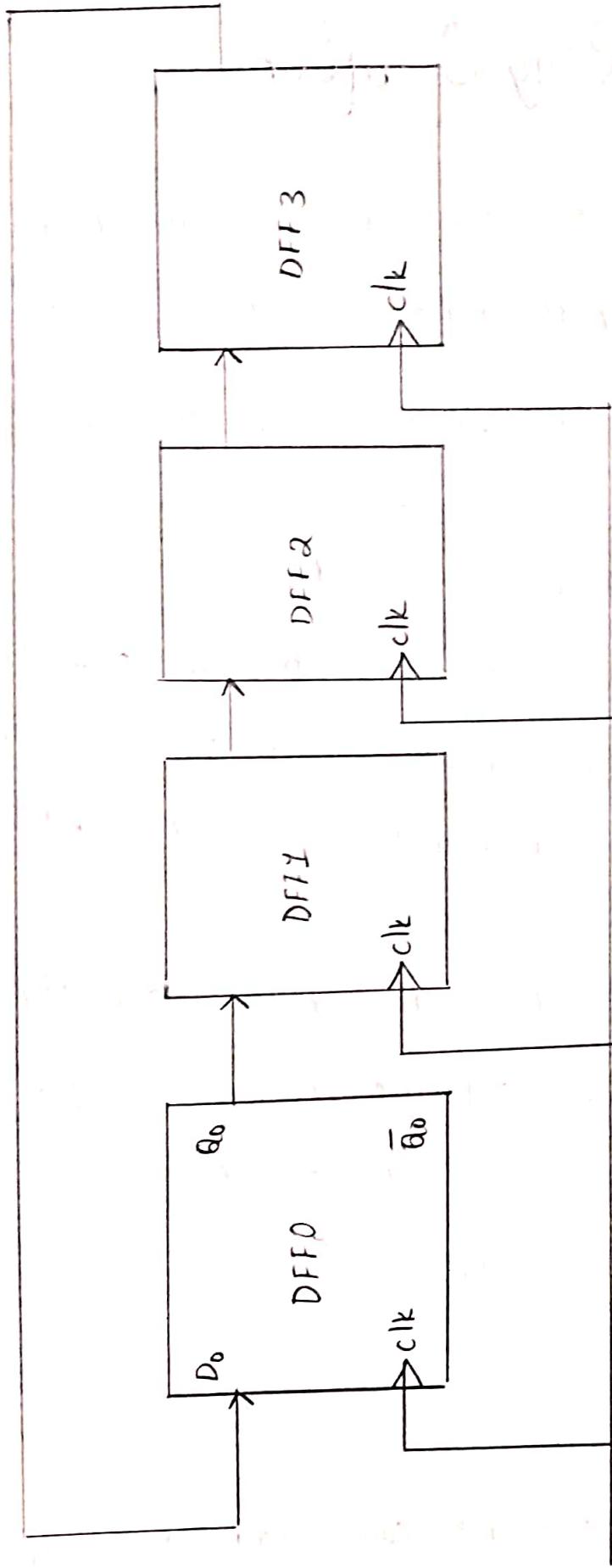
Theory :- A Ring counter is a synchronous counter. A Ring counter is a circular shift register with only one flipflop being set at any particular time, all others are cleared.

The single bit is shifted from one flipflop to the next to produce the sequence of timing signals.

For 4 bits, we need 4 D-Flipflops. Here D_0, D_1, D_2 and D_3 are the D-Flipflops.

Procedure :-

- 1) Check whether all the components are working properly or not.



Circuit diagram of Ring Counter using D-flipflops

clock
signal

- 2) Connect the circuit as per the circuit diagram.
- 3) Construct the truth table for Ring counter for clock inputs.
- 4) Try all the combinations of inputs using RPS ranging from 0V to 5V and read the corresponding values.
- 5) Compare the theoretical and practical values and conclude the functionality of ring counter.

Precautions :-

- 1) Check if any loose connections, and fix them properly.
- 2) Make sure that all the connections are connected properly or not.
- 3) Don't touch live and naked wires.

Practical Readings:-

clock	Q_0	Q_1	Q_2	Q_3
0	ON	OFF	OFF	OFF
1	OFF	ON	OFF	OFF
2	OFF	OFF	ON	OFF
3	OFF	OFF	OFF	ON

Result:-

thus designed and verified the functionality
of Ring Counter.