A quick recap of the material covered in lectures

MOS capacitor C-V characteristics

Consider a nMOS capacitor with p-type substrate doped with carrier density N_a. When threshold voltage is applied to the MOS capacitor, the depletion layer is formed at the oxide-semiconductor interface with a width x_d. Fermi potential - ϕ_F and surface potential in the semiconductor - ϕ_s.

- Metal-Semiconductor work function difference (for any Metal gate):

$$\boxed{\Phi_{ms} = \Phi'_m - \Phi_s = \Phi'_m - (\xi + \frac{E_g}{2q} + \phi_F)} \tag{1}$$

where ξ is electron affinity of semiconductor. In case of polysilicon gate, use $\Phi'_m = \xi$.

- Fermi potential:

$$\boxed{\phi_F = \frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right)} \tag{2}$$

- Flat band voltage:

$$\boxed{V_{FB} = \Phi_{ms} - \frac{Q'_{ss}}{C_{ox}}} \tag{3}$$

where $Q'_{ss} = Q_i$ is the trapped charge near the interface.

- The maximum depletion charge at maximum depletion layer width:

$$\boxed{|Q'_{SD}| = |Q_d| = qN_a x_{d,max}} \tag{4}$$

- Electric field is continuous at the interface:

$$\boxed{\epsilon_{ox} E_{ox} = \epsilon_s E_s} \quad \boxed{E_s = \frac{qN_a}{\epsilon_s} x_d} \tag{5}$$

- Depletion layer width and its maximum width:

$$\boxed{x_d = \sqrt{\frac{2\epsilon_s \phi_s}{qN_a}}} \quad \boxed{x_{d,max} = x_{d,T} = \sqrt{\frac{4\epsilon_s \phi_F}{qN_a}}; \qquad \phi_s = 2\phi_F} \tag{6}$$

- Threshold voltage:

$$\boxed{V_T = \begin{cases} \Phi_{ms} - \frac{Q'_{ss}}{C_{ox}} + 2\phi_s - \frac{Q_d}{C_{ox}} \\ V_{FB} + 2\phi_s - \frac{Q_d}{C_{ox}} \\ V_{FB} + 2\phi_s + \frac{\sqrt{4\epsilon_s q N_a \phi_F}}{C_{ox}}; \qquad \phi_s = 2\phi_F \end{cases}} \tag{7}$$

- MOS capacitance (per unit area):

$$\boxed{C_{max} = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}} \quad \boxed{\frac{1}{C_{min}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}} \tag{8}$$

- Total Capacitance per unit area when the frequency is low (LF-CV) and high (HF-CV) :

Capacitance	C_{LF}	C_{HF}	**Region**	**Biasing (nMOS cap)**
C	C_{ox}	C_{ox}	Accumulation	$V_G \leq V_{FB}$
	$\frac{1}{\frac{1}{C_{ox}}+\frac{x_d}{\epsilon_s}}$	$\frac{1}{\frac{1}{C_{ox}}+\frac{x_d}{\epsilon_s}}$	Depletion	$V_{FB} \leq V_G \leq V_T$
	C_{ox}	$\frac{1}{\frac{1}{C_{ox}}+\frac{x_{d,T}}{\epsilon_s}}$	Inversion	$V_G \geq V_T$

(9)

- If the frequency is low, the capacitance is initially maximum (C_{ox}), then reduces to minimum value (C_{min}) and thus again reaches maximum. Similarly, if the frequency is high the capacitance is initially maximum and it reduces to minimum value.

- The C-V characteristics depends on the carrier density, oxide thickness, temperature, frequency, interface trap charges. Thus the flat-band, threshold voltages shifts accordingly.

- If the MOS capacitor is biased deeply into the depletion region by extreme biasing, the depletion width will be increased and thus the capacitance reduces heavily (i.e. even below C_{min}).

- The equivalent oxide thickness (EOT) to replace ϵ_{SiO_2} with a high-κ dielectric $\epsilon_{high-\kappa}$, which is used to reduce quantum tunneling effects.

$$\boxed{\frac{\epsilon_{ox}}{t_{EOT}} = \frac{\epsilon_{high-\kappa}}{t_{high-\kappa}}} \tag{10}$$

Solve the following questions. There are 11 questions, for a total 25 marks.

1. (1 mark) The typical high-frequency MOS capacitance is less than the low-frequency capacitance in which region(s) of operation?

   A. accumulation

   B. inversion

   C. depletion

   D. accumulation and depletion

   E. accumulation and inversion

2. (1 mark) The threshold voltage (V_T) of an MOS capacitor decreases with a/an ______ in the gate oxide thickness (t_{ox}) and decreases with a/an ______ in the substrate doping concentration. Take the sign of Q_d into account.

   $V_T = -\frac{Q_d}{C_{ox}} + 2\phi_F$

   A. increase, increase

   B. decrease, increase

   If $C_{ox} \uparrow$, $V_T \downarrow$

   C. increase, decrease

   $C_{ox} \uparrow$ when $t_{ox} \downarrow$

   D. decrease, decrease

   E. no change, no change

3. (1 mark) The surface potential in n-MOS capacitor at the threshold voltage is $2\psi_F$. Hence, B

   A. $\frac{kT}{q} \ln \frac{N_a}{n_i}$

   B. $2\frac{kT}{q} \ln \frac{N_a}{n_i}$

   C. $\frac{kT}{q} \ln \frac{n_i}{N_a}$

   D. $\frac{3kT}{2q} \ln \frac{n_i}{N_a}$

   E. $2\frac{kT}{q} \ln \frac{n_i}{N_a}$

   F. $\frac{3kT}{2q} \ln \frac{N_a}{n_i}$

4. (2 marks) Consider a n-MOS capacitor where the gate is made of n^+ (poly) Si has doping $N_a = 1 \times 10^{16}\ cm^{-3}$ and oxide thickness (t_{ox}) is $50\ nm$. If the flat band voltage is $-1\ V$, the threshold voltage is ______ V. (take $n_i = 1.5 \times 10^{10}\ cm^{-1}$, $\epsilon_s = 11.9$, $\epsilon_0 = 8.85 \times 10^{-14}\ Fcm^{-1}$, $kT = 0.0259\ eV$, $\epsilon_{ox} = 3.9$)

A. 0.52

B. -0.52

C. 0.39

D. 0.24

E. -0.24

F. -0.39

$N_a = 10^{16}\ cm^{-3}$ $\quad \phi_F = KT \ln\left(\frac{N_a}{n_i}\right) = 0.0259 \times \ln\left(\frac{10^{16}}{1.5\times10^{10}}\right) = 0.347\ V$

At threshold the surface potential $\phi_s = 2\phi_F$

$Q_d = qN_a x_{dep}$ $\quad x_{dep} = \sqrt{\frac{2\epsilon_{si}}{q N_a} 2\phi_F}$

$= \sqrt{4\epsilon_{si} q N_a \phi_F}$

$C_{ox} = \frac{3.9 \times 8.85\times10^{-14}\ (F/cm)}{50\times10^{-7}\ (cm)}$

Q_d is negative

$V_T = V_{FB} - \frac{Q_d}{C_{ox}} + 2\phi_F$

$= -1 + \frac{\sqrt{4\epsilon_{si} q N_a \phi_F}}{C_{ox}} + 2\times0.347$

$= -1 + 0.7 + 0.694 = \underline{0.394}$

5. (4 marks) The high-frequency C–V plot of an ideal MOS capacitor as shown in the figure.

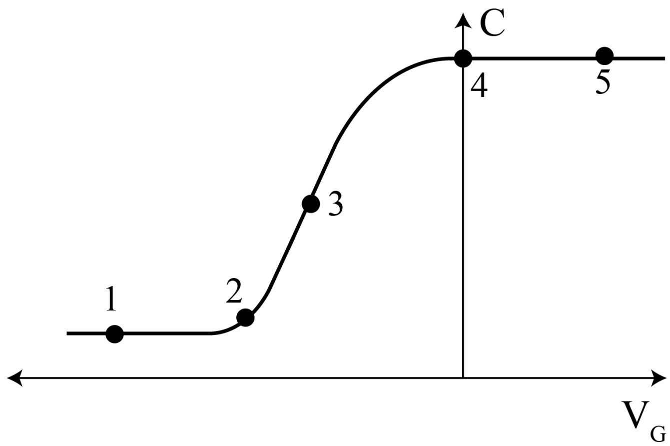


Figure 1: HFCV of MOSCAP

(a) (*1 mark*) Is this a PMOS or an NMOS device?

A. PMOS

B. NMOS

(b) (*3 marks*) For the biasing conditions mentioned below, identify the the corresponding points mentioned on the MOS $C - V$ plot. (Fill $1 - 5$ numbers corresponding to the blanks)

i. flat-band 4

ii. inversion 1

iii. accumulation 5

iv. threshold 2

v. depletion 3

Ans: (i) - 4; (ii) - 1; (iii) - 5; (iv) - 2; (v) - 3

6. (6 marks) Consider a silicon nMOS capacitor with doping $N_a = 1 \times 10^{17}\ cm^{-3}$, aluminium gate ($\phi_M = 4.1\ eV$), and an oxide thickness (t_{ox}) of $20\ nm$. Assume there is no fixed charge in the oxide or at the oxide-silicon interface. (Use $kT = 0.0259\ eV$, $\xi_{Si} = 4.05\ eV$, $n_i = 1.5 \times 10^{10}\ cm^{-3}$, $E_{g,Si} = 1.12\ eV$, $\epsilon_S = 11.9$, $\epsilon_{ox} = 3.9$)

   (a) (*2 mark*) Calculate the flat band voltage.

      A. -0.408 V

      B. 0.408 V

      C. -0.917 V

      D. 0.204

      E. -0.204

      F. 0.917 V

Work function of semiconductor

$$\phi_s = \xi_{Si} + E_g/2 + \phi_F$$

$$\phi_{ms} = \underbrace{4.1}_{\phi_M} - \underbrace{(4.05 + 0.56 + 0.406)}_{\phi_s}$$

$$V_{FB} = \phi_{ms} - \cancel{\frac{Q_{ox}}{C_{ox}}} \rightarrow 0$$

No charge in oxide or interface

$$= -0.916\,V$$

   (b) (*2 mark*) Calculate the oxide capacitance per unit area.

      A. 86 nF/cm^2

      B. 134.4 nF/cm^2

      C. 34.4 nF/cm^2

      D. 172 nF/cm^2

      E. 3.44 nF/cm^2

      F. 1.72 nF/cm^2

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{20 \times 10^{-7}}$$

$$= 172.6\ nF/cm^2$$

   (c) (*2 marks*) Calculate the threshold voltage.

      A. -0.92 V

      B. 0.92 V

      C. -0.85 V

      D. 0.85 V

      E. 0.42

      F. -0.42

$$V_T = V_{FB} - \frac{Q_d}{C_{ox}} + 2\phi_F$$

$$= -0.916 + \frac{\sqrt{4\epsilon_{Si} q N_a \phi_F}}{C_{ox}} + 2 \times 0.406$$

$$= 0.85\,V$$

Previous year GATE questions

7. (2 marks) **(EC-GATE 2007)** Consider a MOS capacitor of area $4 \times 10^{-4}\ cm^2$. Use $\epsilon_{si} = 1 \times 10^{-12}\ F/cm$ and $\epsilon_{sio_2} = 3.5 \times 10^{-13}\ F/cm$.

Capacitance is given in pF, not PF/cm² !

$C_{ox} = 7\ pF = \frac{\epsilon_{ox}}{t_{ox}} \times Area$ F/cm²

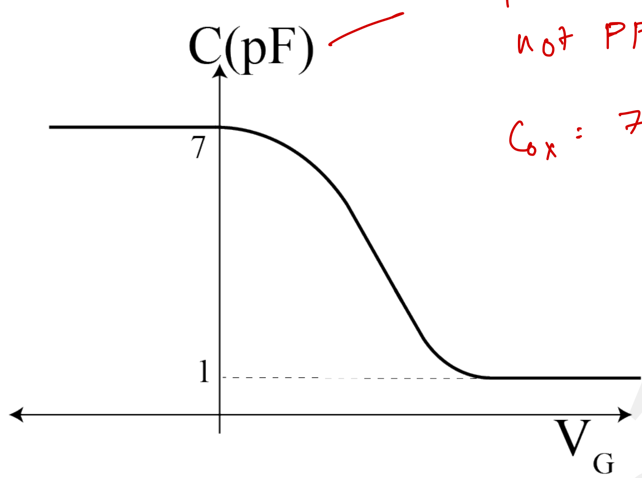


Figure 2: HFCV of NMOS Capacitor

(a) (*1 marks*) The gate oxide thickness in the MOS capacitor is ______ nm.

A. 140

B. 70

C. 200

D. 100

E. 250

F. 1000

$t_{ox} = \frac{\epsilon_{ox} A}{C_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14} \times 4 \times 10^{-4}}{7 \times 10^{-12}}$

$= 1.97 \times 10^{-5}$ cm

$= 197$ nm

~ 200 nm

(b) (*1 marks*) The maximum depletion layer width is ______ μm.

A. 7.5

B. 3.4

C. 1.5

D. 2.5

E. 0.95

F. 0.6

$C_{min} = 1$ pF

$\frac{1}{C_{min}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$

$\therefore C_{dep} = \frac{C_{min} \times C_{ox}}{C_{ox} - C_{min}} = \frac{1 \times 7}{6}$ pF

$C_{dep} = \frac{\epsilon_{si} A}{W_{dep,max}}$

$W_{max} = \frac{11.9 \times 8.85 \times 10^{-14} \times 4 \times 10^{-4}}{7/6 \times 10^{-12}}$

~ 0.00036 cm

~ 3.6 um

with given ϵ_{ox} & ϵ_{si} it will vary slightly. I choose closest answer.

8. (2 marks) **(EC-GATE 2015)** In MOS capacitor with an oxide layer thickness of $10\ nm$, the maximum depletion layer thickness is $100\ nm$. The permittivities of the semiconductor and the oxide layer are ϵ_s and ϵ_{ox} respectively. Assume $\frac{\epsilon_s}{\epsilon_{ox}} = 3$, the ratio of maximum to the minimum capacitance is _______.

   A. 8.66

   B. 0.75

   C. 4.33

   D. 0.33

   E. 3

   F. 1

$$\frac{C_{ox}}{C_{min}} = \frac{C_{ox}}{\left(\frac{C_{ox}\,C_{dep}}{C_{ox}+C_{dep}}\right)}$$

$$= 1 + \frac{C_{ox}}{C_{dep}}$$

$$= 1 + \frac{\epsilon_{ox}/t_{ox}}{\epsilon_{si}/W_{dep}} = 1 + \frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{W_{dep}}{t_{ox}}$$

$$= 1 + \frac{1}{3} \cdot \frac{100}{10} = 4.33$$

9. (2 marks) **(EC-GATE 2016)** Figures I and II show two MOS capacitors of unit area. The capacitor in Figure I has insulator materials X (of thickness $t_1 = 1\ nm$ and dielectric constant $\epsilon_1 = 4$) and Y (of thickness $t_2 = 3\ nm$ and dielectric constant $\epsilon_2 = 20$). The capacitor in Figure II has only insulator material X of thickness t_{eq}. If the capacitors are of equal capacitors, then the value of t_{eq} is ______ nm.

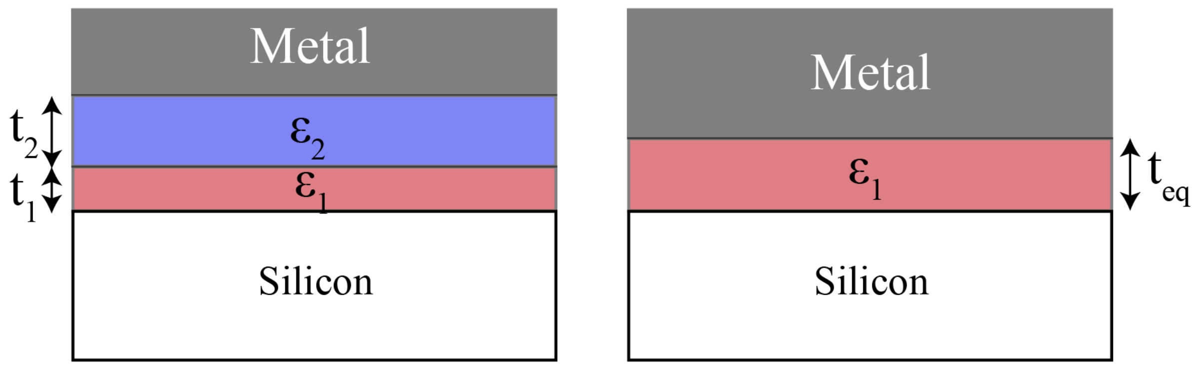


Figure I Figure II

A. 0.5

B. 5

C. 3.2

D. 10

E. 1

F. 1.6

Fig. 1 has 2 capacitors in series.

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{\frac{\epsilon_1}{t_1} \times \frac{\epsilon_2}{t_2}}{\frac{\epsilon_1}{t_1} + \frac{\epsilon_2}{t_2}} = \frac{\epsilon_1 \epsilon_2}{\epsilon_1 t_2 + \epsilon_2 t_1}$$

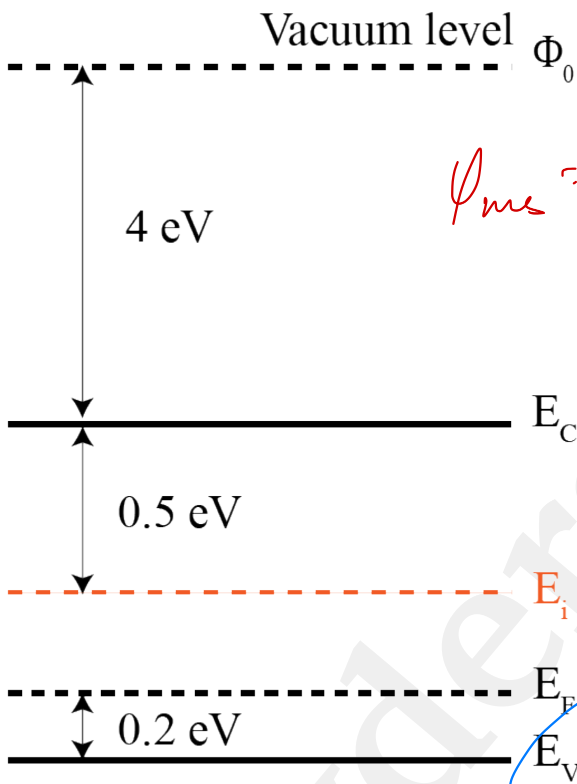
Since both figures have same capacitance

$$\frac{\cancel{\epsilon_1}}{t_{eq}} = \frac{\cancel{\epsilon_1} \epsilon_2}{\epsilon_1 t_2 + \epsilon_2 t_1}$$

$$t_{eq} = \frac{\epsilon_1 t_2 + \epsilon_2 t_1}{\epsilon_2} = \frac{4 \times 3 + 20 \times 1}{20}$$

$$= 1.6$$

10. (2 marks) **(EC-GATE 2020)** The band diagram of a p-type semiconductor with a band-gap of 1 eV is shown in the figure. Using this semiconductor, a MOS capacitor having V_{Th} of $-0.16\ V$, C'_{ox} of 100 nF/cm^2 and a metal work function of $3.87\ eV$ is fabricated. There is no charge within the oxide. If the voltage across the capacitor is V_{Th}, the magnitude of depletion charge per unit area (in nC/cm^2) is _______.



$\phi_{ms} = \phi_m - \phi_s$

$= 3.87 - (4 + 0.5 + 0.3)$

$= -0.93$

No oxide/interface charges

$= 0.3\ eV$

$V_T = \phi_{ms} - \cancel{\frac{Q_{ox}}{C_{ox}}} \to 0 - \frac{Q_d}{C_{ox}} + 2\phi_F$

A. 9.3

B. 5.2

C. 17.0

D. 14.1

E. 6.9

F. 1.70

$-0.16 = -0.93 - \frac{Q_d}{C_{ox}} + 0.6$

$-\frac{Q_d}{C_{ox}} = +0.17$

Since substrate is p type Q_d is negative

$\therefore |Q_d| = 0.17 \times 100 \times 10^{-9}\ C/cm^2$

$= 17\ nC/cm^2$

11. (2 marks) **(EC-GATE 2017)** A MOS capacitor is fabricated on p-type Si (silicon) where the metal work function is $4.1\ eV$ and electron affinity of Si is $4.0\ eV$, $E_C - E_F = 0.9\ eV$; where E_C and E_F are conduction band minimum and the Fermi energy levels of Si, respectively, $\epsilon_{ox} = 3.9$, $\epsilon_0 = 8.85 \times 10^{-14}\ F/cm$, oxide thickness $t_{ox} = 0.1\ \mu m$ and electron charge $q = 1.6 \times 10^{-19}\ C$. If the measured flat band voltage of this capacitor is $-1V$, then the magnitude of the fixed charge at the oxide semiconductor interface is ______ nC/cm^2.

Ans: 6.9

Range: $6.5 - 7.5$

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} \quad ?$$

$$\phi_{ms} = 4.1 - (4 + 0.9) = -0.8V$$

$$C_{ox} = \frac{3.9 \times 8.85 \times 10^{-14}}{0.1 \times 10^{-4}} = 34.5\ nF/cm^2$$

$$-1 = -0.8 - \frac{Q_{ox}}{34.5\ nF/cm^2}$$

$$\Rightarrow Q_{ox} = 0.2 \times 34.5\ nC/cm^2 = 6.9\ nC/cm^2$$