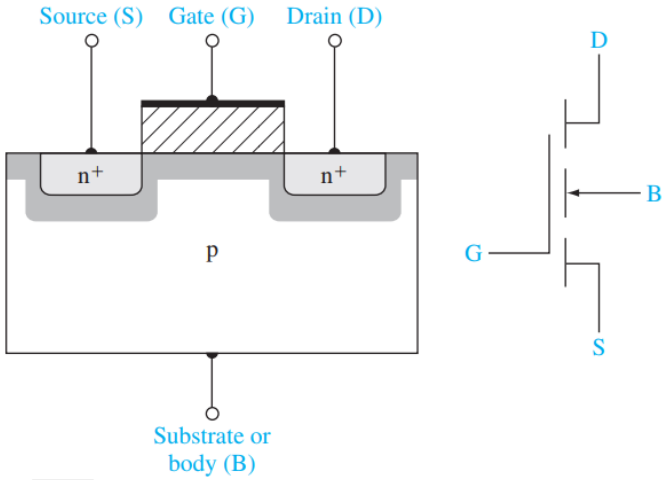
A quick recap of the material covered in lectures

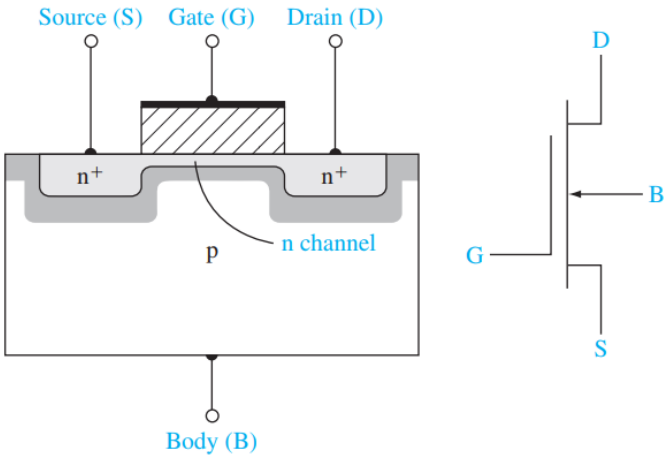
This week was devoted to understanding the physics and characteristics of metal-oxide-semiconductor field-effect transistor (MOSFET). The MOS structure was assumed to be ideal and considerations were limited to basic transistor configuration. When a MOSFET is biased into inversion, the induced surface layer forms a conducting channel between the source and drain contacts. The greater the applied gate voltage in excess of turn-on, the larger the conductance of the internal channel at a given drain voltage. A nonzero drain voltage in turn initiates the current flow between the source and drain. The current flow is proportional to V_D at low drain voltages, slopes over due to channel narrowing as V_D is increased, and eventually saturates once the internal channel vanishes or pinches off near the drain. A summary of formulas for the same is given below.

Enhancement and Depletion MOSFET

- In an enhancement mode MOSFET, the semiconductor substrate is not inverted directly under the oxide with zero gate voltage. A positive gate voltage induces the electron inversion layer, which then "connects" the n-type source and the n-type drain regions. Figure below shows an n-channel enhancement MOSFET.



- In depletion mode MOSFET, n-channel region exists under the oxide with 0 V applied to the gate, meaning an electron inversion layer already exists with zero gate voltage applied. Figure below shows an n-channel depletion MOSFET.



Current-Voltage Relationships

- Here we are considering n-channel MOSFETS for writing the equations. Similar relationships apply for p-channel. In the nonsaturation region, the current is given by -

$$\boxed{I_D = \frac{W\mu_n C_{ox}}{2L}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right]} \tag{1}$$

  The $\frac{V_{DS}^2}{2}$ term can be neglected for small values of V_{DS}.

$$\boxed{I_D = K_n\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right]} \tag{2}$$

  where $K_n = \frac{Wk_n'}{2L}$; $k_n' = \mu_n C_{ox}$

- The peak current occurs when $V_{DS} = V_{DS(sat)}$. At this point saturation occurs,

$$\boxed{V_{DS(sat)} = V_{GS} - V_T} \tag{3}$$

- For $V_{DS} > V_{DS(sat)}$, the ideal drain current is constant and is given by -

$$\boxed{I_{D(sat)} = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2} \tag{4}$$

- MOSFET transconductance is defined as the change in the drain current with respect to the corresponding change in gate voltage.

$$\boxed{g_m = \frac{\partial I_D}{\partial V_{GS}}} \tag{5}$$

- For MOSFET operating in the nonsaturation region,

$$\boxed{g_m = \frac{W\mu_n C_{ox}}{L}V_{DS}} \tag{6}$$

- For MOSFET operating in the saturation region,

$$\boxed{g_m = \frac{\partial I_{D(sat)}}{\partial V_{GS}} = \frac{W\mu_n C_{ox}}{L}(V_{GS} - V_T)} \tag{7}$$

Substrate Bias

- The source-to-substrate pn junction must always be zero or reverse biased, so V_{SB} must always be greater than or equal to zero for an n-channel MOSFET.
- The change in threshold voltage due to substrate bias is -

$$\boxed{\Delta V_T = \gamma\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]} \quad \boxed{\phi_{fp} = V_t \ln\left(\frac{N_A}{n_i}\right)} \tag{8}$$

- where γ is body coefficient defined as -

$$\boxed{\gamma = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}}} \tag{9}$$

Solve the following questions. There are 15 questions, for a total 25 marks.

1. (1 mark) For an ideal p-type Enhancement MOSFET, choose the correct statement.

   A. A hole inversion layer is created for an applied bias of $|V_G| > |V_t|$

   B. An electron inversion layer is created for an applied bias of $|V_G| > |V_t|$

   C. A hole inversion layer exists for $V_G = 0$

   D. An electron inversion layer is created for an applied bias of $|V_G| < |V_t|$

   E. An electron inversion layer exists for $V_G = 0$

   F. A hole inversion layer is created for an applied bias of $|V_G| < |V_t|$

2. (2 marks) Consider an n-channel MOSFET with the following parameters: $k'_n = 0.18\ mA/V^2$, $W/L = 8$, and $V_T = 0.4\ V$. The drain current I_D for $V_{GS} = 0.8\ V$ and $V_{DS} = 1.2\ V$ is _____

   A. $0.2304\ mA$

   B. $0.1152\ mA$

   C. $0.2304\ \mu A$

   D. $0.1152\ \mu A$

   E. $86.4\ mA$

   F. $0.0576\ mA$

$V_{GS} = 0.8V \quad V_{DS} = 1.2V$

Since $V_{DS} > V_{GS} - V_T$ the device is in saturation.

k_n' (process transconductance parameter)

$$I_D = \mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2$$

$$= 0.18 \times \frac{8}{2} (0.4)^2$$

$$= 0.115\ mA$$

3. (1 mark) For a long channel MOSFET biased "beyond pinch-off", the saturated drain current varies as -

   A. $(V_{GS} - V_T)^{0.5}$

   B. $(V_{GS} - V_T)^{1.0}$

   C. $(V_{GS} - V_T)^{1.5}$

   D. $(V_{GS} - V_T)^{2.0}$

   E. $(V_{GS} - V_T)^{2.5}$

4. (2 marks) Answer the following in relation to subthreshold swing of a MOSFET.

   (a) (*1 mark*) The subthreshold swing is defined as:

   A. The increase in gate voltage necessary to increase the drain current by a factor of 2.

   B. The increase in gate voltage necessary to increase the drain current by a factor of 10.

   C. The increase in drain voltage necessary to increase the drain current by a factor of 2.

   D. The increase in drain voltage necessary to increase the drain current by a factor of 10.

   E. The increase in source voltage necessary to increase the drain current by a factor of 2.

   (b) (*1 mark*) What is the minimum subthreshold swing at $T = 300\ K$? of a classical MOSFET

   A. $30\ mV/decade$

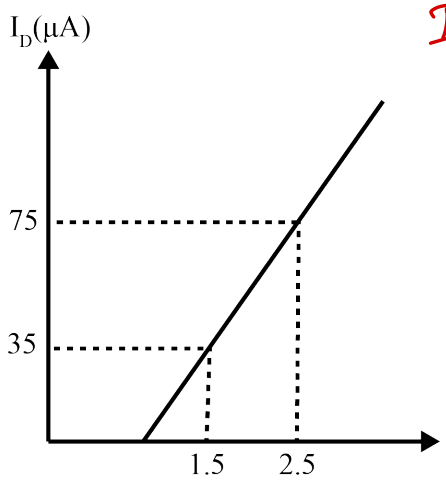
   B. $60\ mV/decade$

   C. $90\ mV/decade$

   D. $120\ mV/decade$

   E. $150\ mV/decade$

5. (3 marks) The I_D vs V_{GS} characteristics determined experimentally for an n-channel MOSFET are given in figure 1. The width and length of this device is $15\ \mu m$ and $2\ \mu m$ respectively. Assuming the drain voltage $V_{DS} = 0.1\ V$, and oxide capacitance $C_{ox} = 6.9 \times 10^{-8}\ Fcm^{-2}$,



$I_D = \mu C_{ox} \frac{W}{2L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$

Two unknowns: μ & V_T

Apply the equation above at $V_{GS} = 1.5V$ and $V_{GS} = 2.5V$ and solve for μ & V_T

Figure 1: I_D vs V_{GS}

(a) (*2 marks*) the mobility of carriers in the inversion region is _____ $(cm^2/V-s)$ (rounded off to the nearest integer)

Ans: 773

Range: $770 - 777$

(b) (*1 mark*) the threshold voltage for the MOSFET is _____ V (*Hint: Ignore V_{DS}^2 term for calculation*)

A. 0.6

B. 0.7

C. 0.625

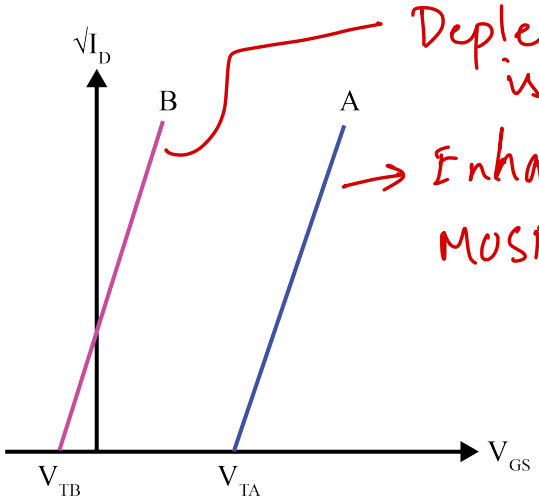
D. 0.72

E. 0.9

F. 1.0

Since V_{DS} is small relative to V_{GS}, V_{DS}^2 can be ignored.

6. (2 marks) The $\sqrt{I_D}$ vs V_{GS} plot for two MOSFETS A and B in saturation is given in figure 2. Identify the type of MOSFETS from the given choices.



Depletion mode MOSFET is on at $V_{GS}=0$

→ Enhancement mode MOSFET turns on for $V_{GS}>0$

Figure 2: $\sqrt{I_D}$ vs V_{GS}

A. $A \rightarrow Depletion\ n-MOSFET$; $B \rightarrow Depletion\ p-MOSFET$

B. $A \rightarrow Enhancement\ n-MOSFET$; $B \rightarrow Enhancement\ p-MOSFET$

C. $A \rightarrow Enhancement\ n-MOSFET$; $B \rightarrow Depletion\ n-MOSFET$

D. $A \rightarrow Depletion\ n-MOSFET$; $B \rightarrow Enhancement\ n-MOSFET$

E. $A \rightarrow Enhancement\ n-MOSFET$; $B \rightarrow Depletion\ p-MOSFET$

F. $A \rightarrow Depletion\ p-MOSFET$; $B \rightarrow Depletion\ n-MOSFET$

7. (1 mark) Given below are two statements regarding I_D in PMOS and NMOS devices.

Assume same $|V|$ & W/L for both devices

$S1$: Drain current for a NMOS device $(I_{D,NMOS})$ > Drain current for a PMOS device $(I_{D,PMOS})$ for a particular V_{GS}

$S2$: Mobility of a PMOS device (μ_P) < Mobility of an NMOS device (μ_N) at the interface

A. Statement $S1$ is true and $S2$ is false

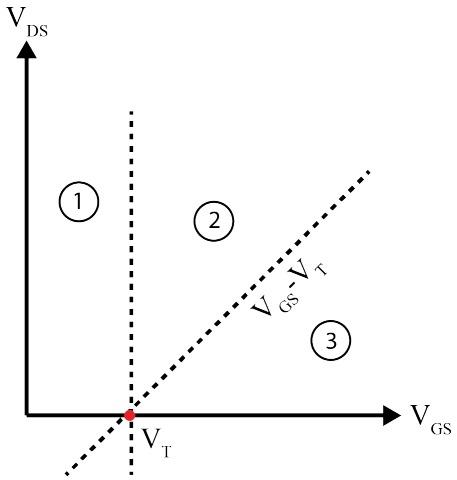
B. Statement $S1$ is false and $S2$ is true

C. Statement $S1$ is true and $S2$ is true and $S2$ is the correct explanation of $S1$

D. Statement $S1$ is true and $S2$ is true and $S2$ is not the correct explanation of $S1$

E. Statement $S1$ and $S2$ are false

8. (2 marks) The V_{DS} vs V_{GS} plot for a NMOSFET is given in figure 3. Map the regions in the graph from the corresponding options in the table.



A	Accumulation
B	Pinch-off
C	Depletion
D	Off
E	Breakdown
F	Saturation
G	Amplification
H	Ohmic

Figure 3: V_{GS} vs V_{DS}

A. $1 \rightarrow H;\ 2 \rightarrow F;\ 3 \rightarrow B$

B. $1 \rightarrow F;\ 2 \rightarrow B$ and $C;\ 3 \rightarrow A$ and H

C. $1 \rightarrow C$ and $D;\ 2 \rightarrow F;\ 3 \rightarrow H$

D. $1 \rightarrow D;\ 2 \rightarrow H;\ 3 \rightarrow F$

E. $1 \rightarrow A;\ 2 \rightarrow G;\ 3 \rightarrow E$

F. $1 \rightarrow B$ and $C;\ 2 \rightarrow A$ and $F;\ 3 \rightarrow H$

9. (1 mark) Given below are two statements regarding substrate bias in NMOSFET.

$S1$: Source-to-body bias V_{SB} must always be greater than or equal to zero for an NMOSFET.

$S2$: The source-to-substrate pn junction must always be either grounded or forward biased for appropriate transistor action.

A. Statement $S1$ is true and $S2$ is false

B. Statement $S1$ is false and $S2$ is true

C. Statement $S1$ is true and $S2$ is true and $S2$ is the correct explanation of $S1$

D. Statement $S1$ is true and $S2$ is true and $S2$ is not the correct explanation of $S1$

E. Statement $S1$ and $S2$ are false

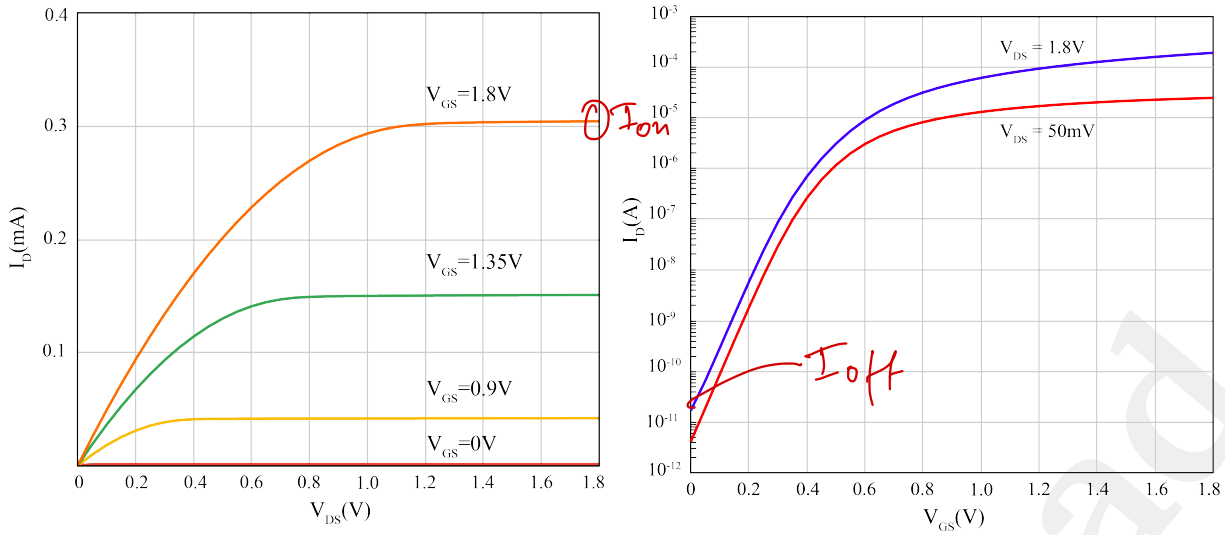


Figure 4: $I-V$ Characteristics Problem

10. (2 marks) The $I-V$ characteristics of an NMOSFET are shown in figure 4.

(a) (*1 mark*) The ON current $(I_{D,on})$ is approximately _____ (in mA)

A. 0.1

B. 0.01

C. 0.02

D. 0.3

E. 0.03

F. 0.25

On current is I_D when $V_{GS} = V_{DS} = V_{DD}$

(b) (*1 mark*) The OFF current $(I_{D,off})$ is approximately _____ pA $(1pA = 10^{-12}\ A)$

A. 2

B. 20

C. 80

D. 4

E. 200

F. 400

I_{off} is I_d when $V_{GS} = 0$ & $V_{DS} = V_{DD}$

Need to check I_D on log scale for accurate answer.

11. (2 marks) A silicon MOSFET has the following parameters: $N_a = 10^{16}\ cm^{-3}$, $t_{ox} = 12\ nm$, $\epsilon_{SiO_2} = 3.9$, $\epsilon_{Si} = 11.7$, and $\phi_f = 0.3473\ V$.

(a) (*1 mark*) The body effect coefficient (γ) is _____ $V^{\frac{1}{2}}$

A. 0.12

B. 0.15

C. 0.20

D. 0.22

E. 0.3

F. 0.32

$\gamma = \frac{\sqrt{2 q \epsilon_{Si} N_a}}{C_{ox}} = \frac{\sqrt{2 \times 1.6 \times 10^{-19} \times 11.7 \times 8.85 \times 10^{-14} \times \sqrt{10^{16}}}}{\frac{3.9 \times 8.85 \times 10^{-14}}{12 \times 10^{-7}\ cm}}$

$= 0.2\ V^{1/2}$

(b) (*1 mark*) The change in threshold voltage for $V_{T0} = 0.64$ and $V_{SB} = 2\ V$ is _____ V (*rounded off to two decimal places*)

Ans: 0.16

Range: $0.10 - 0.20$

$\Delta V_T = \gamma\left(\sqrt{2\psi_F + |V_{SB}|} - \sqrt{2\psi_F}\right)$

$= 0.2 \times \left(\sqrt{2 \times 0.3473 + 2} - \sqrt{2 \times 0.3473}\right)$

$= 0.16$

Previous year GATE questions

12. (2 marks) **(EC-GATE 2016)** Consider long channel NMOS transistor with source and body connected together. Assume that the electron mobility is independent of V_{GS} and V_{DS}.

Given,

$g_m = 0.5\ \mu A/V$ for $V_{DS} = 50\ mV$ *and* $V_{GS} = 2\ V$ and

$g_d = 8\ \mu A/V$ for $V_{DS} = 0\ V$ *and* $V_{GS} = 2\ V$

Where

$g_m = \frac{\partial I_D}{\partial V_{GS}}$ and $g_d = \frac{\partial I_D}{\partial V_{DS}}$.

The threshold voltage (in V) of the transistor is _____

Ans: $V_T = 1.2$

Range: $V_T = 1.0 - 1.5$

$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{ox} \frac{W}{L} V_{DS}$

$\Rightarrow 0.5 \times 10^{-6} = \mu C_{ox} \frac{W}{L} \times 50 \times 10^{-3}$

$g_d = \frac{\partial I_D}{\partial V_{DS}} = \mu C_{ox} \frac{W}{L}\left((V_{GS} - V_T) - V_{DS}\right)$

At $V_{DS} = 0$

$8 \times 10^{-6} = \frac{0.5 \times 10^{-6}}{50 \times 10^{-3}}(2 - V_T)$

$V_T = 2 - 0.8 = 1.2V$

13. (1 mark) **(EC-GATE 2017)** An n-channel enhancement mode MOSFET is biased at $V_{GS} > V_{TH}$ and $V_{DS} > (V_{GS} - V_{TH})$, where V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage and V_{TH} is the threshold voltage. Considering channel length modulation effect to be significant, the MOSFET behaves as a -

MOSFET behaves as a current source in saturation!

A. voltage source with zero output impedance

B. voltage source with non-zero output impedance

C. current source with finite output impedance

D. current source with infinite output impedance

Due to CLM I_D increases slowly with V_{DS} ∴ O/p impedence is finite

14. (2 marks) **(EC-GATE 2019)** Consider a long-channel MOSFET with a channel length $1\ \mu m$ and width $10\ \mu m$. The device parameters are: acceptor concentration $N_A = 5 \times 10^{16}\ cm^{-3}$, electron mobility $\mu_n = 800\ cm^2(V-s)^{-1}$, oxide capacitance per unit area $C_{ox} = 3.45 \times 10^{-7}\ Fcm^{-2}$, threshold voltage $V_T = 0.7\ V$. The drain saturation current I_{Dsat} for a gate voltage of $5\ V$ is _____mA (rounded off to ~~two~~ one decimal places). ($\epsilon_0 = 8.854 \times 10^{-14}\ Fcm^{-1}$, $\epsilon_{Si} = 11.9$)

Ans: 25.52

Range: $25.49 - 25.55$

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

$$= \frac{1}{2} 800 \times 3.45 \times 10^{-7} \times 10 \times (4.3)^2$$

$$= 25.5\ mA$$

15. (1 mark) **(EC-GATE 2008)** The drain current of a MOSFET in saturation region is given by $I_D = K(V_{GS} - V_T)^2$, where K is a constant. The magnitude of the transconductance g_m is -

A. $K(V_{GS} - V_T)^2/V_{DS}$

B. $I_D/(V_{GS} - V_{DS})$

C. $2K(V_{GS} - V_T)$

D. $K(V_{GS} - V_T)^2/V_{GS}$

$I_D = K(V_{GS} - V_T)^2$

$g_m = \frac{\partial I_D}{\partial V_{GS}} = 2K(V_{GS} - V_T)$