

**Solve the following questions. There are 11 questions, for a total of 25 marks.**

1. (6 marks) According to the MOSFET scaling proposed by Dennard, choose the correct options with regards to the scaling of the MOSFET parameters.

(a) (1 mark) For a scaling factor  $\alpha$ , the vertical ( $V$ ) and lateral ( $L$ ) dimensions are scaled as -

- A.  $V \uparrow$  to  $\alpha V$  and  $L \uparrow$  to  $\alpha L$
- B.  $V \downarrow$  to  $\alpha V$  and  $L \uparrow$  to  $\alpha L$
- C.  $V \downarrow$  to  $\alpha V$  and  $L \downarrow$  to  $\alpha L$**
- D.  $V \uparrow$  to  $\alpha V$  and  $L \downarrow$  to  $\alpha L$
- E.  $V$  remains constant and  $L \downarrow$  to  $\alpha L$
- F.  $V \uparrow$  to  $\alpha V$  and  $L$  remains constant

(b) (1 mark) For a scaling factor  $\alpha$ , the supply voltage ( $V_{DD}$ ) and doping concentrations ( $N$ ) scale as -

- A.  $V_{DD} \uparrow$  to  $\alpha V_{DD}$  and  $N \downarrow$  to  $\alpha N$
- B.  $V_{DD} \uparrow$  to  $\alpha V_{DD}$  and  $N \uparrow$  to  $\alpha N$
- C.  $V_{DD} \downarrow$  to  $\alpha V_{DD}$  and  $N \downarrow$  to  $\alpha N$
- D.  $V_{DD} \downarrow$  to  $\alpha V_{DD}$  and  $N \uparrow$  to  $\alpha N$**
- E.  $V_{DD} \downarrow$  to  $\alpha V_{DD}$  and  $N$  remains constant
- F.  $V_{DD}$  remains constant and  $N \uparrow$  to  $\alpha N$

(c) (2 marks) For a scaling factor  $\alpha$ , the total gate capacitance  $C_G$  scales as -

- A.  $C_G \downarrow$  to  $\alpha C_G$**
- B.  $C_G \uparrow$  to  $\alpha C_G$
- C.  $C_G \downarrow$  to  $\alpha^2 C_G$
- D.  $C_G \uparrow$  to  $\alpha^3 C_G$
- E.  $C_G \uparrow$  to  $\alpha^2 C_G$
- F.  $C_G$  does not change

(d) (2 marks) For a scaling factor  $\alpha$ , the delay in the circuit  $t_d$  scales as -

- A.  $t_d \uparrow$  to  $\alpha t_d$
- B.  $t_d \downarrow$  to  $\alpha^2 t_d$
- C.  $t_d \uparrow$  to  $\alpha^2 t_d$
- D.  $t_d \downarrow$  to  $\alpha^{0.5} t_d$

E.  $t_d \uparrow$  to  $\alpha^{0.5} t_d$

**F.  $t_d \downarrow$  to  $\alpha t_d$**

2. (1 mark) The law which qualitatively captures the doubling of transistors every two years on a chip is -

A. Murphy's Law

B. Murray's law

**C. Moore's law**

D. Marconi's law

E. Mobius's Law

F. Mephisto's law

3. (1 mark) Given below are two statements regarding the characteristics of a short channel MOSFET.

$S_1$  : Typically, the channel lengths for a short channel MOSFET are much larger than the depletion widths of the source and drain junctions.

$S_2$  : The current in a short channel MOSFET shows significant deviations from the square law theory.

A. Statement  $S_1$  is true and  $S_2$  is false

**B. Statement  $S_1$  is false and  $S_2$  is true**

C. Both Statement  $S_1$  and  $S_2$  are false

D. Both Statement  $S_1$  and  $S_2$  are true

4. (1 mark) Given below are two statements regarding the current in a short channel MOSFET.

$S_1$  : Typically,  $I_D$  in a short channel MOSFET scales linearly with gate voltage  $V_{GS}$ .

$S_2$  : The magnitude of current in a short channel MOSFET is comparable or larger than that of long channel MOSFETs.

**A. Statement  $S_1$  is true and  $S_2$  is false**

B. Statement  $S_1$  is false and  $S_2$  is true

C. Both Statement  $S_1$  and  $S_2$  are false

D. Both Statement  $S_1$  and  $S_2$  are true

5. (1 mark) Given below are two statements regarding the current in a short channel MOSFET.

$S_1$  : The current for a short channel MOSFET saturates at a larger  $V_{DS}$  as compared to long channel MOSFET

$S_2$  : The short channel reaches the critical field at smaller applied biases leading to velocity saturation.

A. Statement  $S1$  is true and  $S2$  is false

**B. Statement  $S1$  is false and  $S2$  is true**

C. Statement  $S1$  and  $S2$  is true and  $S2$  is the correct explanation for  $S1$

D. Statement  $S1$  and  $S2$  is true and  $S2$  is not the correct explanation for  $S1$

6. (5 marks) In figure 1,  $V_{DS}$  vs  $I_D$  for two MOSFETS having different lengths is plotted for a gate voltage  $V_{GS} = 1.8$  V. The  $W/L$  ratio for both MOSFETS is kept constant. Answer the following questions based on the given data.

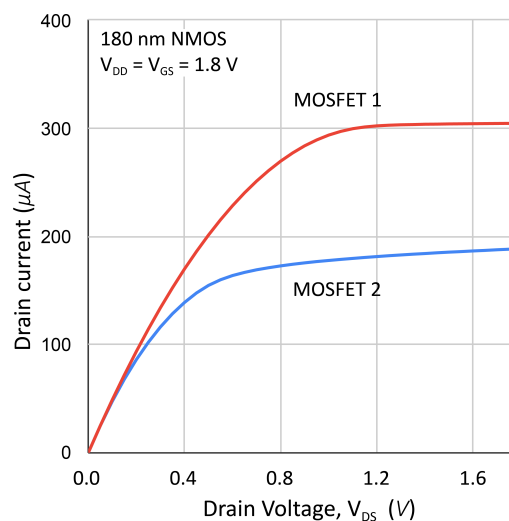


Figure 1: MOSFET  $V_{DS}$  vs  $I_D$

- (a) (1 mark) Identify the type of MOSFET corresponding to the curves given in the figure

A. MOSFET 1  $\rightarrow$  Short Channel; MOSFET 2  $\rightarrow$  Short Channel

**B. MOSFET 1  $\rightarrow$  Long Channel; MOSFET 2  $\rightarrow$  Short Channel**

C. MOSFET 1  $\rightarrow$  Long Channel; MOSFET 2  $\rightarrow$  Long Channel

D. MOSFET 1  $\rightarrow$  Short Channel; MOSFET 2  $\rightarrow$  Long Channel

- (b) (2 marks) Choose the correct option(s) with regards to critical electric field  $\mathcal{E}_c$  at which velocity saturation occurs in a short channel MOSFET -

**A. Electric field across the channel of MOSFET 1  $< \mathcal{E}_c$**

B. Electric field across the channel of MOSFET 2  $< \mathcal{E}_c$

C. Electric field across the channel of MOSFET 1  $> \mathcal{E}_c$

D. Electric field across the channel of MOSFET 1 = Electric field across the channel of MOSFET 2  $< \mathcal{E}_c$

**E. Electric field across the channel of MOSFET 2  $> \mathcal{E}_c$**

F. Electric field across the channel of MOSFET 1 = Electric field across the channel of MOSFET 2  $> \mathcal{E}_c$

(c) (2 marks) The approximate  $V_{DSat}$  for the MOSFETS is -

A. MOSFET 1  $\rightarrow V_{DSat} = 0.4 \text{ V}$  and MOSFET 2  $\rightarrow V_{DSat} = 0.2 \text{ V}$

**B. MOSFET 1  $\rightarrow V_{DSat} = 1 \text{ V}$  and MOSFET 2  $\rightarrow V_{DSat} = 0.4 \text{ V}$**

C. MOSFET 1  $\rightarrow V_{DSat} = 0.2 \text{ V}$  and MOSFET 2  $\rightarrow V_{DSat} = 1 \text{ V}$

D. MOSFET 1  $\rightarrow V_{DSat} = 1 \text{ V}$  and MOSFET 2  $\rightarrow V_{DSat} = 1 \text{ V}$

E. MOSFET 1  $\rightarrow V_{DSat} = 0.6 \text{ V}$  and MOSFET 2  $\rightarrow V_{DSat} = 0.6 \text{ V}$

F. MOSFET 1  $\rightarrow V_{DSat} = 1 \text{ V}$  and MOSFET 2  $\rightarrow V_{DSat} = 1.8 \text{ V}$

7. (2 marks) In a short channel MOSFET, as  $V_{DS}$  is increased -

A. Effective channel length  $L_{eff} \downarrow$  and total drain current  $I_D \downarrow$

**B. Effective channel length  $L_{eff} \downarrow$  and total drain current  $I_D \uparrow$**

C. Effective channel length  $L_{eff} \uparrow$  and total drain current  $I_D \uparrow$

D. Effective channel length  $L_{eff} \uparrow$  and total drain current  $I_D \downarrow$

E. Effective channel length  $L_{eff} \downarrow$  and total drain current  $I_D$  remains constant

F. Effective channel length  $L_{eff}$  remains constant and total drain current  $I_D \downarrow$

8. (2 marks) In a short channel MOSFET, as  $V_{DS}$  is increased -

**A. The barrier across the gate is lowered, leading to an increased off-current,  $I_{off}$**

B. The barrier across the gate is increased, leading to an increased off-current,  $I_{off}$

C. The barrier across the gate is lowered, leading to an reduced off-current,  $I_{off}$

D. The barrier across the gate is increased, leading to a reduced off-current,  $I_{off}$

E. The barrier across the gate is unimpacted.

9. (1 mark) In the year 2007, high-k dielectric and metal gate were introduced in the 45 nm technology node primarily -

A. to increase mobility of electrons resulting from strain due to high-k dielectric

- B. due to inefficient contact between polysilicon and  $SiO_2$  layer
  - C. to reduce the drive current for an applied gate voltage
  - D. to reduce the leakage current due to tunneling across  $SiO_2$  layer**
  - E. to reduce the DIBL resulting from scaling the devices
10. (2 marks) The reason(s) for introduction of the trigate transistor, or FinFET, in 2011 was -
- A. to reduce tunneling across the oxide layer
  - B. to achieve more gate control over the inversion layer formation**
  - C. to increase the critical electric field over which velocity saturation occurs
  - D. to further reduce the dimensions of the transistor as scaling using planar technology was not feasible**
  - E. to improve the tunneling across the junction for better channel control
11. (3 marks) Given below are a few statements regarding the FinFET technology. Choose the correct statements.
- A : FinFET technology allows packaging more transistors in a given area than the planar technology
  - B : FinFET offers better electrostatic control over the gate than planar MOSFETS
  - C : FinFET has lower  $I_{ON}$  to  $I_{OFF}$  ratio than planar MOSFETS
  - D : FinFET has lower leakage current than planar MOSFETS
  - E : For a similar operating voltage, planar MOSFETS offers much lower delays than FinFET.
- A. B, C, E
  - B. A, B, E
  - C. A, B, D**
  - D. C, D, E
  - E. A, B, C, D