# Tutorial 2

1. Performance: Latency vs. Throughput

**Car:** speed = 60 miles/hour, capacity = 5
**Bus:** speed = 20 miles/hour, capacity = 60

**Task:** transport passengers 10 miles

| | Latency (min) | Throughput (PPH) |
|---|---|---|
| **Car** | | |
| **Bus** | | |

- **Latency**
  Car = 10 min, Bus = 30 min
  - Car is __ times faster than bus
  - Car is _% faster than bus

- **Throughput**
  Car = 15 PPH, Bus = 60 PPH
  - Bus is _ times faster than car
  - Bus is _% faster than car

2. CPI Example

- Assume a processor with instruction frequencies and costs
  - Integer ALU: 50%, 1 cycle
  - Load: 20%, 5 cycle
  - Store: 10%, 1 cycle
  - Branch: 20%, 2 cycle
- Which change would improve performance more?
  A: "Branch prediction" to reduce branch cost to 1 cycle?
  B: "Cache" to reduce load cost to 3 cycles?
- Compute CPI

| | INT | LD | ST | BR | CPI |
|---|---|---|---|---|---|
| Base | | | | | |
| A | | | | | |
| B | | | | | |

3 Computer A has a clock cycle time of 250 ps and a CPI of 2.0 for a program, and machine B has a clock cycle time of 500 ps and a CPI of 1.2 for the same program. Which machine is faster for this program, and by how much?

4.

| Instruction class | CPI for this instruction class |
|---|---|
| A | 1 |
| B | 2 |
| C | 3 |

| Code sequence | Instruction counts for instruction class | | |
|---|---|---|---|
| | A | B | C |
| 1 | 2 | 1 | 2 |
| 2 | 4 | 1 | 1 |

Which code sequence executes the most instructions? -

Which will be faster?
What is the CPI for each sequence?

5.

Processor A runs at 200 MHz and executes a 40 million instruction program at a sustained 50 MIPS • Processor B runs at 400 MHz and executes the same program (w/ a different compiler) which yields a count of 60 million instructions and a CPI of 6 • What is the CPI of the program on Proc. A? • Which processor executes the program faster and by what factor? • What is the MIPS rate of Proc. B?

6.

Calculate CPI of this snippet of code using the following CPI's for each instruction type

```
        add     $s0,$zero,$zero
        addi    $t1,$zero,4
loop:   lw      $t2,0($t0)
        add     $t2,$t2,$t1
        addi    $t0,$t0,4
        addi    $t1,$t1,-1
        bne     $t1,$zero,loop
        sw      $t2,0($t2)
```

| Instruction Type | CPI |
|---|---|
| add | 1 |
| lw / sw | 4 |
| bne | 2 |

Dynamic Instruction Count = 4*5 + 3 = 23

$$CPI = \sum_i CPI_{Type\_i} * P(InstructionType_i)$$

| Instruction Type | Dynamic Count |
|---|---|
| add | 14 |
| lw / sw | 5 |
| bne | 4 |

7. Our favorite program runs in 10 seconds on computer A, which has a 400 MHz clock. We are trying to help a computer designer build a new machine B, that will run this program in 6 seconds. The designer can use new (or perhaps more expensive) technology to substantially increase the clock rate, but has informed us that this increase will affect the rest of the CPU design, causing machine B to require 1.2 times as many clock cycles as machine A for the same program. What clock rate should we tell the designer to target at?