

OpenRV 5-Stage Pipeline CPU and SoC System

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Project Overview

Overview: Lightweight RISC-V soft core for programmable control and rapid prototyping
Architecture: Harvard architecture with dual AHB-Lite ports
Application: Embedded control, sensor interfacing, hardware acceleration

Key Innovations

Software+CPU control plane design
Plug-and-play AHB peripheral integration
Flexible state machine management
Unified bus protocol interface

Core Architecture

• Pipeline Design:

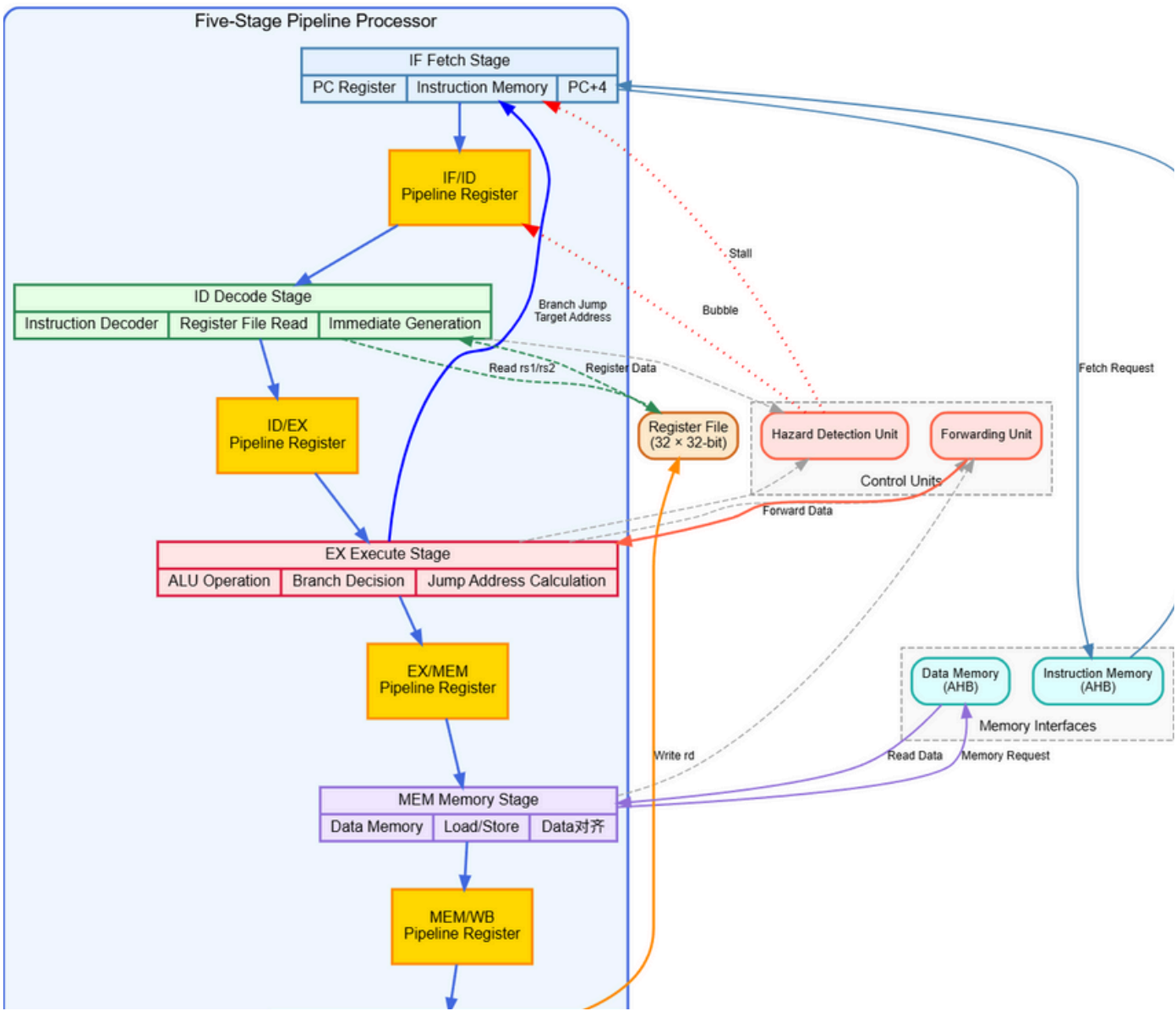
Five-stage RISC-V pipeline with forwarding
Load-Use hazard detection and resolution
Branch prediction and resolution logic

• Memory System:

Separate instruction/data AHB ports
Byte/halfword/word memory access
IROM/BRAM controllers with AHBbridge

• Peripheral Integration

PLL clock, button, LED, 7-seg display, UART



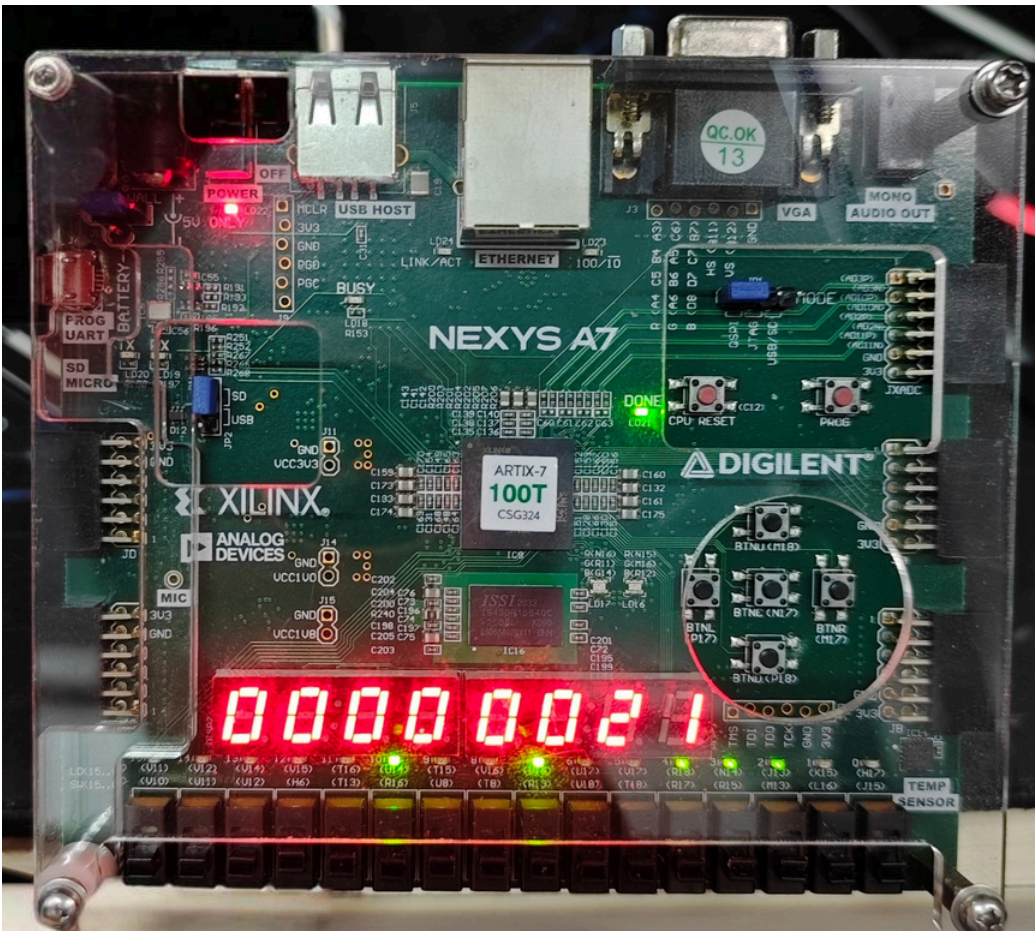
Verification & Results

• Hardware Verification:

RISC-V compliancetest suite passed
Custom tests for peripherals
Real-world control applications

• Performance

Frequency: 80-100MHz
CPI : ≈ 1 (ideal pipeline throughput)
Single-cycle memory access



Program running on our FPGA board, meaning pass 0x21 (33 in dec) instruction tests.

Project Value

Engineering Practicality: Programmable controller for peripherals/accelerators
Easy Integration: Standardized AHB-Lite interface
Rapid Proto typing: Quick Ip integration and software driver reuse
Edu Value: Teaching platform for HW/SW co-design

references

[1] ARM Ltd. (n.d.). *AMBA AHB Protocol Specification (IHI 0033)*. Retrieved October 30, 2025, from [https://developer.arm.com/documentation/ihi0033/latest/]
[2] darklife. (n.d.). *darkriscv: RISC-V compatible softcore implemented in Verilog*. GitHub repository. Retrieved October 30, 2025, from [https://github.com/darklife/darkriscv]
[3] RISC-V Software Source. (n.d.). *riscv-tests: RISC-V ISA tests*. GitHub repository. Retrieved October 30, 2025, from [https://github.com/riscv-software-src/riscv-tests]