FPGA Innovation Design Contest

OpenRV 5-Stage Pipeline SoC System

Team Name
University
Supervisor

2025 National College Student
Embedded Chip and System Design Competition

November 2025

Project Overview

Overview: Lightweight RISC-V soft core for programmable control and rapid prototyping

Architecture: Harvard architecture with dual AHB-Lite ports

Application: Embedded control, sensor interfacing, hardware acceleration

Key Innovations

Software + CPU control plane design

Plug-and-play AHB peripheral integration

Flexible state machine management

Unified bus protocol interface

Technical Specs

ISA:	RV32I Base Integer
Pipeline:	5-stage
Interface:	Dual AHB-Lite
Platform:	Artix-7 FPGA

Core Architecture

Pipeline Design:

- Five-stage RISC-V pipeline with forwarding
- Load-Use hazard detection and resolution
- Branch prediction and resolution logic
- Full RV32I instruction support

Memory System:

- Separate instruction/data AHB ports
- Byte/halfword/word memory access
- IROM/BRAM controllers with AHB bridge

System Integration

[Block Diagram]
Place the top-level architecture diagram from report section 2.2.1

Layered design with core and bus interconnect

Standard AHB-Lite protocol for all peripherals

Configurable address mapping and decoding

Peripheral Integration

[Peripheral Interface]
Place the AHB peripheral connection diagram here

Basic Peripherals:

- Configurable PLL clock management
- 5-button input with debouncing
- 16 LEDs + 2 RGB LEDs
- 8-digit seven-segment display
- UART (9600 baud) for debugging

Verification & Results

Hardware Verification:

- RISC-V compliance test suite passed
- Custom tests for peripherals
- Real-world control applications

Performance:

- Target frequency: 50-100 MHz
- CPI 1 (ideal pipeline throughput)
- Single-cycle memory access

Project Value

Engineering Practicality: Programmable controller for peripherals/accelerators

Easy Integration: Standardized AHB-Lite interface

Rapid Prototyping: Quick IP integration and software driver reuse

Educational Value: Teaching platform for HW/SW co-design

Future Directions

RV32M extension implementation

Cache hierarchy enhancement

Advanced branch prediction

DMA and interrupt controller

Additional peripheral support

Contact & Resources

Repository: github.com/Narwhal-Wu/LibreCore
Documentation: Project Wiki & API Reference
Development: Vivado 2023.2