★★★ MODULE APPLICATION NOTE APPROVAL FORM ★★★
模块应用指引确认单

MOUDLE PART NUMBER:
模块型号：/
Sample Lot No.:/
样品单号： /
Prepared By:
制作：Zhao Yaqi
Date:
日期：2017-7-27

APPLICATION NOTE VERSION:
应用文档版本：0.1
Qty:/
数量：/
Approved By:
审批： Zhan Junbin
Date:
日期：2017-7-27

Customer Name（客户名称）：/

The intent of this form is for you to provide confirmation as to the accompanying module sample meeting your testing criteria.。Once you have completed your evaluation,please sign and date the appropriate approvedor rejected signature block,along with any comments you wish to make, After we are in receipt of this document reflecting approval of this test condition ,if you issue a purchase order, we will begin to product this module with the test condition of this document.
此表格中的所有项目内容仅用于确认模块样品是否符合测试标准。请相关人员评估各个项目之后，在其后面的Appr'd一栏的空格中或者Rej'd一栏的空格中签名，并填写时间和意见。如果所有项目都确认OK并回传此确认函至我司，我司将按照此文件所确认的测试标准进行后续订单的生产。

* CHECK ITEM	STATUS	
	Appr'd	Rej'd
The schematic of the testing circuit and the value of components 测试线路的原理图和元器件的电气值	As Application Note V0.1	
The input voltage and current of the testing circuit测试线路的输入电压和输入电流值	As Application Note V0.1	
The software setting 软件设置	As Application Note V0.1	

Specification规格
(If Appr'd,Please write APPLICATION NOTE's REV NO ;
如果确认OK，请填写APPLICATION NOTE的版本编码
If Rej'd,Please write improving advice)
如果确认NG，请填写改善建议。

Notes:

① If APPLICATION NOTE is updated ,we use approval APPLICATION NOTE's the latest version as a testing condition.
如果APPLICATION NOTE有所更新，我们将以最新版本的APPLICATION NOTE的测试条件为准

② If APPLICATION NOTE approval item is default ,it means that you accept APPLICATION NOTE's contents.
如果APPLICATION NOTE的某些项目没有做出回应，将默认为确认OK。

③ If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.
如果液晶显示模块长时间工作于同一个显示图案，换屏时会出现鬼影，也会出现轻微的对比

度不均。停止使用一段时间后可恢复到正常状态。此现象不会严重影响性能可靠性。

* NOTE: Please place an ″√″ in the appropriate Approved or Rejected block for each subject category 备注：每个项目，如果确认OK，请在后续的Appr'd栏的空格打″√″，如果确认NG，请在Rej'd栏的空格打″√″。

APPROVED 批准	*** COMMENTS *** 评论	AUTHORIZED SIGNATURE&DATE 签字及日期
REJECTED 拒绝		

If customer don't agree the APPLICATION NOTE ,please provide customer's testing tool and inspecting method.

若客户拒绝此模块应用指引 ,请提供客户的测试工具及检测方法。

PRODUCT : LCD MODULE

SUPPLIER : TRULY SEMICONDUCTORS LTD.

CERT. No.QAC0946535 (ISO9001)

CERT. No.HKG002005 (ISO14001)

/

APPLICATION NOTE

This application note is only for reference and maybe changed without any notice .
Please contact TRULY R&D department for update files and product status before design for this product or release the order.

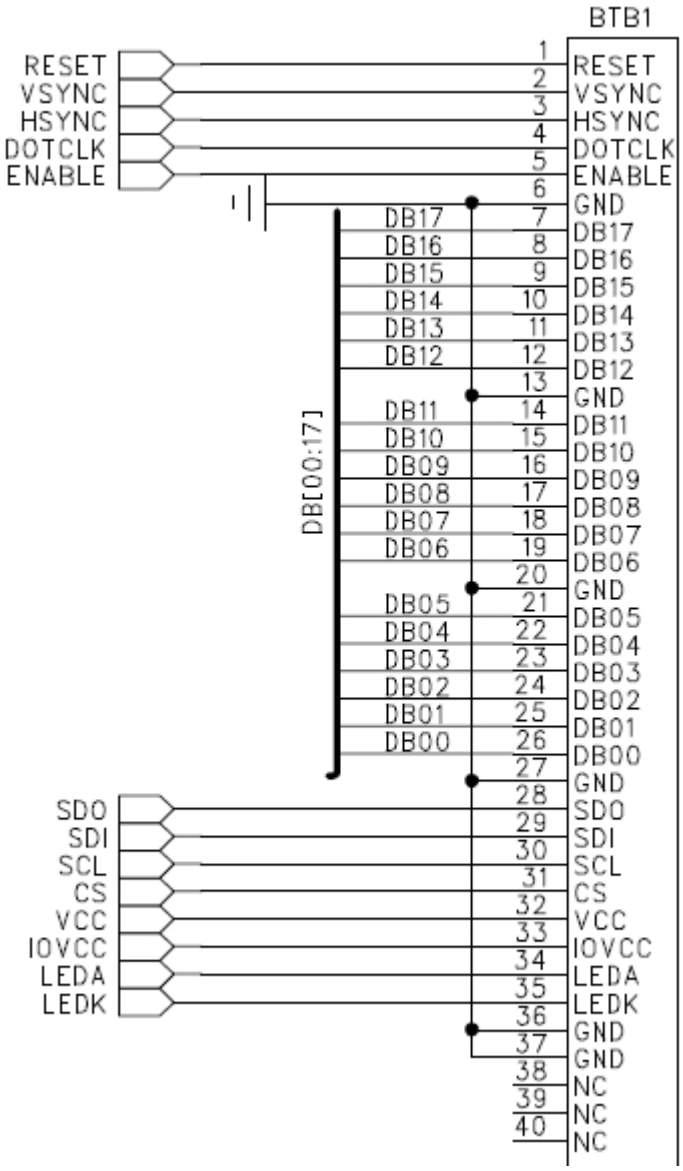
WRITTEN BY	APPROVED BY
Zhao Yaqi	Zhan Junbin

■ APPLICATION CIRCUIT

测试外围电路：
24-Bit RGB Interface
VCC=IOVCC=3.3V
Backlight:If=20mA， Vf= 10.0V~13.2V（TYP 12V）

-The MCU interface mode select.

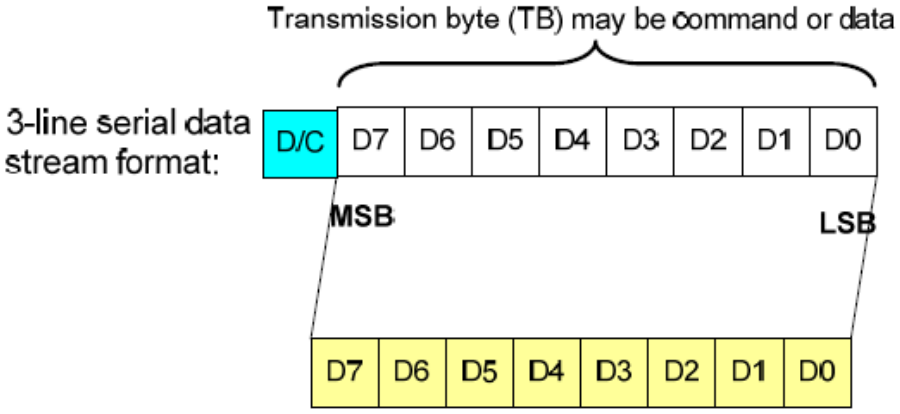
IM2	IM1	IM0	MPU Interface Mode	Data pin
0	0	0	8080 18-bit Interface	DB[17:0]
0	0	1	8080 9-bit Interface	DB[8:0]
0	1	0	8080 16-bit Interface	DB[15:0]
0	1	1	8080 8-bit Interface	DB[7:0],
1	0	0	Reserve	--
1	0	1	3SPI	SDA, SDO
1	1	0	MIPI	MIPI_DATA MIPI_CLOCK
1	1	1	4 Line SPI	SDA, SDO


BTB1
RESET
VSYNC
HSYNC
DOTCLK
ENABLE
DB[00:17]
SDO
SDI
SCL
CS
VCC
IOVCC
LEDA
LEDK
1 RESET
2 VSYNC
3 HSYNC
4 DOTCLK
5 ENABLE
6 GND
7 DB17
8 DB16
9 DB15
10 DB14
11 DB13
12 DB12
13 GND
14 DB11
15 DB10
16 DB09
17 DB08
18 DB07
19 DB06
20 GND
21 DB05
22 DB04
23 DB03
24 DB02
25 DB01
26 DB00
27 GND
28 SDO
29 SDI
30 SCL
31 CS
32 VCC
33 IOVCC
34 LEDA
35 LEDK
36 GND
37 GND
38 NC
39 NC
40 NC

■ Timing Diagrams

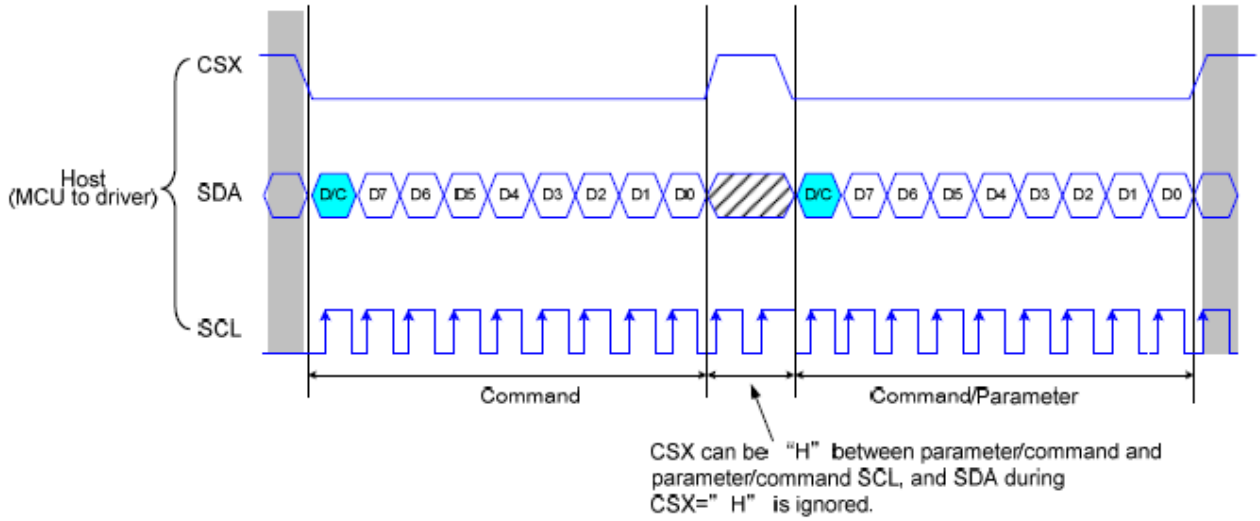
8.4.1.1 Write Sequence.

In the write mode of 3-line serial interface contains a D/CX (data/command) select bit and a transmission byte. If the D/C bit is "0", the transmission byte is interpreted as a command byte. If the D/C bit is "1", the transmission byte is display data, or stored in the command register as parameter data.



8 Bit Data Trasmission Byte

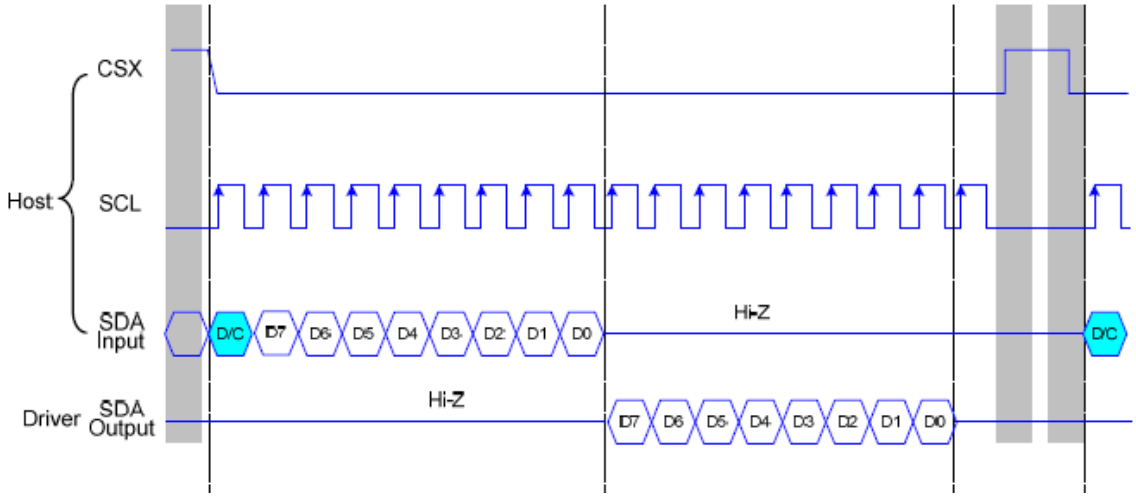
The instruction of ST7796s can be sent in any order, and the MSB is transmitted first. The 3-line serial interface is initialized when the CSX keeps high level. In this state, the SCL clock pulse and SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.



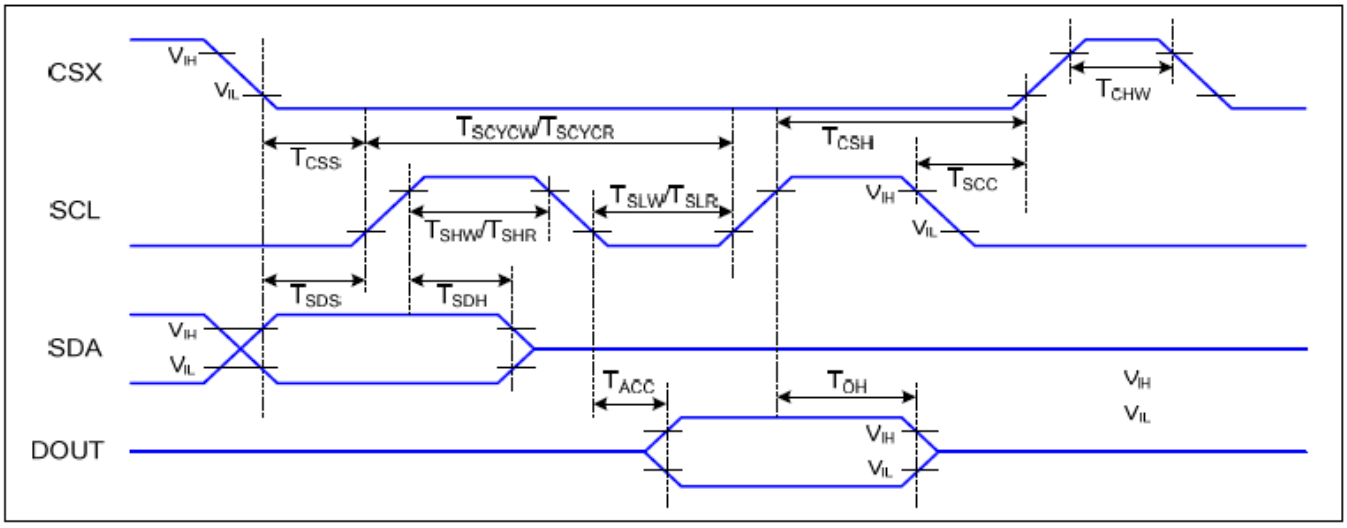
8.4.1.2 Read Sequence

In the read mode of the interface, the host reads the register value from the ST7796s. The host sends out a command (Read ID or register command), then a byte is (bytes are) transmitted in the opposite direction. The ST7796s samples the SDA (input data) at the rising edges of the SCL (serial clock), and shifts to SDO (output data) at the falling edges of the SCL (serial clock). The read mode has three types of transmitted command data (8-/24-/32-bit) according to the command code.

4-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



7.4.2 3-SPI Serial Data Transfer Interface Characteristics:



3-SPI Interface Timing Characteristics

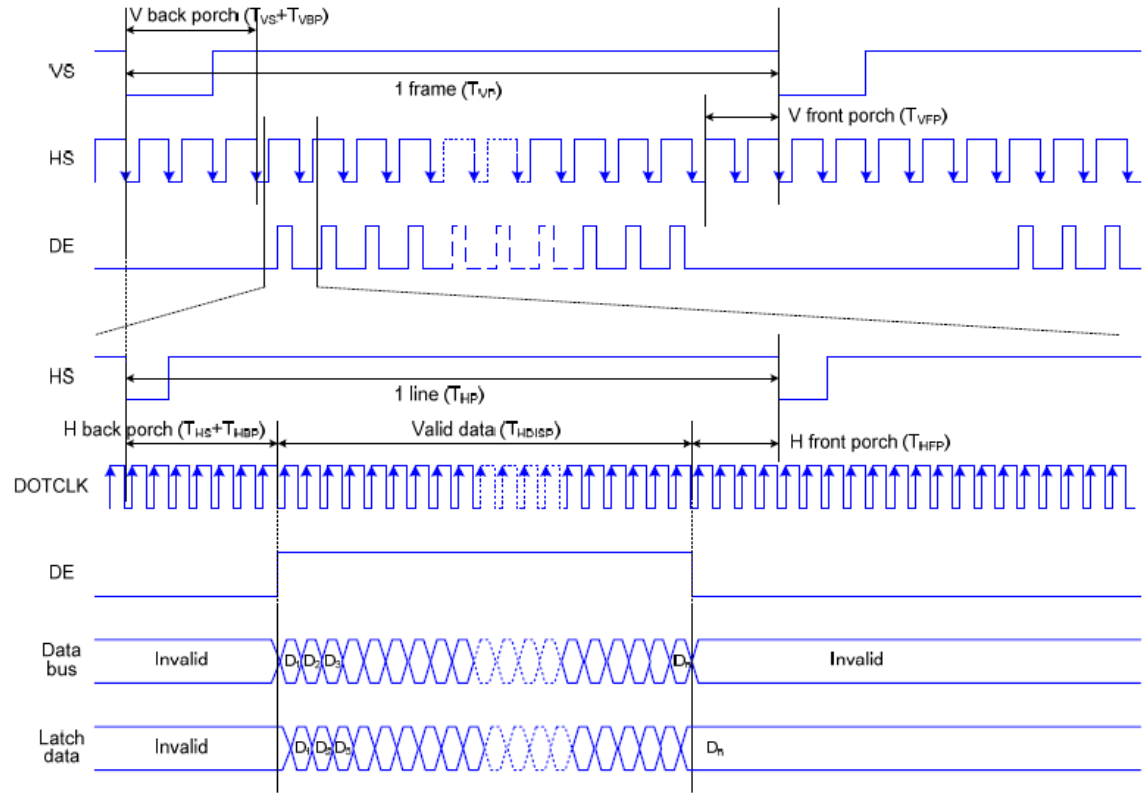
VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

3-SPI Interface Characteristics

8.3.3 RGB Interface Timing

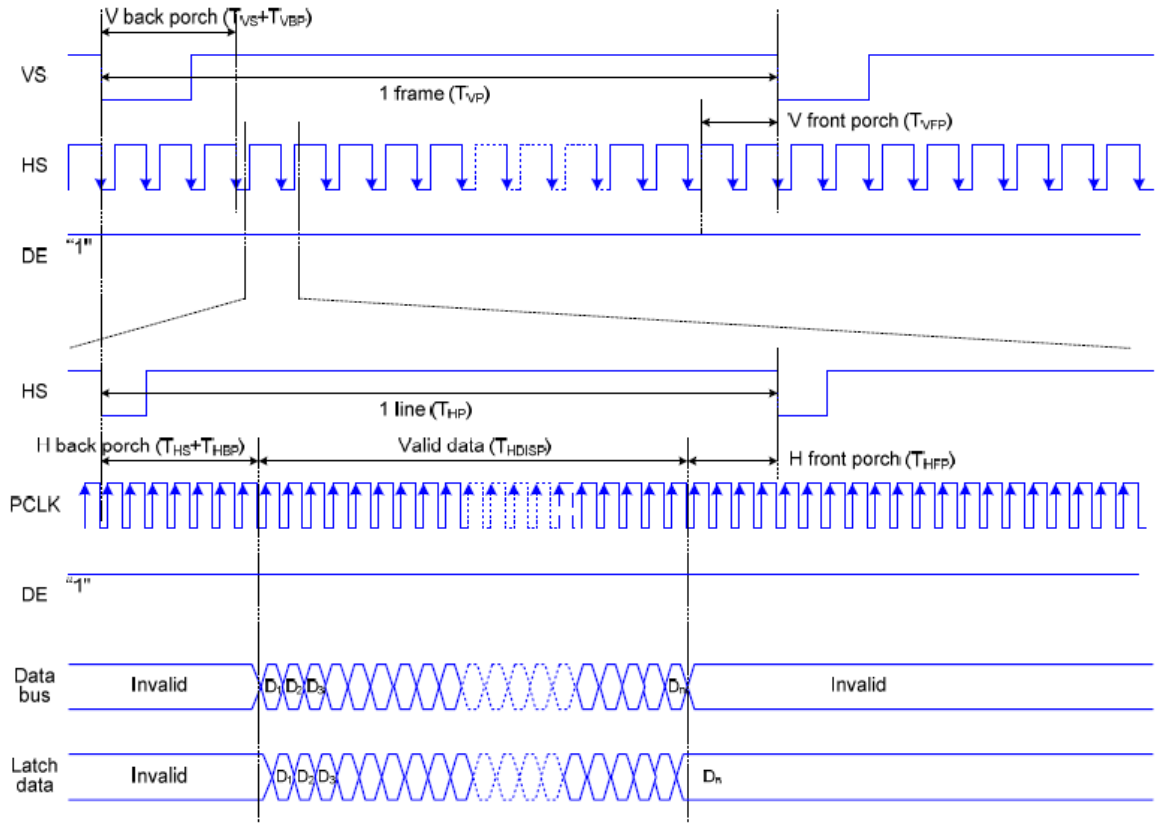
The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.



Timing chart of RGB interface HV mode

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	2	-	hpw + hbp = 75	Clock
Horizontal Sync. Back Porch	hbp	4	-		Clock
Horizontal Sync. Front Porch	hfp	2	38	-	Clock
Vertical Sync. Width	vs	2	4	-	Line
Vertical Sync. Back Porch	vbp	2	4		Line
Vertical Sync. Front Porch	vfp	2	8	-	Line

Note

■ RESET input Timing

7.4.5 Reset Timing:

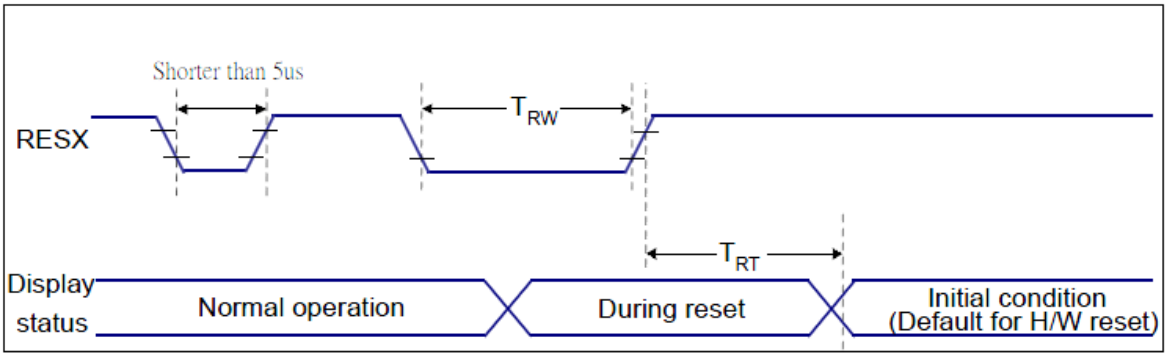


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 8 Reset Timing

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

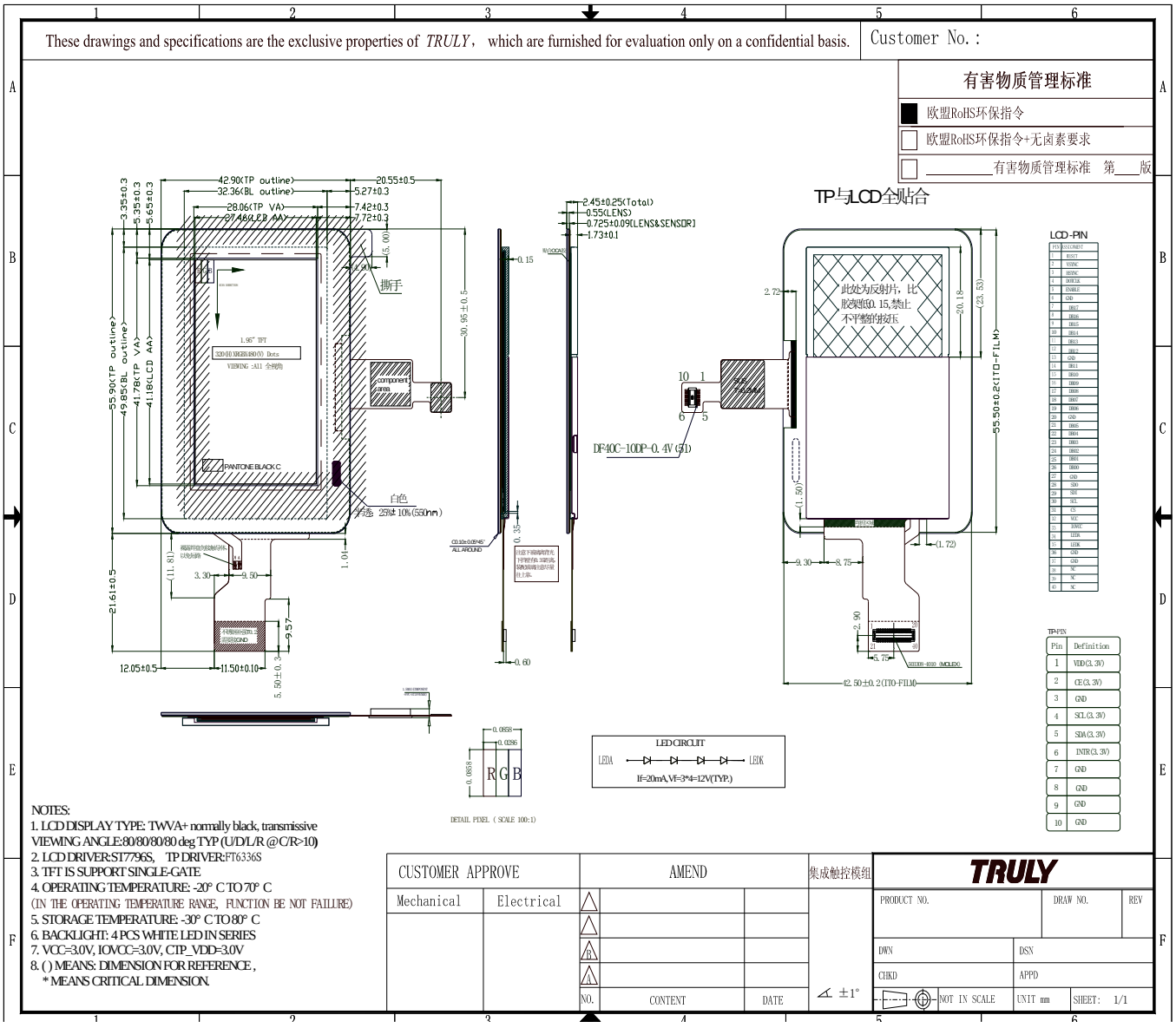
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:

■ EXTERNAL DIMENSIONS



For more information please refer to ST7796S data sheet.

■ Iintial code

```
void LCDICINIT(void) //VDD=3.3V
{
CS(1);
SCLK(1);
SDI(1);
LCD_RST(1);
WaitTime(10);
LCD_RST(0);
WaitTime(10);
LCD_RST(1);
WaitTime(150);

LCDSPI_InitCMD(0x11); //Sleep Out
WaitTime(150);

LCDSPI_InitCMD(0x36); // Memory Data Access Control MY,MX
LCDSPI_InitDAT(0x48); //

LCDSPI_InitCMD(0x3A) ;//Interface Pixel Format
LCDSPI_InitDAT(0x66) ;//

LCDSPI_InitCMD(0xF0); // Command Set Control
LCDSPI_InitDAT(0xC3);
LCDSPI_InitCMD(0xf0);
LCDSPI_InitDAT(0x96);

LCDSPI_InitCMD(0xB0) ;//Interface Mode Control
LCDSPI_InitDAT(0x80) ;// VSCP HSCP PKP DEP 极性

LCDSPI_InitCMD(0xB4) ;//Display Inversion Control
LCDSPI_InitDAT(0x01) ;//

LCDSPI_InitCMD(0xB5) ;//Display Function Control
LCDSPI_InitDAT(0x0A); //
LCDSPI_InitDAT(0x14);
LCDSPI_InitDAT(0x00);
LCDSPI_InitDAT(0x0A);

LCDSPI_InitCMD(0xB6) ;//Display Function Control
LCDSPI_InitDAT(0xB0); //
LCDSPI_InitDAT(0x02);
LCDSPI_InitDAT(0x3B);
```

```
LCDSPI_InitCMD(0xB7) ;//    Entry Mode Set
LCDSPI_InitDAT(0xC6) ; //

LCDSPI_InitCMD(0xE8) ;//Display Output Ctrl Adjust
LCDSPI_InitDAT(0x40) ;
LCDSPI_InitDAT(0x8A) ;
LCDSPI_InitDAT(0x00) ;
LCDSPI_InitDAT(0x00) ;
LCDSPI_InitDAT(0x29) ;
LCDSPI_InitDAT(0x19) ;
LCDSPI_InitDAT(0xA5) ;
LCDSPI_InitDAT(0x33) ;

LCDSPI_InitCMD(0xC0) ;//Power Control 1
LCDSPI_InitDAT(0x80) ;//AVDD，AVCL
LCDSPI_InitDAT(0x51) ;//

LCDSPI_InitCMD(0xC1) ;//VAP(GVDD),VAN(GVCL)
LCDSPI_InitDAT(0x19) ;

LCDSPI_InitCMD(0xC2) ;
LCDSPI_InitDAT(0xA7) ;

LCDSPI_InitCMD(0xc5) ;//VCOM Control
LCDSPI_InitDAT(0x08) ;//

LCDSPI_InitCMD(0xE0);
LCDSPI_InitDAT(0xA0);
LCDSPI_InitDAT(0x0B);
LCDSPI_InitDAT(0x14);
LCDSPI_InitDAT(0x0B);
LCDSPI_InitDAT(0x0B);
LCDSPI_InitDAT(0x27);
LCDSPI_InitDAT(0x3E);
LCDSPI_InitDAT(0x33);
LCDSPI_InitDAT(0x56);
LCDSPI_InitDAT(0x3B);
LCDSPI_InitDAT(0x1A);
LCDSPI_InitDAT(0x19);
LCDSPI_InitDAT(0x31);
LCDSPI_InitDAT(0x33);

LCDSPI_InitCMD(0xE1);
LCDSPI_InitDAT(0xA0);
```

```
LCDSPI_InitDAT(0x0B);
LCDSPI_InitDAT(0x14);
LCDSPI_InitDAT(0x0B);
LCDSPI_InitDAT(0x0B);
LCDSPI_InitDAT(0x27);
LCDSPI_InitDAT(0x3E);
LCDSPI_InitDAT(0x33);
LCDSPI_InitDAT(0x56);
LCDSPI_InitDAT(0x3B);
LCDSPI_InitDAT(0x1A);
LCDSPI_InitDAT(0x19);
LCDSPI_InitDAT(0x31);
LCDSPI_InitDAT(0x33);

LCDSPI_InitCMD(0xF0) ;
LCDSPI_InitDAT(0x3C) ;

LCDSPI_InitCMD(0xF0) ;
LCDSPI_InitDAT(0x69) ;
WaitTime(120); // Delay 120ms

LCDSPI_InitCMD(0x29) ; // Display ON
WaitTime(120); // Delay 120ms

LCDSPI_InitCMD(0x21) ;

}
```